Table 1 lists the key characteristics of this device.

Table 1. Device Characteristics

Name	Value
Part Number	CY8C4147AZI-S475
Package Name	64-TQFP
Family	PSoC 4
Series	PSoC 4100S Plus
Max CPU speed (MHz)	48
Flash size (kB)	128
SRAM size (kB)	16
Vdd range (V)	1.71 to 5.5
Automotive qualified	No (Industrial Grade Only)
Temp range (Celsius)	-40 to 85

NOTE: The CPU speed noted above is the maximum available speed. The CPU is clocked by HFCLK, listed in the System Clocks section below.

Table 2 lists the device resources that this design uses:

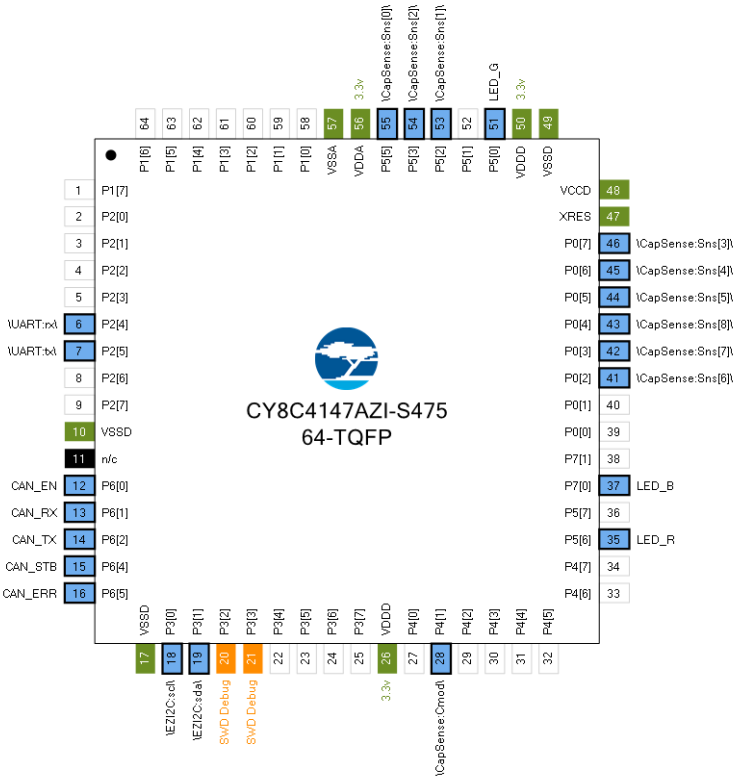
Table 2. Device Resources

Resource Type	Used	Free	Max	% Used
Interrupts	6	22	28	21.43 %
IO	24	30	54	44.44 %
Segment LCD	0	1	1	0.00 %
CapSense	1	0	1	100.00 %
Die Temp	0	1	1	0.00 %
CAN 2.0b	1	0	1	100.00 %
Serial Communication (SCB)	2	3	5	40.00 %
DMA Channels	0	8	8	0.00 %
Timer/Counter/PWM	3	5	8	37.50 %
Crypto	0	1	1	0.00 %
Smart IO Ports	0	3	3	0.00 %
Comparator/Opamp	0	2	2	0.00 %
Comparator	1	0	1	100.00 %
LP Comparator	0	2	2	0.00 %
SAR ADC	0	1	1	0.00 %
DAC				
7-bit IDAC	2	0	2	100.00 %

2 Pins

Figure 2 shows the pin layout of this device.

Figure 2. Device Pin Layout



2.1 Hardware Pins

Table 3 contains information about the pins on this device in device pin order. (No connection ["n/c"] pins have been omitted.)

Table 3. Device Pins

Pin	Port	Name	Type	Drive Mode
1	P1[7]	GPIO [unused]		
2	P2[0]	GPIO [unused]		
3	P2[1]	GPIO [unused]		
4	P2[2]	GPIO [unused]		
5	P2[3]	GPIO [unused]		
6	P2[4]	\UART:rx\	Dgtl In	HiZ digital
7	P2[5]	\UART:tx\	Dgtl Out	Strong drive
8	P2[6]	GPIO [unused]		
9	P2[7]	GPIO [unused]		
10	VSSD	VSSD	Power	
12	P6[0]	CAN_EN	Dgtl Out	Strong drive
13	P6[1]	CAN_RX	Dgtl In	HiZ digital
14	P6[2]	CAN_TX	Dgtl Out	Strong drive
15	P6[4]	CAN_STB	Software In/Out	Strong drive
16	P6[5]	CAN_ERR	Software In/Out	HiZ digital
17	VSSD	VSSD	Power	
18	P3[0]	\EZI2C:scl\	Dgtl In	OD, DL
19	P3[1]	\EZI2C:sda\	Dgtl In	OD, DL
20	P3[2]	Debug:SWD_IO	Reserved	
21	P3[3]	Debug:SWD_CK	Reserved	
22	P3[4]	GPIO [unused]		
23	P3[5]	GPIO [unused]		
24	P3[6]	GPIO [unused]		
25	P3[7]	GPIO [unused]		
26	VDDD	VDDD	Power	
27	P4[0]	GPIO [unused]		
28	P4[1]	\CapSense:Cmod\	Analog	HiZ analog
29	P4[2]	GPIO [unused]		
30	P4[3]	GPIO [unused]		
31	P4[4]	GPIO [unused]		
32	P4[5]	GPIO [unused]		
33	P4[6]	GPIO [unused]		
34	P4[7]	GPIO [unused]		
35	P5[6]	LED_R	Dgtl Out	Strong drive
36	P5[7]	GPIO [unused]		
37	P7[0]	LED_B	Dgtl Out	Strong drive
38	P7[1]	GPIO [unused]		
39	P0[0]	GPIO [unused]		
40	P0[1]	GPIO [unused]		
41	P0[2]	\CapSense:Sns[6]\	Analog	HiZ analog
42	P0[3]	\CapSense:Sns[7]\	Analog	HiZ analog
43	P0[4]	\CapSense:Sns[8]\	Analog	HiZ analog
44	P0[5]	\CapSense:Sns[5]\	Analog	HiZ analog
45	P0[6]	\CapSense:Sns[4]\	Analog	HiZ analog

Pin	Port	Name	Type	Drive Mode
46	P0[7]	\CapSense:Sns[3]\	Analog	HiZ analog
47	XRES	XRES	Dedicated	
48	VCCD	VCCD	Power	
49	VSSD	VSSD	Power	
50	VDDD	VDDD	Power	
51	P5[0]	LED_G	Dgtl Out	Strong drive
52	P5[1]	GPIO [unused]		
53	P5[2]	\CapSense:Sns[1]\	Analog	HiZ analog
54	P5[3]	\CapSense:Sns[2]\	Analog	HiZ analog
55	P5[5]	\CapSense:Sns[0]\	Analog	HiZ analog
56	VDDA	VDDA	Power	
57	VSSA	VSSA	Power	
58	P1[0]	GPIO [unused]		
59	P1[1]	GPIO [unused]		
60	P1[2]	GPIO [unused]		
61	P1[3]	GPIO [unused]		
62	P1[4]	GPIO [unused]		
63	P1[5]	GPIO [unused]		
64	P1[6]	GPIO [unused]		

Abbreviations used in Table 3 have the following meanings:

- Dgtl In = Digital Input
- HiZ digital = High impedance digital
- Dgtl Out = Digital Output
- OD, DL = Open drain, drives low
- HiZ analog = High impedance analog

2.2 Hardware Ports

Table 4 contains information about the pins on this device in device port order. (No connection ["n/c"], power and dedicated pins have been omitted.)

Table 4. Device Ports

Port	Pin	Name	Type	Drive Mode
P0[0]	39	GPIO [unused]		
P0[1]	40	GPIO [unused]		
P0[2]	41	\CapSense:Sns[6]\	Analog	HiZ analog
P0[3]	42	\CapSense:Sns[7]\	Analog	HiZ analog
P0[4]	43	\CapSense:Sns[8]\	Analog	HiZ analog
P0[5]	44	\CapSense:Sns[5]\	Analog	HiZ analog
P0[6]	45	\CapSense:Sns[4]\	Analog	HiZ analog
P0[7]	46	\CapSense:Sns[3]\	Analog	HiZ analog
P1[0]	58	GPIO [unused]		
P1[1]	59	GPIO [unused]		
P1[2]	60	GPIO [unused]		
P1[3]	61	GPIO [unused]		
P1[4]	62	GPIO [unused]		
P1[5]	63	GPIO [unused]		
P1[6]	64	GPIO [unused]		
P1[7]	1	GPIO [unused]		
P2[0]	2	GPIO [unused]		
P2[1]	3	GPIO [unused]		
P2[2]	4	GPIO [unused]		
P2[3]	5	GPIO [unused]		
P2[4]	6	\UART:rx\	Dgtl In	HiZ digital
P2[5]	7	\UART:tx\	Dgtl Out	Strong drive
P2[6]	8	GPIO [unused]		
P2[7]	9	GPIO [unused]		
P3[0]	18	\EZI2C:scl\	Dgtl In	OD, DL
P3[1]	19	\EZI2C:sda\	Dgtl In	OD, DL
P3[2]	20	Debug:SWD_IO	Reserved	
P3[3]	21	Debug:SWD_CK	Reserved	
P3[4]	22	GPIO [unused]		
P3[5]	23	GPIO [unused]		
P3[6]	24	GPIO [unused]		
P3[7]	25	GPIO [unused]		
P4[0]	27	GPIO [unused]		
P4[1]	28	\CapSense:Cmod\	Analog	HiZ analog
P4[2]	29	GPIO [unused]		
P4[3]	30	GPIO [unused]		
P4[4]	31	GPIO [unused]		
P4[5]	32	GPIO [unused]		
P4[6]	33	GPIO [unused]		
P4[7]	34	GPIO [unused]		
P5[0]	51	LED_G	Dgtl Out	Strong drive
P5[1]	52	GPIO [unused]		
P5[2]	53	\CapSense:Sns[1]\	Analog	HiZ analog
P5[3]	54	\CapSense:Sns[2]\	Analog	HiZ analog
P5[5]	55	\CapSense:Sns[0]\	Analog	HiZ analog

Port	Pin	Name	Type	Drive Mode
P5[6]	35	LED_R	Dgtl Out	Strong drive
P5[7]	36	GPIO [unused]		
P6[0]	12	CAN_EN	Dgtl Out	Strong drive
P6[1]	13	CAN_RX	Dgtl In	HiZ digital
P6[2]	14	CAN_TX	Dgtl Out	Strong drive
P6[4]	15	CAN_STB	Software In/Out	Strong drive
P6[5]	16	CAN_ERR	Software In/Out	HiZ digital
P7[0]	37	LED_B	Dgtl Out	Strong drive
P7[1]	38	GPIO [unused]		

Abbreviations used in Table 4 have the following meanings:

- HiZ analog = High impedance analog
- Dgtl In = Digital Input
- HiZ digital = High impedance digital
- Dgtl Out = Digital Output
- OD, DL = Open drain, drives low

2.3 Software Pins

Table 5 contains information about the software pins on this device in alphabetical order. (Only software-accessible pins are shown.)

Table 5. Software Pins

Name	Port	Type
\CapSense:Cmod\	P4[1]	Analog
\CapSense:Sns[0]\	P5[5]	Analog
\CapSense:Sns[1]\	P5[2]	Analog
\CapSense:Sns[2]\	P5[3]	Analog
\CapSense:Sns[3]\	P0[7]	Analog
\CapSense:Sns[4]\	P0[6]	Analog
\CapSense:Sns[5]\	P0[5]	Analog
\CapSense:Sns[6]\	P0[2]	Analog
\CapSense:Sns[7]\	P0[3]	Analog
\CapSense:Sns[8]\	P0[4]	Analog
\EZI2C:scl\	P3[0]	Dgtl In
\EZI2C:sda\	P3[1]	Dgtl In
\UART:rx\	P2[4]	Dgtl In
\UART:tx\	P2[5]	Dgtl Out
CAN_EN	P6[0]	Dgtl Out
CAN_ERR	P6[5]	Software In/Out
CAN_RX	P6[1]	Dgtl In
CAN_STB	P6[4]	Software In/Out
CAN_TX	P6[2]	Dgtl Out
Debug:SWD_CK	P3[3]	Reserved
Debug:SWD_IO	P3[2]	Reserved
GPIO [unused]	P5[7]	
GPIO [unused]	P0[0]	
GPIO [unused]	P0[1]	
GPIO [unused]	P7[1]	
GPIO [unused]	P1[3]	
GPIO [unused]	P1[2]	
GPIO [unused]	P1[5]	
GPIO [unused]	P1[4]	
GPIO [unused]	P1[6]	
GPIO [unused]	P5[1]	
GPIO [unused]	P1[1]	
GPIO [unused]	P1[0]	
GPIO [unused]	P2[1]	
GPIO [unused]	P2[2]	
GPIO [unused]	P3[7]	
GPIO [unused]	P3[6]	
GPIO [unused]	P2[3]	
GPIO [unused]	P2[6]	
GPIO [unused]	P2[7]	
GPIO [unused]	P3[5]	
GPIO [unused]	P3[4]	
GPIO [unused]	P2[0]	
GPIO [unused]	P4[6]	

Name	Port	Type
GPIO [unused]	P4[5]	
GPIO [unused]	P1[7]	
GPIO [unused]	P4[7]	
GPIO [unused]	P4[2]	
GPIO [unused]	P4[0]	
GPIO [unused]	P4[3]	
GPIO [unused]	P4[4]	
LED_B	P7[0]	Dgtl Out
LED_G	P5[0]	Dgtl Out
LED_R	P5[6]	Dgtl Out

Abbreviations used in Table 5 have the following meanings:

- Dgtl In = Digital Input
- Dgtl Out = Digital Output

For more information on reading, writing and configuring pins, please refer to:

- Pins chapter in the System Reference Guide
  - CyPins API routines
- Programming Application Interface section in the cy_pins component datasheet

3 System Settings

3.1 System Configuration

Table 6. System Configuration Settings

Name	Value
Device Configuration Mode	Compressed
Unused Bonded IO	Disallowed
Heap Size (bytes)	0x80
Stack Size (bytes)	0x0800
Include CMSIS Core Peripheral Library Files	True

3.2 System Debug Settings

Table 7. System Debug Settings

Name	Value
Debug Select	SWD (serial wire debug)
Chip Protection	Open

3.3 System Operating Conditions

Table 8. System Operating Conditions

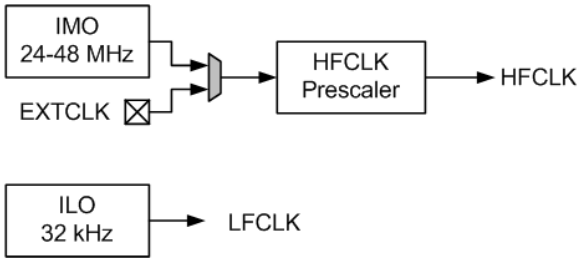
Name	Value
VDDA (V)	3.3
VDDD (V)	3.3
Variable VDDA	True

4 Clocks

The clock system includes these clock resources:

- Two internal clock sources:
  - 24 to 48 MHz Internal Main Oscillator (IMO) ±2% at all frequencies with trim
  - 32 kHz Internal Low Speed Oscillator (ILO)
- External clock (EXTCLK) generated using a signal from an I/O pin
- High-frequency clock (HFCLK) of up to 48 MHz selected from IMO or external clock
- Dedicated prescaler for HFCLK
- Low-frequency clock (LFCLK sourced by ILO
  - Dedicated prescaler for system clock (SYSCLK) of up to 48 MHz sourced by HFCLK
- 24 to 48 MHz Internal Main Oscillator (IMO) ±2%

Figure 3. System Clock Configuration



4.1 System Clocks

Table 9 lists the system clocks used in this design.

Table 9. System Clocks

Name	Domain	Source	Desired Freq	Nominal Freq	Accuracy (%)	Start at Reset	Enabled
SysClk	NONE	HFClk	? MHz	24 MHz	±2	True	True
PLL0_Sel	NONE	IMO	24 MHz	24 MHz	±2	True	True
HFClk	NONE	IMO	24 MHz	24 MHz	±2	True	True
IMO	NONE		24 MHz	24 MHz	±2	True	True
ILO	NONE		40 kHz	40 kHz	-50,+100	True	True
Timer_Sel	NONE	ILO	40 kHz	40 kHz	-50,+100	True	True
LFClk	NONE	ILO	? MHz	40 kHz	-50,+100	True	True
RTC_Sel	NONE	None	? MHz	? MHz	±0	True	True
Timer2	NONE	Timer_Sel	? MHz	? MHz	±0	False	False
Timer1	NONE	Timer_Sel	? MHz	? MHz	±0	False	False
ExtClk	NONE		16 MHz	? MHz	±0	False	False
Timer0	NONE	Timer_Sel	? MHz	? MHz	±0	False	False
PLL0	NONE	PLL0_Sel	24 MHz	? MHz	±0	False	False
ECO	NONE		24 MHz	? MHz	±0	False	False
Timer (WDT)	NONE	LFClk	? MHz	? MHz	±0	False	False
WCO	NONE		32.768 kHz	? MHz	±0.015	False	False

4.2 Local and Design Wide Clocks

Local clocks drive individual analog and digital blocks. Design wide clocks are a user-defined optimization, where two or more analog or digital blocks that share a common clock profile (frequency, etc) can be driven from the same clock divider output source.

Figure 4. Local and Design Wide Clock Configuration

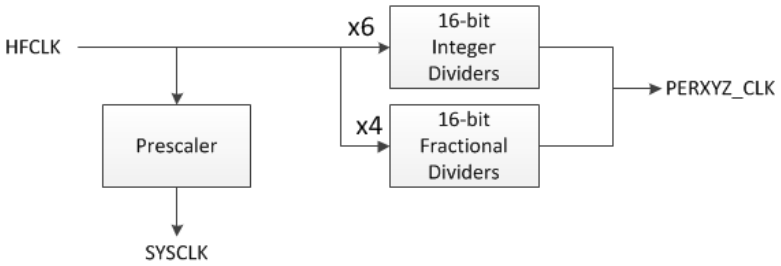


Table 10 lists the local clocks used in this design.

Table 10. Local Clocks

Name	Domain	Source	Desired Freq	Nominal Freq	Accuracy (%)	Start at Reset	Enabled
CAN_BUS_-HFCLK	NONE	HFClk	? MHz	24 MHz	±2	True	True
Clock_1	FIXED_-FUNCT-ION	HFClk	12 MHz	12 MHz	±2	True	True

Name	Domain	Source	Desired Freq	Nominal Freq	Accuracy (%)	Start at Reset	Enabled
EZI2C_-SCBCLK	FIXED_-FUNCT-ION	HFClk	1.55 MHz	1.6 MHz	±2	True	True
UART_SCBCLK	FIXED_-FUNCT-ION	HFClk	1.382 MHz	1.412 MHz	±2	True	True
CapSense_-ModClk	FIXED_-FUNCT-ION	HFClk	? MHz	94.118 kHz	±2	True	True

For more information on clocking resources, please refer to:

- Clocking System chapter in the PSoC 4 Technical Reference Manual
- Clocking chapter in the System Reference Guide
  - CySysClkImo API routines
  - CySysClkIlo API routines
  - CySysClkPll0 API routines
  - CySysClkEco API routines
  - CySysClkWco API routines
  - CySysClkWrite API routines

5 Interrupts

5.1 Interrupts

This design contains the following interrupt components: (0 is the highest priority)

Table 11. Interrupts

Name	Intr Num	Vector	Priority
EZI2C_SCB_IRQ	8	8	3
CapSense_ISR	16	16	3
Isr_TC_G	17	17	3
Isr_TC_B	21	21	3
Isr_TC_R	24	24	3
CAN_BUS_isr	26	26	3

For more information on interrupts, please refer to:

- Interrupt Controller chapter in the PSoC 4 Technical Reference Manual
- Interrupts chapter in the System Reference Guide
  - CyInt API routines and related registers
- Datasheet for cy_isr component

6 Flash Memory

PSoC 4 devices offer a host of Flash protection options and device security features that you can leverage to meet the security and protection requirements of an application. These requirements range from protecting configuration settings or Flash data to locking the entire device from external access.

Table 12 lists the Flash protection settings for your design.

Table 12. Flash Protection Settings

Start Address	End Address	Protection Level
0x0	0x1FFFF	U - Unprotected

Flash memory is organized as rows with each row of flash having 256 bytes. Each flash row can be assigned one of four protection levels:

- U - Unprotected
- W - Full Protection

For more information on Flash memory and protection, please refer to:

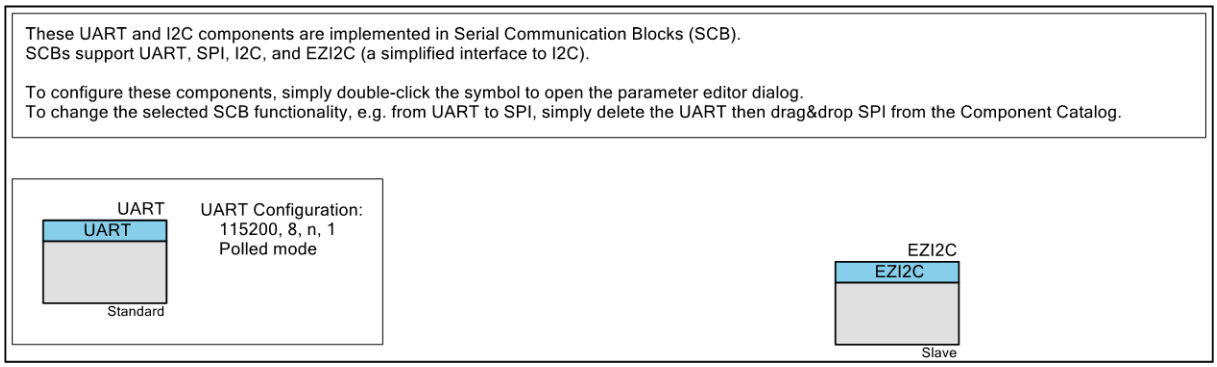
- Flash Protection chapter in the PSoC 4 Technical Reference Manual
- Flash and EEPROM chapter in the System Reference Guide
  - CySysFlash API routines

7 Design Contents

This design's schematic content consists of the following 4 schematic sheets:

7.1 Schematic Sheet: Communication

Figure 5. Schematic Sheet: Communication

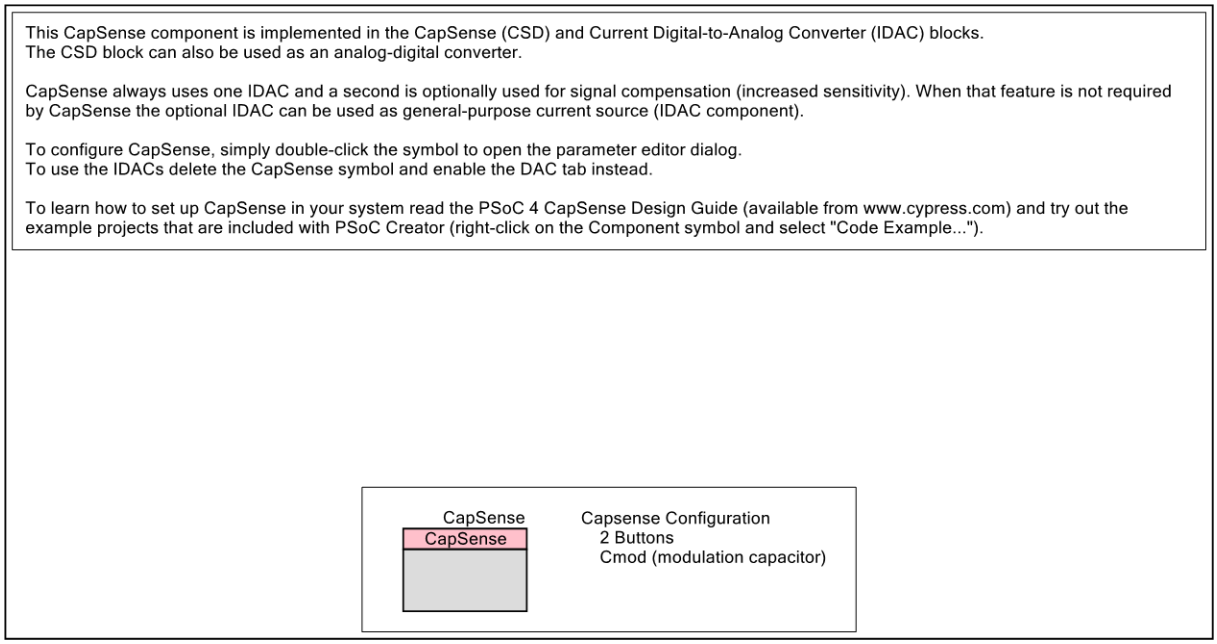


This schematic sheet contains the following component instances:

- Instance EZI2C (type: SCB_P4_v4_0)
- Instance UART (type: SCB_P4_v4_0)

7.2 Schematic Sheet: CapSense

Figure 6. Schematic Sheet: CapSense

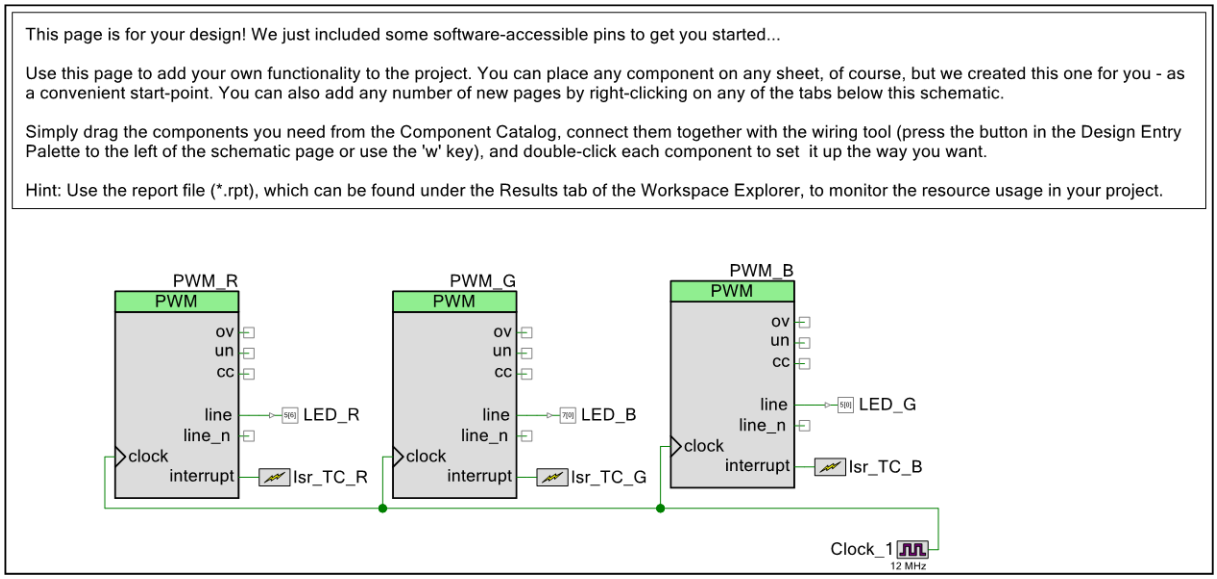


This schematic sheet contains the following component instances:

- Instance CapSense (type: CapSense_P4_v7_0)

7.3 Schematic Sheet: MyDesign

Figure 7. Schematic Sheet: MyDesign

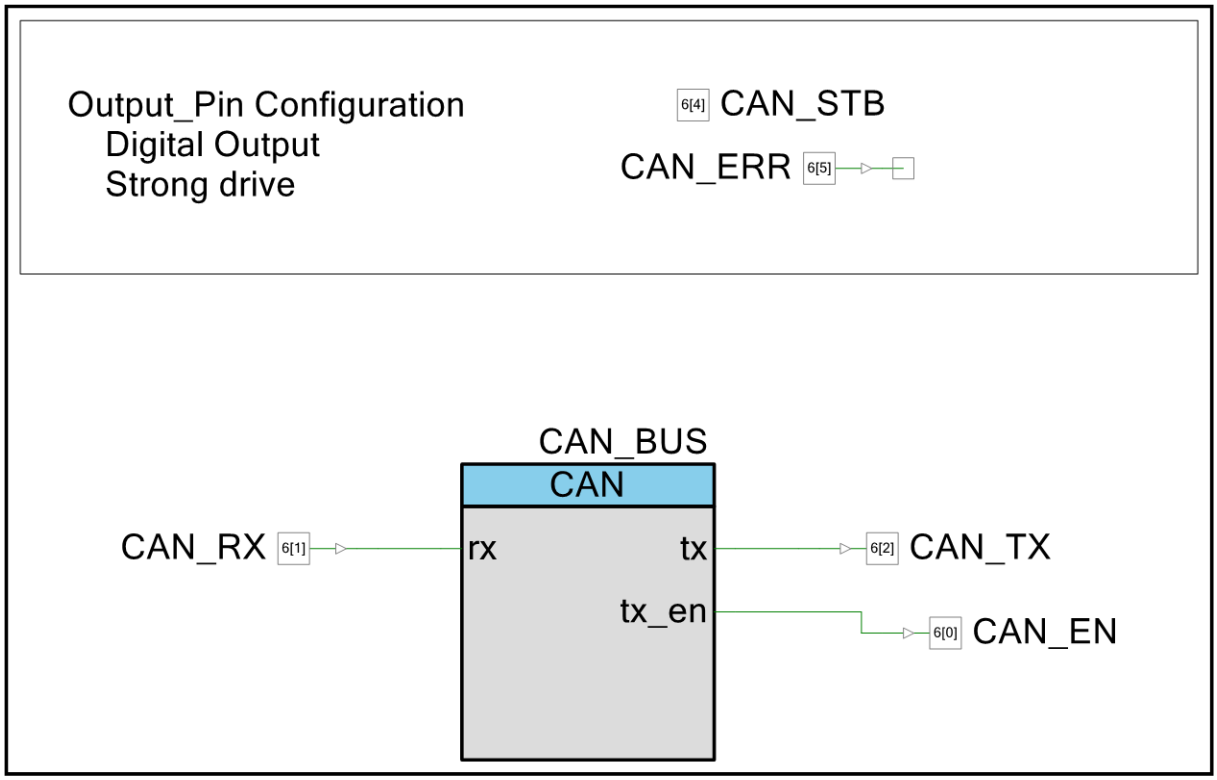


This schematic sheet contains the following component instances:

- Instance PWM_B (type: TCPWM_P4_v2_10)
- Instance PWM_G (type: TCPWM_P4_v2_10)
- Instance PWM_R (type: TCPWM_P4_v2_10)

7.4 Schematic Sheet: CAN

Figure 8. Schematic Sheet: CAN



This schematic sheet contains the following component instances:

- Instance CAN_BUS (type: CAN_v3_0)