Filter example project
2.0

Features

- FIR Low Pass filter with Rectangular window
- 128 Filter taps
- 1 kHz Cutoff Frequency
- DMA request is used as the Data ready signal

General Description

This example project demonstrates the operation of a Low Pass FIR Filter with Rectangular window.

Development kit configuration

1. This project is written for a 2X16 LCD display as there is one available in the Cypress kit CY8CKIT-001.
2. Build the project and program the hex file on to CY8C3866AXI-040 using MiniProg3.
3. Connect pins as described below and power cycle the device.
4. Observe the ADC output and also the filter input and output register values on LCD.
5. Observe the VDAC output as described below.

Project configuration

The example project consists of the Filter, ADC_DelSig, DMA, VDAC and Char LCD components. The top design schematic is shown in Figure 1. The Character LCD component is used for displaying the ADC output and also the filter input and output register values.

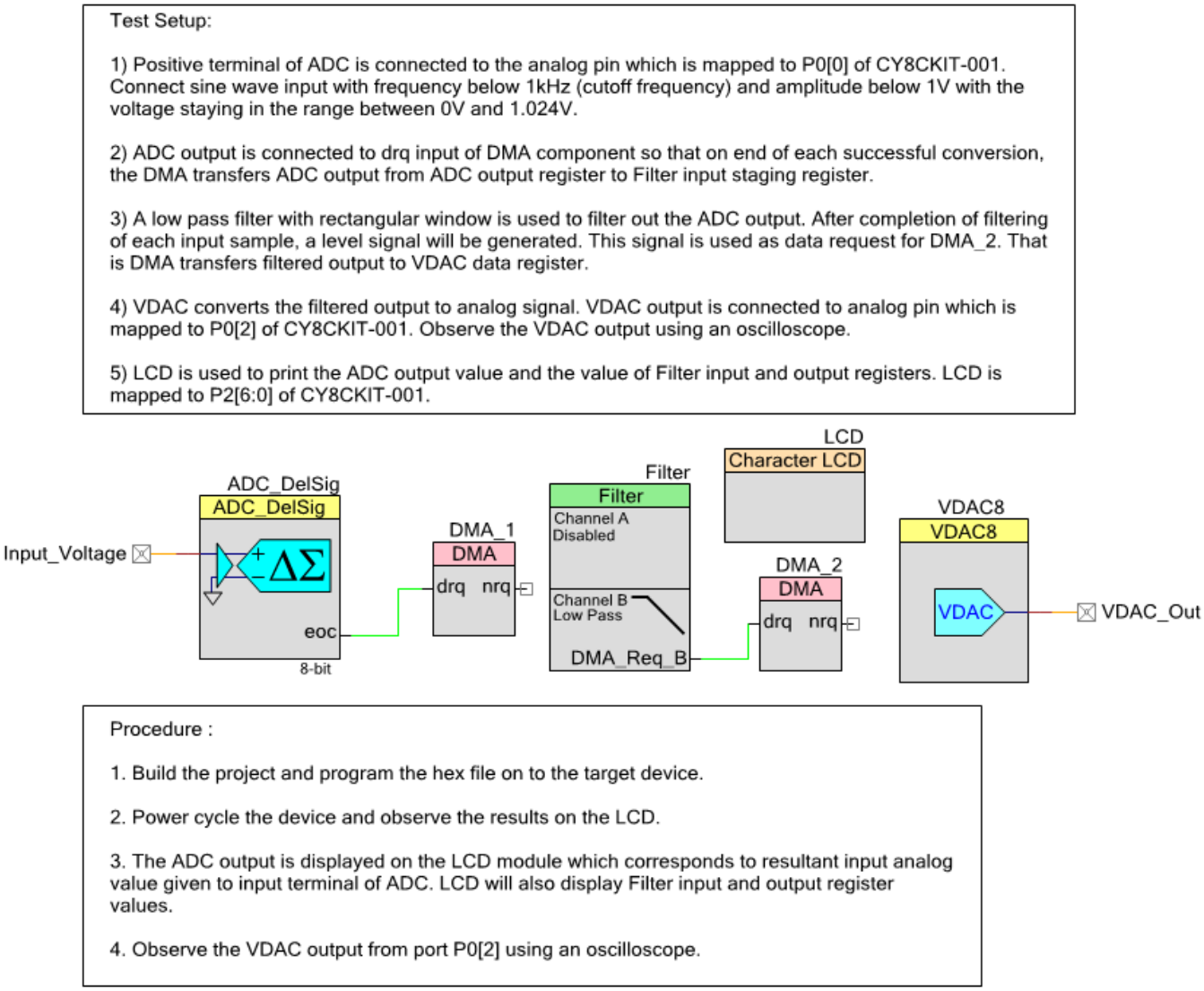

Figure 1. Top design schematic.

The Character LCD and VDAC uses the default configuration. The ADC is configured in the default single ended mode with Continuous conversion mode for 8-bit resolution. The DMA is configured to have the Level triggered hardware request signal. The Filter component is configured as shown below in figure 2.

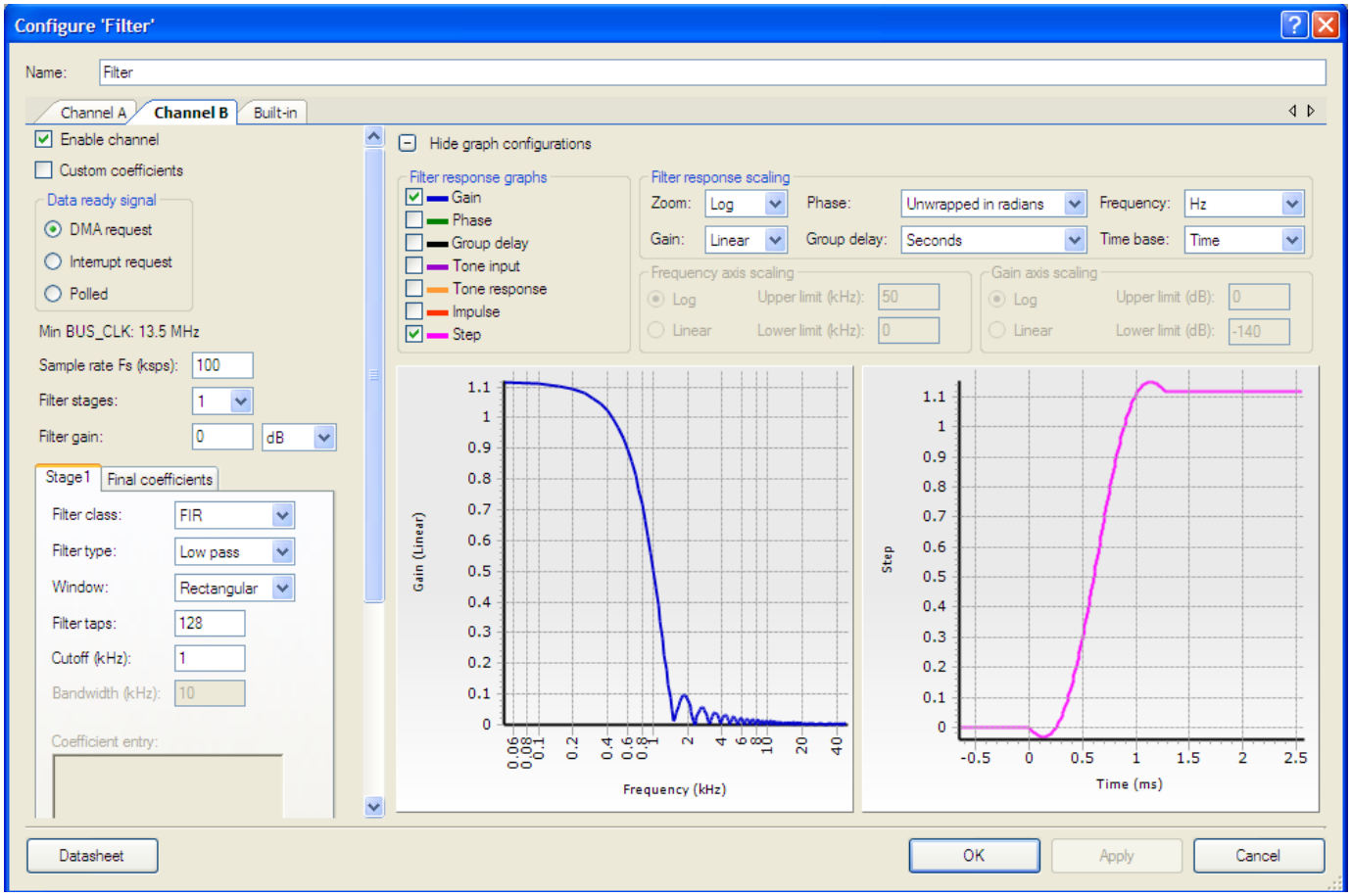

Figure 2. Filter Component Configuration.

Project description

In the main function all components are started. For the proper usage of Character LCD, VDAC, ADC_DelSig components, please refer to the corresponding component datasheets.

In this project, ADC output is given as the input sample to the low pass FIR filter. Connections are mad as explained in the Figure 1 above. ADC component converts input analog voltage given to its +ve terminal. On each successful conversion, DMA_1 transfers the ADC output to Filter input register. Filtered output is stored in the Filter output register. Filter generates data ready signal on filtering each of the input samples. This data ready signal is used to transfer the filtered output to VDAC data register using DMA_2. LCD is used in this project to display the ADC output and Filter input and output register values.

Expected Results

The sine wave observed on the output terminal of the VDAC should be equal in amplitude and frequency to the sine wave given to the input terminal of ADC component.