

Filter example project

2.0

Features

- FIR Low Pass filter with Rectangular window
- 128 Filter taps
- 1 kHz Cutoff Frequency
- DMA request is used as the Data ready signal

General Description

This example project demonstrates the operation of a Low Pass FIR Filter with Rectangular window.

Development kit configuration

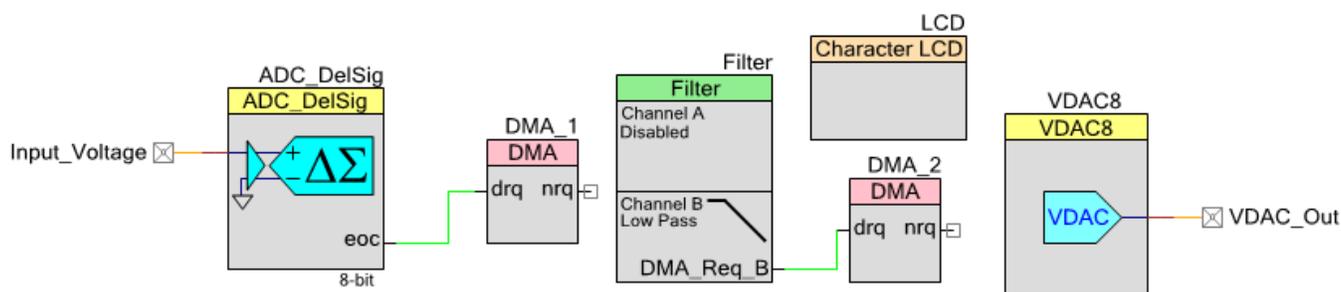
1. This project is written for a 2X16 LCD display as there is one available in the Cypress kit CY8CKIT-001.
2. Build the project and program the hex file on to CY8C3866AXI-040 using MiniProg3.
3. Connect pins as described below and power cycle the device.
4. Observe the ADC output and also the filter input and output register values on LCD.
5. Observe the VDAC output as described below.

Project configuration

The example project consists of the Filter, ADC_DeISig, DMA, VDAC and Char LCD components. The top design schematic is shown in Figure 1. The Character LCD component is used for displaying the ADC output and also the filter input and output register values.

Test Setup:

- 1) Positive terminal of ADC is connected to the analog pin which is mapped to P0[0] of CY8CKIT-001. Connect sine wave input with frequency below 1kHz (cutoff frequency) and amplitude below 1V with the voltage staying in the range between 0V and 1.024V.
- 2) ADC output is connected to drq input of DMA component so that on end of each successful conversion, the DMA transfers ADC output from ADC output register to Filter input staging register.
- 3) A low pass filter with rectangular window is used to filter out the ADC output. After completion of filtering of each input sample, a level signal will be generated. This signal is used as data request for DMA_2. That is DMA transfers filtered output to VDAC data register.
- 4) VDAC converts the filtered output to analog signal. VDAC output is connected to analog pin which is mapped to P0[2] of CY8CKIT-001. Observe the VDAC output using an oscilloscope.
- 5) LCD is used to print the ADC output value and the value of Filter input and output registers. LCD is mapped to P2[6:0] of CY8CKIT-001.

**Procedure :**

1. Build the project and program the hex file on to the target device.
2. Power cycle the device and observe the results on the LCD.
3. The ADC output is displayed on the LCD module which corresponds to resultant input analog value given to input terminal of ADC. LCD will also display Filter input and output register values.
4. Observe the VDAC output from port P0[2] using an oscilloscope.

Figure 1. Top design schematic.

The Character LCD and VDAC uses the default configuration. The ADC is configured in the default single ended mode with Continuous conversion mode for 8-bit resolution. The DMA is configured to have the Level triggered hardware request signal. The Filter component is configured as shown below in figure 2.

Expected Results

The sine wave observed on the output terminal of the VDAC should be equal in amplitude and frequency to the sine wave given to the input terminal of ADC component.

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