

Filter_ADC_VDAC Example Project

1.10

Features

- FIR low-pass filter at 6 kHz with Blackman window, 85 taps
- AC-coupled input provided bias with internal Opamp for maximum swing
- DMA used to transfer ADC result to Filter
- VDAC used to display output

General Description

This example project is also a PSoC Creator starter design. It demonstrates PSoC's unique capability of leveraging the Digital Filter Block (DFB) to filter an analog input all in hardware. It also provides all the DMA setup to transfer data from the ADC directly to the DFB, bypassing the processor. PSoC allows you to implement a filter without having to write CPU-intensive algorithms in firmware.

This project demonstrates the operation of a Low Pass FIR Filter with Blackman window. By changing only a few input parameters in the Filter customizer, you can experiment with a wide variety of FIR and IIR filters.

Development Kit Configuration

The following configuration instructions provide a guideline to test this design. For simplicity, the instructions describe the stepwise process to be followed when testing this design with the PSoC Development Kit (CY8CKIT-001) board, but can be generalized for the PSoC 3 Development Kit (CY8CKIT-030) and PSoC 5 Development Kit (CY8CKIT-050) as well.

1. Set SW3 to 5V and leave the rest of the board at default configuration. This ensures $V_{dda}=V_{ddd}=5V$.
2. Set up the passives used in the schematic as shown in Figure 1.
3. Ensure that the Function generator input has a peak-to-peak amplitude of 4V or less.
4. Build the Filter_ADC_VDAC project and then program the hex file onto the PSoC device using the MiniProg3. After programming is complete, disconnect the MiniProg3.
5. Reset the PSoC device.

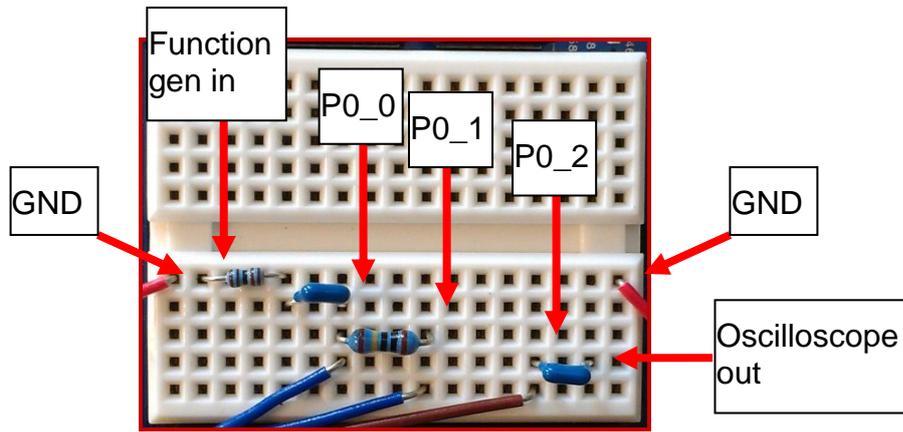


Figure 1. Breadboard setup

Project Configuration

The top design schematic for this project is shown in Figure 2.

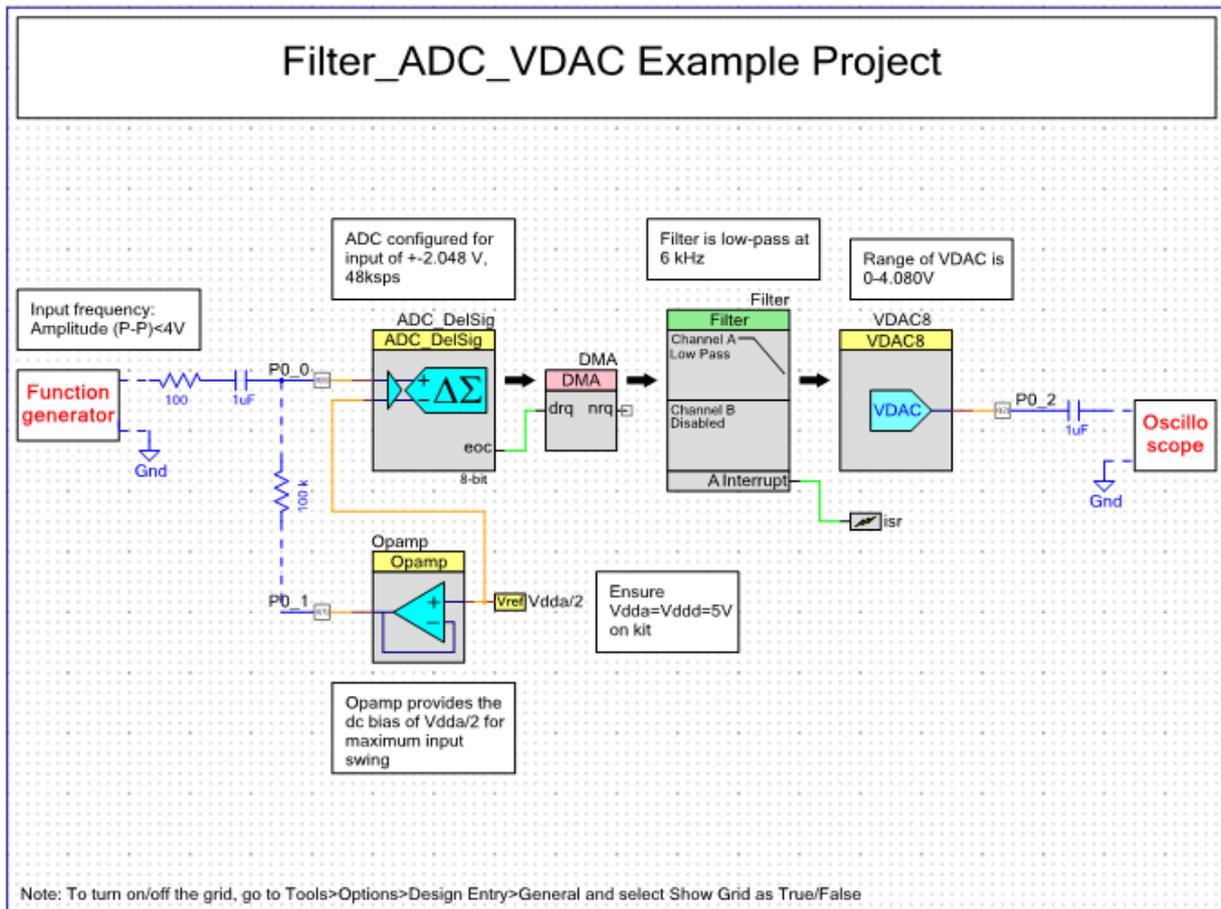


Figure 2. TopDesign Schematic

The ADC_DeISig component configuration window is shown below in Figure 3. The Opamp is simply configured in follower mode, so that its output voltage is equal to Vdda/2. The DMA is

configured using the DMA wizard to transfer one byte from the ADC output register to the Filter channel A input register on each rising edge of the ADC EOC signal.

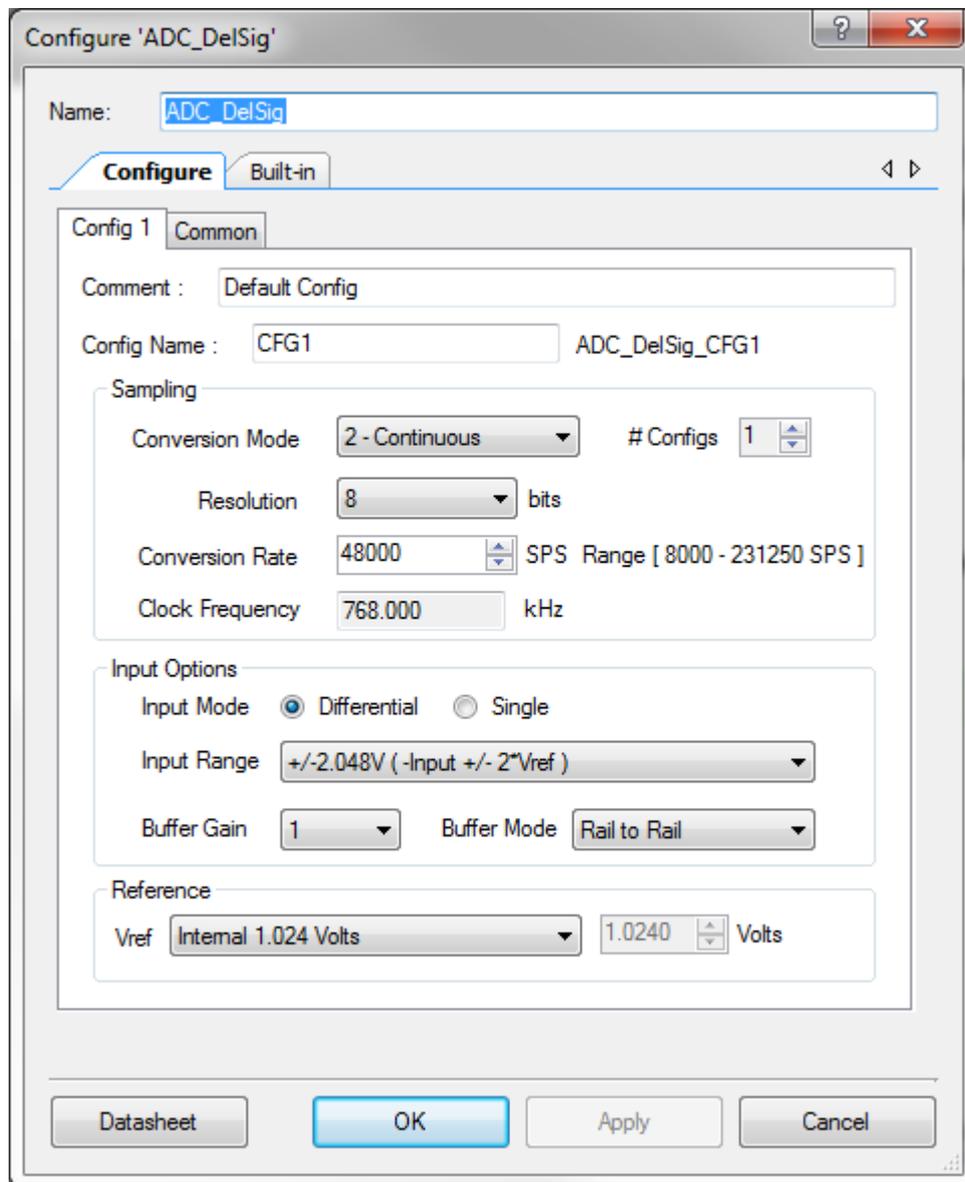


Figure 3. ADC_DeISig Component Configuration

The Filter sample rate is set to be same as the sample rate on the ADC – 48 ksp. Data ready signal is set to be ISR, and the rest of the parameters which configure the Filter response are as shown in Figure 4. Notably, the filter is a single stage, FIR, low-pass filter with a cutoff of 6 kHz. By changing these parameters, you can easily create a Filter of your choice.

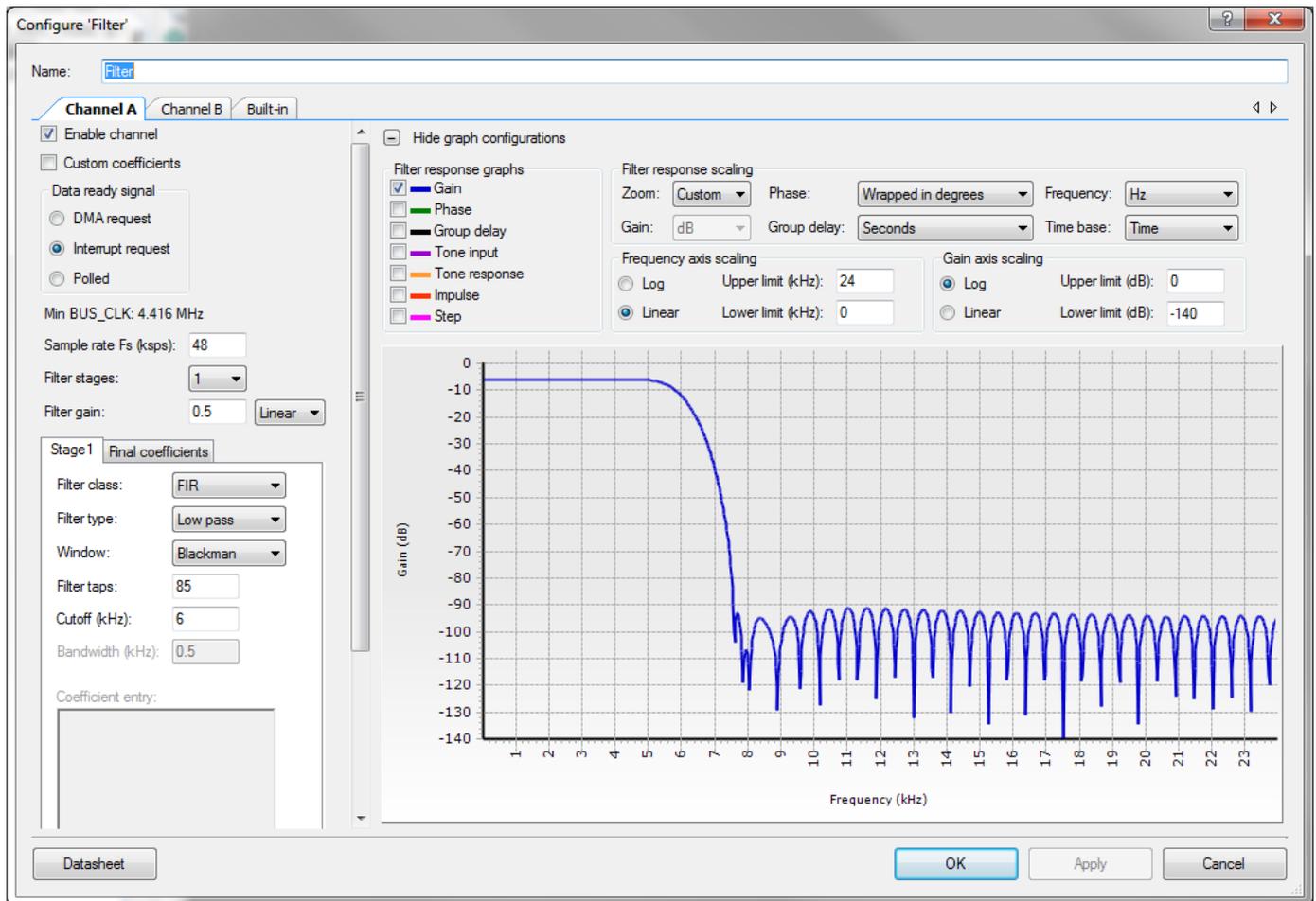


Figure 4. Filter configuration window

The VDAC is configured for an output range of 0-4.080V for the sake of easily verifying the output.

Project Description

The code required for this project is surprisingly simple. In the main function all components are started. The DMA is configured to transfer the ADC output to the input data register of the Filter's channel A. Finally, global interrupts are enabled. Note that there is no code in the 'forever' loop.

Each time the ADC completes a conversion, it triggers the DMA to transfer the converted data to the Filter. The Filter in turn, processes this sample and sets off the interrupt when the processing is complete. Since the VDAC can take in only positive data, the Filter channel A output is converted into an unsigned form and then written to the VDAC data register. The Filtered result can then be verified by observing the VDAC output.

Expected Results

The VDAC output should behave as a low-pass filtered output with cut-off at 6 kHz.

Related Material

Example Projects

- [ADC_DMA_VDAC](#)

Application Notes

- [AN2099 - PSoC® 1, PSoC 3, and PSoC 5 - Single-Pole Infinite Impulse Response \(IIR\) Filters](#)
- [AN52705 - PSoC® 3 and PSoC 5 - Getting Started with DMA](#)
- [AN61102 - PSoC® 3 and PSoC 5 - ADC Data Buffering Using DMA](#)
- [AN57821- PSoC® 3 and PSoC 5 Mixed Signal Circuit Board Layout Considerations](#)

Training

- [PSoC 3 and PSoC 5 104: Introduction to Analog Peripherals](#)



Cypress Semiconductor
198 Champion Court
San Jose, CA 95134-1709

Phone : 408-943-2600
Fax : 408-943-4730
Website : www.cypress.com

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