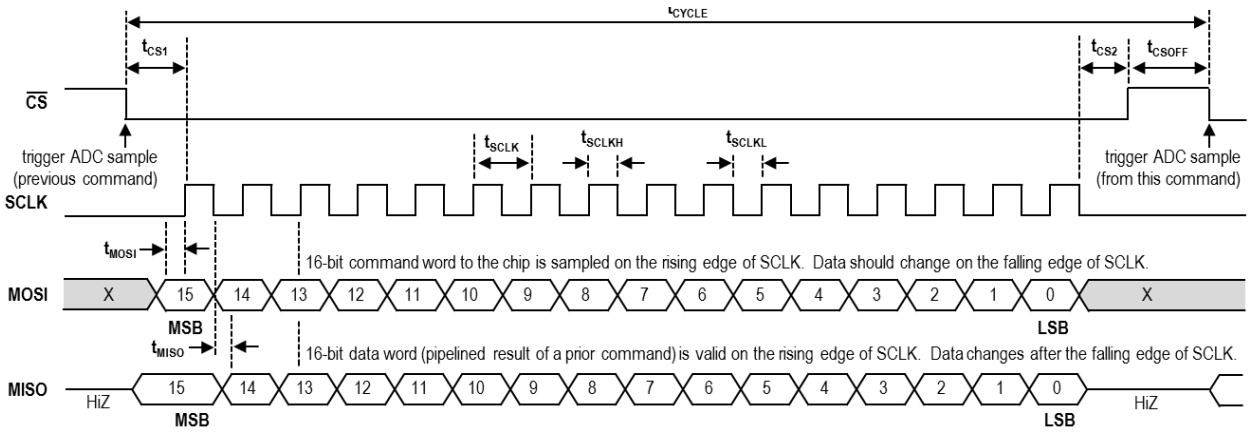
SPI Bus Signals

RHD2000 chips communicate using a standard SPI interface consisting of four signals: an active-low chip select ($\overline{CS}$); a serial data clock (SCLK) with a base value of zero; a "Master Out, Slave In" data line (MOSI) to receive commands from the master device; and a "Master In, Slave Out" data line (MISO) to send pipelined results from prior commands to the master device. The RHD2000 chip always functions as the SPI slave device. During each chip select cycle, 16-bit data words are transferred in each direction, MSB first. As shown below, the RHD2000 samples MOSI on the rising edge of SCLK. The master should sample MISO on the rising edge of SCLK. (The master device SPI interface should be configured with SPI options CPOL=0 and CPHA=0.) The RHD2000 ADC samples the selected analog signal on the falling edge of $\overline{CS}$. The $\overline{CS}$ line must be pulsed high between every 16-bit data transfer, even when the command word does not request an analog-to-digital conversion.

Timing Diagram



SPI BUS TIMING SPECIFICATIONS

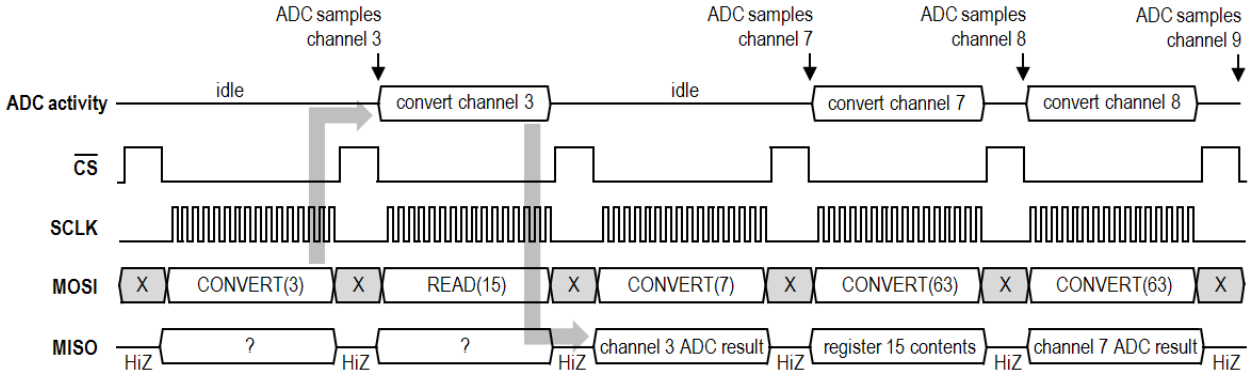
T_A = 25ºC, V_{DD} = 3.3V unless otherwise noted.

SYMBOL	PARAMETER	MIN	MAX	UNIT	COMMENTS
t_{SCLK}	SCLK Period	41.6		ns	Maximum SCLK frequency is 24 MHz
t_{SCLKH}	SCLK Pulse Width High	20.8		ns	
t_{SCLKL}	SCLK Pulse Width Low	20.8		ns	
t_{CS1}	$\overline{CS}$ Low to SCLK High Setup	20.8		ns	
t_{CS2}	SCLK Low to $\overline{CS}$ High Setup	20.8		ns	
t_{CSOFF}	$\overline{CS}$ High Duration	154		ns	
t_{MOSI}	MOSI Data Valid to SCLK High Setup	10.4		ns	
t_{MISO}	SCLK or $\overline{CS}$ Falling Edge to MISO Data Valid		12	ns	
t_{CYCLE}	Total Cycle Time Between ADC Samples	950		ns	Maximum sample rate is 1.05 MS/s, or 30 kS/s per channel for 35 multiplexed channels.

SPI Command Words

Each RHD2000 chip responds to five basic commands: perform an analog-to-digital conversion on a particular signal; run an ADC self-calibration routine; clear ADC calibration; write to a RAM register; or read from a RAM or ROM register. Each chip contains 18 eight-bit RAM registers that configure various aspects of chip behavior and several eight-bit ROM registers that store basic properties of the chip.

The RHD2000 uses a pipelined communication protocol; each command sent over the MOSI line generates a 16-bit result that is transmitted over the MISO line two commands later. Communication with the chip is illustrated in the following example diagram:



After receiving a CONVERT(C) command, the on-chip ADC samples channel C on the falling edge of the next $\overline{CS}$ pulse. The analog-to-digital conversion is performed during the next 16 SCLK cycles, and the result is relayed to the master over the MISO line during the following 16 SCLK cycles.

The RHD2000 commands are described by the following bit patterns:

Command: CONVERT(C) – Run analog-to-digital conversion on channel C

MSB 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	LSB 0
0	**0**	**C[5]**	**C[4]**	**C[3]**	**C[2]**	**C[1]**	**C[0]**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**H**

Result:

MSB 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	LSB 0
A[15]	**A[14]**	**A[13]**	**A[12]**	**A[11]**	**A[10]**	**A[9]**	**A[8]**	**A[7]**	**A[6]**	**A[5]**	**A[4]**	**A[3]**	**A[2]**	**A[1]**	**A[0]**

Comments:

The CONVERT(C) command executes an analog-to-digital conversion of analog channel C. Channels 0-31 correspond to the 32 biopotential amplifiers sharing the chip with the ADC. (Only channels 0-15 are active in the RHD2216.) A subset of channels 32-62 are used for auxiliary sensors on and off the chip (see later sections). The conversion result A is sent back to the master (MSB first) two commands later, as shown in the figure above.

A special case of the CONVERT command with C = 63 can be used to cycle through successive amplifier channels. The CONVERT(63) command automatically increments the multiplexer to the next amplifier channel. After reaching the end of the amplifier array, the multiplexer rolls back to channel 0. (Note: The state of the chip is undefined at power-up, so at least one CONVERT(0) command should be sent before executing this variant of the command.)

If the LSB (bit H) of a CONVERT(C) command is set to 1 when DSP offset removal is enabled (see "DSP High-Pass Filter for Offset Removal" section), then the output of the digital high-pass filter associated with amplifier channel C is reset to zero. This can be used to rapidly recover from a large transient and settle to baseline.