PSoC® Creator™
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1 Overview

The Cypress PSoC 5 is a family of 32-bit devices with the following characteristics:

- High-performance 32-bit ARM Cortex-M3 core with a nested vectored interrupt controller (NVIC) and a high-performance DMA controller
- Digital system that includes configurable Universal Digital Blocks (UDBs) and specific function peripherals, such as USB, I2C and SPI
- Analog subsystem that includes 20-bit Delta Sigma converters (ADC), SAR ADCs, 8-bit DACs that can be configured for 12-bit operation, comparators, op amps and configurable switched capacitor (SC) and continuous time (CT) blocks to create PGAs, TIAs, mixers, and more
- Several types of memory elements, including SRAM, flash, and EEPROM
- Programming and debug system through JTAG, serial wire debug (SWD), and single wire viewer (SWV)
- Flexible routing to all pins

Figure 1 shows the major components of a typical CY8C54LP series member PSoC 5LP device. For details on all the systems listed above, please refer to the PSoC 5LP Technical Reference Manual.

Figure 1. CY8C54LP Device Series Block Diagram

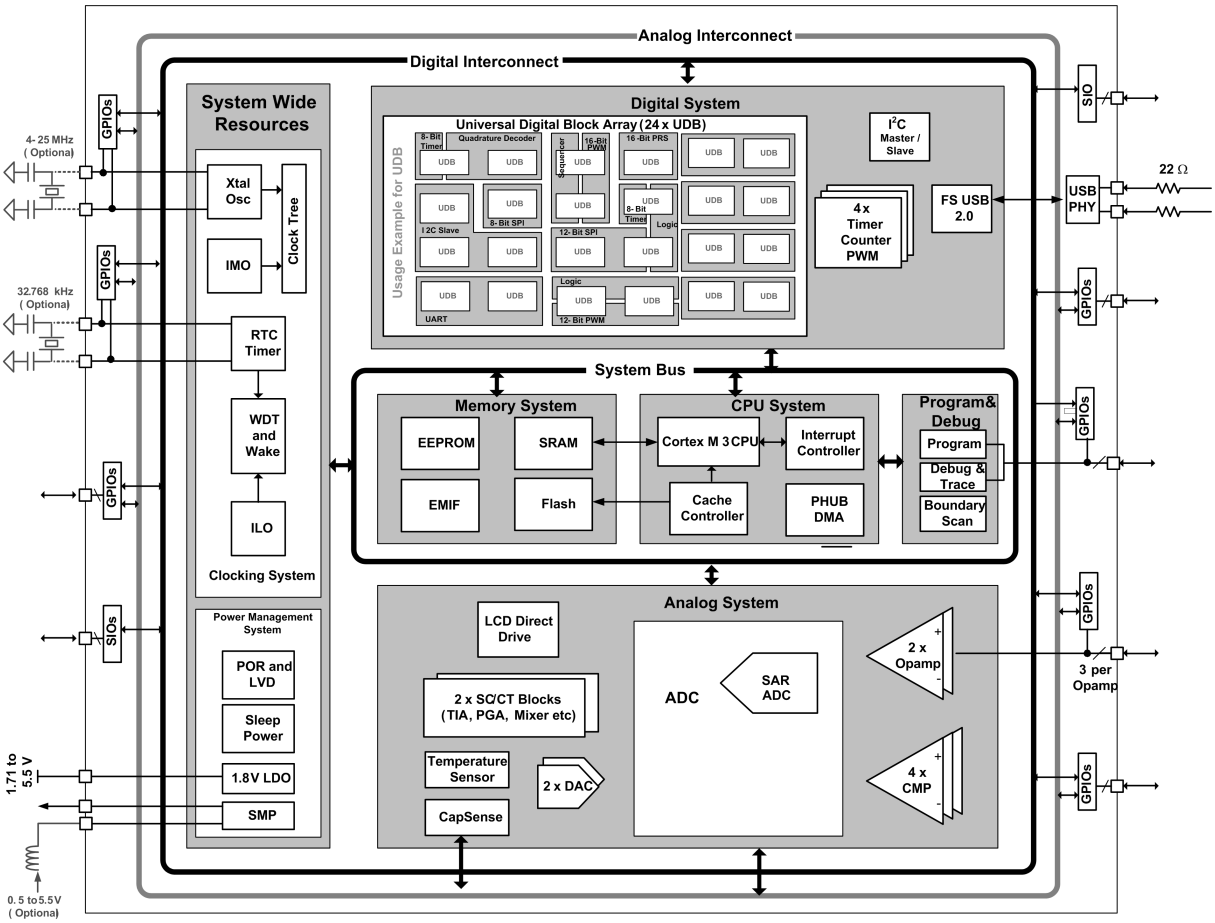


Table 1 lists the key characteristics of this device.

Table 1. Device Characteristics

Name	Value
Part Number	CY8C5468AXI-LP042
Package Name	100-TQFP
Family	PSoC 5LP
Series	CY8C54LP
Max CPU speed (MHz)	0
Flash size (kB)	256
SRAM size (kB)	64
EEPROM size (bytes)	2048
Vdd range (V)	1.71 to 5.5
Automotive qualified	No (Industrial Grade Only)
Temp range (Celsius)	-40 to 85
JTAG ID	0x2E12A069

NOTE: The CPU speed noted above is the maximum available speed. The CPU is clocked by Bus Clock, listed in the System Clocks section below.

Table 2 lists the device resources that this design uses:

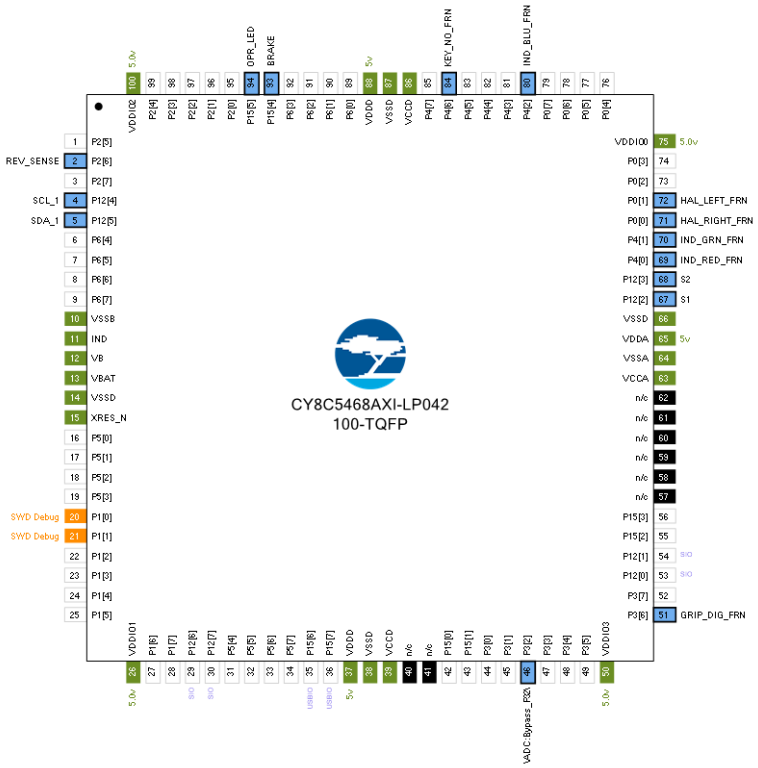
Table 2. Device Resources

Resource Type	Used	Free	Max	% Used
Digital Clocks	3	5	8	37.50 %
Analog Clocks	2	2	4	50.00 %
CapSense Buffers	0	2	2	0.00 %
Interrupts	4	28	32	12.50 %
IO	17	55	72	23.61 %
Segment LCD	0	1	1	0.00 %
I2C	0	1	1	0.00 %
USB	0	1	1	0.00 %
DMA Channels	0	24	24	0.00 %
Timer	0	4	4	0.00 %
UDB				
Macrocells	31	161	192	16.15 %
Unique P-terms	47	337	384	12.24 %
Total P-terms	59			
Datapath Cells	15	9	24	62.50 %
Status Cells	6	18	24	25.00 %
StatusI Registers	5			
Routed Count7 Load/Enable	1			
Control Cells	4	20	24	16.67 %
Control Registers	3			
Count7 Cells	1			
Opamp	0	2	2	0.00 %
Comparator	0	4	4	0.00 %
Delta-Sigma ADC	1	0	1	100.00 %
LPF	0	2	2	0.00 %
Analog (SC/CT) Blocks	0	2	2	0.00 %
DAC				
VIDAC	0	2	2	0.00 %

2 Pins

Figure 2 shows the pin layout of this device.

Figure 2. Device Pin Layout



2.1 Hardware Pins

Table 3 contains information about the pins on this device in device pin order. (No connection ["n/c"] pins have been omitted.)

Table 3. Device Pins

Pin	Port	Name	Type	Drive Mode	Reset State
1	P2[5]	GPIO [unused]			HiZ Analog Unb
2	P2[6]	REV_SENSE	Software In/Out	Strong drive	HiZ Analog Unb
3	P2[7]	GPIO [unused]			HiZ Analog Unb
4	P12[4]	SCL_1	Software In/Out	OD, DL	HiZ Analog Unb
5	P12[5]	SDA_1	Software In/Out	OD, DL	HiZ Analog Unb
6	P6[4]	GPIO [unused]			HiZ Analog Unb
7	P6[5]	GPIO [unused]			HiZ Analog Unb
8	P6[6]	GPIO [unused]			HiZ Analog Unb
9	P6[7]	GPIO [unused]			HiZ Analog Unb
10	VSSB	VSSB	Dedicated		
11	IND	IND	Dedicated		
12	VB	VB	Dedicated		
13	VBAT	VBAT	Dedicated		
14	VSSD	VSSD	Power		
15	XRES_N	XRES_N	Dedicated		
16	P5[0]	GPIO [unused]			HiZ Analog Unb
17	P5[1]	GPIO [unused]			HiZ Analog Unb
18	P5[2]	GPIO [unused]			HiZ Analog Unb
19	P5[3]	GPIO [unused]			HiZ Analog Unb
20	P1[0]	Debug:SWD_IO	Reserved		
21	P1[1]	Debug:SWD_CK	Reserved		
22	P1[2]	GPIO [unused]			HiZ Analog Unb
23	P1[3]	GPIO [unused]			HiZ Analog Unb
24	P1[4]	GPIO [unused]			HiZ Analog Unb
25	P1[5]	GPIO [unused]			HiZ Analog Unb
26	VDDIO1	VDDIO1	Power		
27	P1[6]	GPIO [unused]			HiZ Analog Unb
28	P1[7]	GPIO [unused]			HiZ Analog Unb
29	P12[6]	SIO [unused]			HiZ Analog Unb
30	P12[7]	SIO [unused]			HiZ Analog Unb
31	P5[4]	GPIO [unused]			HiZ Analog Unb
32	P5[5]	GPIO [unused]			HiZ Analog Unb
33	P5[6]	GPIO [unused]			HiZ Analog Unb
34	P5[7]	GPIO [unused]			HiZ Analog Unb
35	P15[6]	USB IO [unused]			HiZ Analog Unb
36	P15[7]	USB IO [unused]			HiZ Analog Unb
37	VDDD	VDDD	Power		
38	VSSD	VSSD	Power		
39	VCCD	VCCD	Power		
42	P15[0]	GPIO [unused]			HiZ Analog Unb
43	P15[1]	GPIO [unused]			HiZ Analog Unb
44	P3[0]	GPIO [unused]			HiZ Analog Unb
45	P3[1]	GPIO [unused]			HiZ Analog Unb

Pin	Port	Name	Type	Drive Mode	Reset State
46	P3[2]	\ADC:Bypass_P32\	Analog	HiZ analog	HiZ Analog Unb
47	P3[3]	GPIO [unused]			HiZ Analog Unb
48	P3[4]	GPIO [unused]			HiZ Analog Unb
49	P3[5]	GPIO [unused]			HiZ Analog Unb
50	VDDIO3	VDDIO3	Power		
51	P3[6]	GRIP_DIG_FRN	Software In/Out	Res pull up	HiZ Analog Unb
52	P3[7]	GPIO [unused]			HiZ Analog Unb
53	P12[0]	SIO [unused]			HiZ Analog Unb
54	P12[1]	SIO [unused]			HiZ Analog Unb
55	P15[2]	GPIO [unused]			HiZ Analog Unb
56	P15[3]	GPIO [unused]			HiZ Analog Unb
63	VCCA	VCCA	Power		
64	VSSA	VSSA	Power		
65	VDDA	VDDA	Power		
66	VSSD	VSSD	Power		
67	P12[2]	S1	Dgtl Out	Strong drive	HiZ Analog Unb
68	P12[3]	S2	Dgtl In	HiZ digital	HiZ Analog Unb
69	P4[0]	IND_RED_FRN	Software In/Out	Open drain, drives high	HiZ Analog Unb
70	P4[1]	IND_GRN_FRN	Software In/Out	Open drain, drives high	HiZ Analog Unb
71	P0[0]	HAL_RIGHT_FRN	Analog	HiZ analog	HiZ Analog Unb
72	P0[1]	HAL_LEFT_FRN	Analog	HiZ analog	HiZ Analog Unb
73	P0[2]	GPIO [unused]			HiZ Analog Unb
74	P0[3]	GPIO [unused]			HiZ Analog Unb
75	VDDIO0	VDDIO0	Power		
76	P0[4]	GPIO [unused]			HiZ Analog Unb
77	P0[5]	GPIO [unused]			HiZ Analog Unb
78	P0[6]	GPIO [unused]			HiZ Analog Unb
79	P0[7]	GPIO [unused]			HiZ Analog Unb
80	P4[2]	IND_BLU_FRN	Software In/Out	Open drain, drives high	HiZ Analog Unb
81	P4[3]	GPIO [unused]			HiZ Analog Unb
82	P4[4]	GPIO [unused]			HiZ Analog Unb
83	P4[5]	GPIO [unused]			HiZ Analog Unb
84	P4[6]	KEY_NO_FRN	Software In/Out	Res pull up	HiZ Analog Unb
85	P4[7]	GPIO [unused]			HiZ Analog Unb
86	VCCD	VCCD	Power		
87	VSSD	VSSD	Power		
88	VDDD	VDDD	Power		
89	P6[0]	GPIO [unused]			HiZ Analog Unb
90	P6[1]	GPIO [unused]			HiZ Analog Unb
91	P6[2]	GPIO [unused]			HiZ Analog Unb
92	P6[3]	GPIO [unused]			HiZ Analog Unb
93	P15[4]	BRAKE	Software In/Out	Strong drive	HiZ Analog Unb
94	P15[5]	OPR_LED	Software In/Out	Strong drive	HiZ Analog Unb
95	P2[0]	GPIO [unused]			HiZ Analog Unb
96	P2[1]	GPIO [unused]			HiZ Analog Unb
97	P2[2]	GPIO [unused]			HiZ Analog Unb
98	P2[3]	GPIO [unused]			HiZ Analog Unb

Pin	Port	Name	Type	Drive Mode	Reset State
99	P2[4]	GPIO [unused]			HiZ Analog Unb
100	VDDIO2	VDDIO2	Power		

Abbreviations used in Table 3 have the following meanings:

- HiZ Analog Unb = Hi-Z Analog Unbuffered
- OD, DL = Open drain, drives low
- HiZ analog = High impedance analog
- Res pull up = Resistive pull up
- Dgtl Out = Digital Output
- Dgtl In = Digital Input
- HiZ digital = High impedance digital

2.2 Hardware Ports

Table 4 contains information about the pins on this device in device port order. (No connection ["n/c"], power and dedicated pins have been omitted.)

Table 4. Device Ports

Port	Pin	Name	Type	Drive Mode	Reset State
P0[0]	71	HAL_RIGHT_FRN	Analog	HiZ analog	HiZ Analog Unb
P0[1]	72	HAL_LEFT_FRN	Analog	HiZ analog	HiZ Analog Unb
P0[2]	73	GPIO [unused]			HiZ Analog Unb
P0[3]	74	GPIO [unused]			HiZ Analog Unb
P0[4]	76	GPIO [unused]			HiZ Analog Unb
P0[5]	77	GPIO [unused]			HiZ Analog Unb
P0[6]	78	GPIO [unused]			HiZ Analog Unb
P0[7]	79	GPIO [unused]			HiZ Analog Unb
P1[0]	20	Debug:SWD_IO	Reserved		
P1[1]	21	Debug:SWD_CK	Reserved		
P1[2]	22	GPIO [unused]			HiZ Analog Unb
P1[3]	23	GPIO [unused]			HiZ Analog Unb
P1[4]	24	GPIO [unused]			HiZ Analog Unb
P1[5]	25	GPIO [unused]			HiZ Analog Unb
P1[6]	27	GPIO [unused]			HiZ Analog Unb
P1[7]	28	GPIO [unused]			HiZ Analog Unb
P12[0]	53	SIO [unused]			HiZ Analog Unb
P12[1]	54	SIO [unused]			HiZ Analog Unb
P12[2]	67	S1	Dgtl Out	Strong drive	HiZ Analog Unb
P12[3]	68	S2	Dgtl In	HiZ digital	HiZ Analog Unb
P12[4]	4	SCL_1	Software In/Out	OD, DL	HiZ Analog Unb
P12[5]	5	SDA_1	Software In/Out	OD, DL	HiZ Analog Unb
P12[6]	29	SIO [unused]			HiZ Analog Unb
P12[7]	30	SIO [unused]			HiZ Analog Unb
P15[0]	42	GPIO [unused]			HiZ Analog Unb
P15[1]	43	GPIO [unused]			HiZ Analog Unb
P15[2]	55	GPIO [unused]			HiZ Analog Unb
P15[3]	56	GPIO [unused]			HiZ Analog Unb
P15[4]	93	BRAKE	Software In/Out	Strong drive	HiZ Analog Unb
P15[5]	94	OPR_LED	Software In/Out	Strong drive	HiZ Analog Unb
P15[6]	35	USB IO [unused]			HiZ Analog Unb
P15[7]	36	USB IO [unused]			HiZ Analog Unb
P2[0]	95	GPIO [unused]			HiZ Analog Unb
P2[1]	96	GPIO [unused]			HiZ Analog Unb
P2[2]	97	GPIO [unused]			HiZ Analog Unb
P2[3]	98	GPIO [unused]			HiZ Analog Unb
P2[4]	99	GPIO [unused]			HiZ Analog Unb
P2[5]	1	GPIO [unused]			HiZ Analog Unb
P2[6]	2	REV_SENSE	Software In/Out	Strong drive	HiZ Analog Unb
P2[7]	3	GPIO [unused]			HiZ Analog Unb
P3[0]	44	GPIO [unused]			HiZ Analog Unb

Port	Pin	Name	Type	Drive Mode	Reset State
P3[1]	45	GPIO [unused]			HiZ Analog Unb
P3[2]	46	\ADC:Bypass_P32\	Analog	HiZ analog	HiZ Analog Unb
P3[3]	47	GPIO [unused]			HiZ Analog Unb
P3[4]	48	GPIO [unused]			HiZ Analog Unb
P3[5]	49	GPIO [unused]			HiZ Analog Unb
P3[6]	51	GRIP_DIG_FRN	Software In/Out	Res pull up	HiZ Analog Unb
P3[7]	52	GPIO [unused]			HiZ Analog Unb
P4[0]	69	IND_RED_FRN	Software In/Out	Open drain, drives high	HiZ Analog Unb
P4[1]	70	IND_GRN_FRN	Software In/Out	Open drain, drives high	HiZ Analog Unb
P4[2]	80	IND_BLU_FRN	Software In/Out	Open drain, drives high	HiZ Analog Unb
P4[3]	81	GPIO [unused]			HiZ Analog Unb
P4[4]	82	GPIO [unused]			HiZ Analog Unb
P4[5]	83	GPIO [unused]			HiZ Analog Unb
P4[6]	84	KEY_NO_FRN	Software In/Out	Res pull up	HiZ Analog Unb
P4[7]	85	GPIO [unused]			HiZ Analog Unb
P5[0]	16	GPIO [unused]			HiZ Analog Unb
P5[1]	17	GPIO [unused]			HiZ Analog Unb
P5[2]	18	GPIO [unused]			HiZ Analog Unb
P5[3]	19	GPIO [unused]			HiZ Analog Unb
P5[4]	31	GPIO [unused]			HiZ Analog Unb
P5[5]	32	GPIO [unused]			HiZ Analog Unb
P5[6]	33	GPIO [unused]			HiZ Analog Unb
P5[7]	34	GPIO [unused]			HiZ Analog Unb
P6[0]	89	GPIO [unused]			HiZ Analog Unb
P6[1]	90	GPIO [unused]			HiZ Analog Unb
P6[2]	91	GPIO [unused]			HiZ Analog Unb
P6[3]	92	GPIO [unused]			HiZ Analog Unb
P6[4]	6	GPIO [unused]			HiZ Analog Unb
P6[5]	7	GPIO [unused]			HiZ Analog Unb
P6[6]	8	GPIO [unused]			HiZ Analog Unb
P6[7]	9	GPIO [unused]			HiZ Analog Unb

Abbreviations used in Table 4 have the following meanings:

- HiZ analog = High impedance analog
- HiZ Analog Unb = Hi-Z Analog Unbuffered
- Dgtl Out = Digital Output
- Dgtl In = Digital Input
- HiZ digital = High impedance digital
- OD, DL = Open drain, drives low
- Res pull up = Resistive pull up

2.3 Software Pins

Table 5 contains information about the software pins on this device in alphabetical order. (Only software-accessible pins are shown.)

Table 5. Software Pins

Name	Port	Type	Reset State
\ADC:Bypass_P32\	P3[2]	Analog	HiZ Analog Unb
BRAKE	P15[4]	Software In/Out	HiZ Analog Unb
Debug:SWD_CK	P1[1]	Reserved	
Debug:SWD_IO	P1[0]	Reserved	
GPIO [unused]	P6[0]		HiZ Analog Unb
GPIO [unused]	P15[0]		HiZ Analog Unb
GPIO [unused]	P3[5]		HiZ Analog Unb
GPIO [unused]	P3[4]		HiZ Analog Unb
GPIO [unused]	P3[3]		HiZ Analog Unb
GPIO [unused]	P3[1]		HiZ Analog Unb
GPIO [unused]	P15[1]		HiZ Analog Unb
GPIO [unused]	P3[0]		HiZ Analog Unb
GPIO [unused]	P3[7]		HiZ Analog Unb
GPIO [unused]	P0[3]		HiZ Analog Unb
GPIO [unused]	P0[2]		HiZ Analog Unb
GPIO [unused]	P4[3]		HiZ Analog Unb
GPIO [unused]	P0[5]		HiZ Analog Unb
GPIO [unused]	P0[4]		HiZ Analog Unb
GPIO [unused]	P0[7]		HiZ Analog Unb
GPIO [unused]	P0[6]		HiZ Analog Unb
GPIO [unused]	P15[3]		HiZ Analog Unb
GPIO [unused]	P15[2]		HiZ Analog Unb
GPIO [unused]	P4[4]		HiZ Analog Unb
GPIO [unused]	P4[5]		HiZ Analog Unb
GPIO [unused]	P4[7]		HiZ Analog Unb
GPIO [unused]	P5[1]		HiZ Analog Unb
GPIO [unused]	P5[2]		HiZ Analog Unb
GPIO [unused]	P2[2]		HiZ Analog Unb
GPIO [unused]	P5[0]		HiZ Analog Unb
GPIO [unused]	P1[3]		HiZ Analog Unb
GPIO [unused]	P1[4]		HiZ Analog Unb
GPIO [unused]	P5[3]		HiZ Analog Unb
GPIO [unused]	P1[2]		HiZ Analog Unb
GPIO [unused]	P2[4]		HiZ Analog Unb
GPIO [unused]	P2[3]		HiZ Analog Unb
GPIO [unused]	P2[5]		HiZ Analog Unb
GPIO [unused]	P2[7]		HiZ Analog Unb
GPIO [unused]	P6[6]		HiZ Analog Unb
GPIO [unused]	P6[7]		HiZ Analog Unb
GPIO [unused]	P6[4]		HiZ Analog Unb
GPIO [unused]	P6[5]		HiZ Analog Unb
GPIO [unused]	P1[5]		HiZ Analog Unb
GPIO [unused]	P6[1]		HiZ Analog Unb
GPIO [unused]	P5[4]		HiZ Analog Unb
GPIO [unused]	P2[0]		HiZ Analog Unb

Name	Port	Type	Reset State
GPIO [unused]	P5[6]		HiZ Analog Unb
GPIO [unused]	P6[2]		HiZ Analog Unb
GPIO [unused]	P6[3]		HiZ Analog Unb
GPIO [unused]	P5[7]		HiZ Analog Unb
GPIO [unused]	P2[1]		HiZ Analog Unb
GPIO [unused]	P1[6]		HiZ Analog Unb
GPIO [unused]	P1[7]		HiZ Analog Unb
GPIO [unused]	P5[5]		HiZ Analog Unb
GRIP_DIG_FRN	P3[6]	Software In/Out	HiZ Analog Unb
HAL_LEFT_FRN	P0[1]	Analog	HiZ Analog Unb
HAL_RIGHT_FRN	P0[0]	Analog	HiZ Analog Unb
IND_BLU_FRN	P4[2]	Software In/Out	HiZ Analog Unb
IND_GRN_FRN	P4[1]	Software In/Out	HiZ Analog Unb
IND_RED_FRN	P4[0]	Software In/Out	HiZ Analog Unb
KEY_NO_FRN	P4[6]	Software In/Out	HiZ Analog Unb
OPR_LED	P15[5]	Software In/Out	HiZ Analog Unb
REV_SENSE	P2[6]	Software In/Out	HiZ Analog Unb
S1	P12[2]	Dgtl Out	HiZ Analog Unb
S2	P12[3]	Dgtl In	HiZ Analog Unb
SCL_1	P12[4]	Software In/Out	HiZ Analog Unb
SDA_1	P12[5]	Software In/Out	HiZ Analog Unb
SIO [unused]	P12[6]		HiZ Analog Unb
SIO [unused]	P12[0]		HiZ Analog Unb
SIO [unused]	P12[1]		HiZ Analog Unb
SIO [unused]	P12[7]		HiZ Analog Unb
USB IO [unused]	P15[6]		HiZ Analog Unb
USB IO [unused]	P15[7]		HiZ Analog Unb

Abbreviations used in Table 5 have the following meanings:

- HiZ Analog Unb = Hi-Z Analog Unbuffered
- Dgtl Out = Digital Output
- Dgtl In = Digital Input

For more information on reading, writing and configuring pins, please refer to:

- Pins chapter in the System Reference Guide
  - CyPins API routines
- Programming Application Interface section in the cy_pins component datasheet

3 System Settings

3.1 System Configuration

Table 6. System Configuration Settings

Name	Value
Device Configuration Mode	Compressed
Enable Error Correcting Code (ECC)	False
Store Configuration Data in ECC Memory	True
Instruction Cache Enabled	True
Enable Fast IMO During Startup	True
Unused Bonded IO	Disallowed
Heap Size (bytes)	0x200
Stack Size (bytes)	0x1200
Include CMSIS Core Peripheral Library Files	True

3.2 System Debug Settings

Table 7. System Debug Settings

Name	Value
Debug Select	SWD (serial wire debug)
Enable Device Protection	False
Embedded Trace (ETM)	False
Use Optional XRES	False

3.3 System Operating Conditions

Table 8. System Operating Conditions

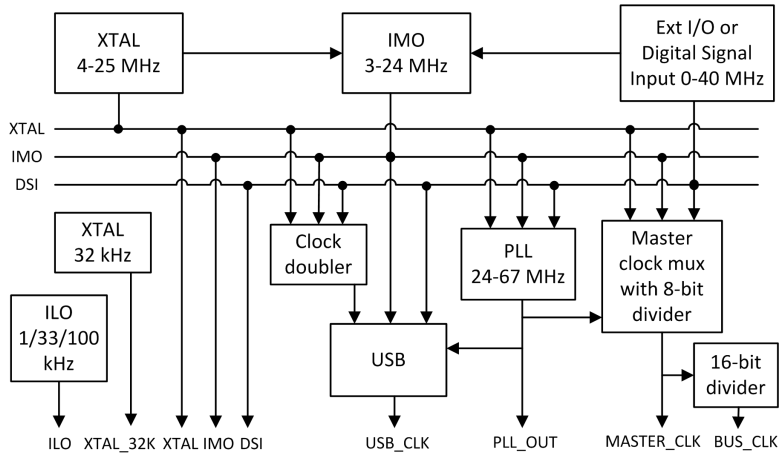
Name	Value
VDDA (V)	5
VDDD (V)	5
VDDIO0 (V)	5.0
VDDIO1 (V)	5.0
VDDIO2 (V)	5.0
VDDIO3 (V)	5.0
Variable VDDA	True
Temperature Range	-40C - 85/125C

4 Clocks

The clock system includes these clock resources:

- Four internal clock sources increase system integration:
  - 3 to 74.7 MHz Internal Main Oscillator (IMO) ±1% at 3 MHz
  - 1 kHz, 33 kHz, and 100 kHz Internal Low Speed Oscillator (ILO) outputs
  - 12 to 80 MHz clock doubler output, sourced from IMO, MHz External Crystal Oscillator (MHzECO), and Digital System Interconnect (DSI)
  - 24 to 80 MHz fractional Phase-Locked Loop (PLL) sourced from IMO, MHzECO, and DSI
- Clock generated using a DSI signal from an external I/O pin or other logic
- Two external clock sources provide high precision clocks:
  - 4 to 25 MHz External Crystal Oscillator (MHzECO)
  - 32.768 kHz External Crystal Oscillator (kHzECO) for Real Time Clock (RTC)
- Dedicated 16-bit divider for bus clock
- Eight individually sourced 16-bit clock dividers for the digital system peripherals
- Four individually sourced 16-bit clock dividers with skew for the analog system peripherals
- IMO has a USB mode that synchronizes to USB host traffic, requiring no external crystal for USB. (USB equipped parts only)

Figure 3. System Clock Configuration



4.1 System Clocks

Table 9 lists the system clocks used in this design.

Table 9. System Clocks

Name	Domain	Source	Desired Freq	Nominal Freq	Accuracy (%)	Start at Reset	Enabled
BUS_CLK	DIGITAL	MASTER_CLK	? MHz	24 MHz	±1	True	True
PLL_OUT	DIGITAL	IMO	24 MHz	24 MHz	±1	True	True
MASTER_CLK	DIGITAL	PLL_OUT	? MHz	24 MHz	±1	True	True
IMO	DIGITAL		3 MHz	3 MHz	±1	True	True
ILO	DIGITAL		? MHz	1 kHz	-50,+100	True	True
USB_CLK	DIGITAL	IMO	48 MHz	? MHz	±0	False	False
XTAL	DIGITAL		24 MHz	? MHz	±0	False	False
XTAL 32kHz	DIGITAL		32.768 kHz	? MHz	±0	False	False
Digital Signal	DIGITAL		? MHz	? MHz	±0	False	False

4.2 Local and Design Wide Clocks

Local clocks drive individual analog and digital blocks. Design wide clocks are a user-defined optimization, where two or more analog or digital blocks that share a common clock profile (frequency, etc) can be driven from the same clock divider output source.

Figure 4. Local and Design Wide Clock Configuration

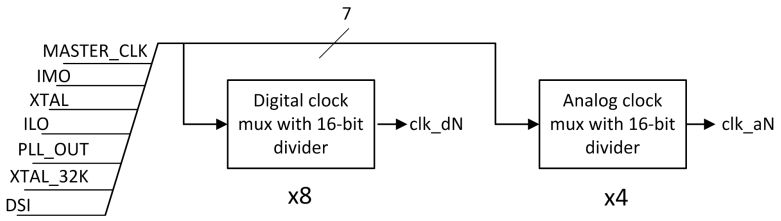


Table 10 lists the design wide clocks used in this design.

Table 10. Design Wide Clocks

Name	Domain	Source	Desired Freq	Nominal Freq	Accuracy (%)	Start at Reset	Enabled
ScBoostClk	ANALOG	PLL_OUT	10 MHz	12 MHz	±1	False	True

Table 11 lists the local clocks used in this design.

Table 11. Local Clocks

Name	Domain	Source	Desired Freq	Nominal Freq	Accuracy (%)	Start at Reset	Enabled
ClockX	DIGITAL	MASTER_CLK	24 MHz	24 MHz	±1	True	True
ADC_Ext_CP_-Clk	DIGITAL	MASTER_CLK	? MHz	24 MHz	±1	True	True
ADC_theACLK	ANALOG	MASTER_CLK	2.19 MHz	2.182 MHz	±1	True	True

Name	Domain	Source	Desired Freq	Nominal Freq	Accuracy (%)	Start at Reset	Enabled
UART_IntClock	DIGITAL	MASTER_CLK	921.6 kHz	923.077 kHz	±1	True	True

For more information on clocking resources, please refer to:

- Clocking System chapter in the PSoC 5LP Technical Reference Manual
- Clocking chapter in the System Reference Guide
  - CyPLL API routines
  - CyIMO API routines
  - CyILO API routines
  - CyMaster API routines
  - CyXTAL API routines

5 Interrupts and DMAs

5.1 Interrupts

This design contains the following interrupt components: (0 is the highest priority)

Table 12. Interrupts

Name	Intr Num	Vector	Priority
ISR1s	0	0	7
ISR5s	1	1	7
ISRtimerXs	2	2	0
ADC_IRQ	29	29	7

For more information on interrupts, please refer to:

- Interrupt Controller chapter in the PSoC 5LP Technical Reference Manual
- Interrupts chapter in the System Reference Guide
  - CyInt API routines and related registers
- Datasheet for cy_isr component

5.2 DMAs

This design contains no DMA components.

6 Flash Memory

PSoC 5LP devices offer a host of Flash protection options and device security features that you can leverage to meet the security and protection requirements of an application. These requirements range from protecting configuration settings or Flash data to locking the entire device from external access.

Table 13 lists the Flash protection settings for your design.

Table 13. Flash Protection Settings

Start Address	End Address	Protection Level
0x0	0x3FFFF	U - Unprotected

Flash memory is organized as rows with each row of flash having 256 bytes. Each flash row can be assigned one of four protection levels:

- U - Unprotected
- F - Factory Upgrade
- R - Field Upgrade
- W - Full Protection

For more information on Flash memory and protection, please refer to:

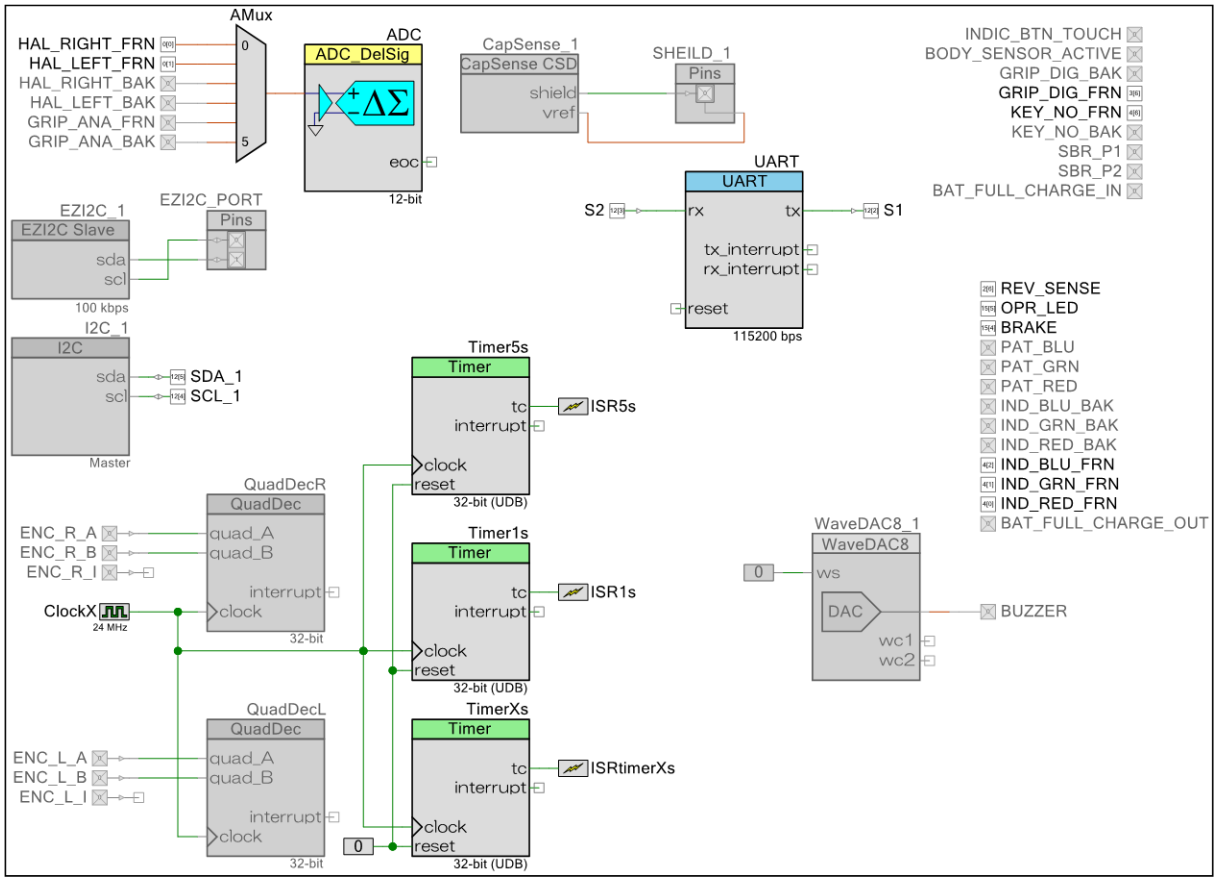
- Flash Protection chapter in the PSoC 5LP Technical Reference Manual
- Flash and EEPROM chapter in the System Reference Guide
  - CyWrite API routines
  - CyFlash API routines

7 Design Contents

This design's schematic content consists of the following schematic sheet:

7.1 Schematic Sheet: Page 1

Figure 5. Schematic Sheet: Page 1



This schematic sheet contains the following component instances:

- Instance ADC (type: ADC_DelSig_v3_30)
- Instance AMux (type: AMux_v1_80)
- Instance Timer1s (type: Timer_v2_80)
- Instance Timer5s (type: Timer_v2_80)
- Instance TimerXs (type: Timer_v2_80)
- Instance UART (type: UART_v2_50)

8 Components

8.1 Component type: ADC_DelSig [v3.30]

8.1.1 Instance ADC

Description: Delta-Sigma ADC
Instance type: ADC_DelSig [v3.30]
Datasheet: online component datasheet for ADC_DelSig

Table 14. Component Parameters for ADC

Parameter Name	Value	Description
ADC_Alignment	Right	This parameter determines how the result is aligned in the 24 bit result word.
ADC_Alignment_Config2	Right	This parameter determines how the result is aligned in the 24 bit result word.
ADC_Alignment_Config3	Right	This parameter determines how the result is aligned in the 24 bit result word.
ADC_Alignment_Config4	Right	This parameter determines how the result is aligned in the 24 bit result word.
ADC_Charge_Pump_Clock	true	Low power charge pump clock selection
ADC_Clock	Internal	Parameter for selecting the ADC clock type.
ADC_Input_Mode	Single	Differential or Single ended input mode
ADC_Input_Range	Vssa to Vdda	Choose input operating mode that best supports the range of the signals being measured.
ADC_Input_Range_Config2	-Input +/- Vref	Choose input operating mode that best supports the range of the signals being measured.
ADC_Input_Range_Config3	-Input +/- Vref	Choose input operating mode that best supports the range of the signals being measured.
ADC_Input_Range_Config4	-Input +/- Vref	Choose input operating mode that best supports the range of the signals being measured.
ADC_Power	Medium Power	Sets power level of ADC.
ADC_Reference	Internal Vdda/4 Bypassed on P3.2	Selects voltage reference source and configuration.
ADC_Reference_Config2	Internal 1.024 Volts	Selects voltage reference source and configuration.
ADC_Reference_Config3	Internal 1.024 Volts	Selects voltage reference source and configuration.
ADC_Reference_Config4	Internal 1.024 Volts	Selects voltage reference source and configuration.
ADC_Resolution	12	ADC Resolution in bits
ADC_Resolution_Config2	16	ADC Resolution in bits

Parameter Name	Value	Description
ADC_Resolution_Config3	16	ADC Resolution in bits
ADC_Resolution_Config4	16	ADC Resolution in bits
Clock_Frequency	64000	Determines the ADC clock frequency.
Comment_Config1	Default Config	Parameter which holds the user comment for the config1.
Comment_Config2	Second Config	Parameter which holds the user comment for the config2.
Comment_Config3	Third Config	Parameter which holds the user comment for the config3.
Comment_Config4	Fourth Config	Parameter which holds the user comment for the config4.
Config1_Name	CFG1	This parameter is used to create constants in the header file for config 1.
Config2_Name	CFG2	This parameter is used to create constants in the header file for config 2.
Config3_Name	CFG3	This parameter is used to create constants in the header file for config 3.
Config4_Name	CFG4	This parameter is used to create constants in the header file for config 4.
Configs	1	Number of active configurations
Conversion_Mode	3 - Multi Sample (Turbo)	ADC conversion mode
Conversion_Mode_Config2	2 - Continuous	ADC conversion mode
Conversion_Mode_Config3	2 - Continuous	ADC conversion mode
Conversion_Mode_Config4	2 - Continuous	ADC conversion mode
Enable_Vref_Vss	false	Determines whether or not to connect ADC's reference Vssa to AGL[6].
EnableModulatorInput	false	When this parameter is enabled, the modulator input terminal will be enabled on the symbol.
Input_Buffer_Gain	1	Gain of input amplifier
Input_Buffer_Gain_Config2	1	Gain of input amplifier
Input_Buffer_Gain_Config3	1	Gain of input amplifier
Input_Buffer_Gain_Config4	1	Gain of input amplifier
Input_Buffer_Mode	Rail to Rail	Buffer Mode type selection
Input_Buffer_Mode_Config2	Rail to Rail	Buffer Mode type selection
Input_Buffer_Mode_Config3	Rail to Rail	Buffer Mode type selection
Input_Buffer_Mode_Config4	Rail to Rail	Buffer Mode type selection
Ref_Voltage	1.25	Set reference voltage
Ref_Voltage_Config2	1.024	Set reference voltage
Ref_Voltage_Config3	1.024	Set reference voltage
Ref_Voltage_Config4	1.024	Set reference voltage
rm_int	false	Removes internal interrupt (IRQ)
Sample_Rate	14698	Sample Rate in Hz

Parameter Name	Value	Description
Sample_Rate_Config2	10000	Sample Rate in Hz
Sample_Rate_Config3	10000	Sample Rate in Hz
Sample_Rate_Config4	10000	Sample Rate in Hz
Start_of_Conversion	Software	Continuous conversions or hardware controlled
User Comments		Instance-specific comments.

8.2 Component type: AMux [v1.80]

8.2.1 Instance AMux

Description: Multiplexer used to route analog signals.
Instance type: AMux [v1.80]
Datasheet: online component datasheet for AMux

Table 15. Component Parameters for AMux

Parameter Name	Value	Description
AtMostOneActive	false	Limit to at most one active channel.
Channels	6	Channel count.
Isolation	Maximum	Specify minimum, medium, or maximum switch control; affects channel isolation and switching time.
MuxType	Single	Select between single or differential inputs.
User Comments		Instance-specific comments.

8.3 Component type: Timer [v2.80]

8.3.1 Instance Timer1s

Description: 8, 16, 24 or 32-bit Timer
Instance type: Timer [v2.80]
Datasheet: online component datasheet for Timer

Table 16. Component Parameters for Timer1s

Parameter Name	Value	Description
CaptureAlternatingFall	false	Enables data capture on either edge but not until a valid falling edge is detected first.
CaptureAlternatingRise	false	Enables data capture on either edge but not until a valid rising edge is detected first.
CaptureCount	2	The CaptureCount parameter works as a divider on the hardware input "capture". A CaptureCount value of 2 would result in an actual capture taking place every other time the input "capture" is changed.
CaptureCounterEnabled	false	Enables the capture counter to count capture events (up to 127) before a capture is triggered.

Parameter Name	Value	Description
CaptureMode	None	This parameter defines the capture input signal requirements to trigger a valid capture event
EnableMode	Software Only	This parameter specifies the methods in enabling the component. Hardware mode makes the enable input pin visible. Software mode may reduce the resource usage if not enabled.
FixedFunction	false	Configures the component to use fixed function HW block instead of the UDB implementation.
InterruptOnCapture	false	Parameter to check whether interrupt on a capture event is enabled or disabled.
InterruptOnFIFOFull	false	Parameter to check whether interrupt on a FIFO Full event is enabled disabled.
InterruptOnTC	true	Parameter to check whether interrupt on a TC is enabled or disabled.
NumberOfCaptures	1	Number of captures allowed until the counter is cleared or disabled.
Period	23999999	Defines the timer period (This is also the reload value when terminal count is reached)
Resolution	32	Defines the resolution of the hardware. This parameter affects how many bits are used in the Period counter and defines the maximum resolution of the internal component signals.
RunMode	Continuous	Defines the hardware to run continuously, run until a terminal count is reached or run until an interrupt event is triggered.
TriggerMode	None	Defines the required trigger input signal to cause a valid trigger enable of the timer
User Comments		Instance-specific comments.

8.3.2 Instance Timer5s

Description: 8, 16, 24 or 32-bit Timer
Instance type: Timer [v2.80]
Datasheet: online component datasheet for Timer

Table 17. Component Parameters for Timer5s

Parameter Name	Value	Description
CaptureAlternatingFall	false	Enables data capture on either edge but not until a valid falling edge is detected first.

Parameter Name	Value	Description
CaptureAlternatingRise	false	Enables data capture on either edge but not until a valid rising edge is detected first.
CaptureCount	2	The CaptureCount parameter works as a divider on the hardware input "capture". A CaptureCount value of 2 would result in an actual capture taking place every other time the input "capture" is changed.
CaptureCounterEnabled	false	Enables the capture counter to count capture events (up to 127) before a capture is triggered.
CaptureMode	None	This parameter defines the capture input signal requirements to trigger a valid capture event
EnableMode	Software Only	This parameter specifies the methods in enabling the component. Hardware mode makes the enable input pin visible. Software mode may reduce the resource usage if not enabled.
FixedFunction	false	Configures the component to use fixed function HW block instead of the UDB implementation.
InterruptOnCapture	false	Parameter to check whether interrupt on a capture event is enabled or disabled.
InterruptOnFIFOFull	false	Parameter to check whether interrupt on a FIFO Full event is enabled disabled.
InterruptOnTC	true	Parameter to check whether interrupt on a TC is enabled or disabled.
NumberOfCaptures	1	Number of captures allowed until the counter is cleared or disabled.
Period	71999999	Defines the timer period (This is also the reload value when terminal count is reached)
Resolution	32	Defines the resolution of the hardware. This parameter affects how many bits are used in the Period counter and defines the maximum resolution of the internal component signals.
RunMode	Continuous	Defines the hardware to run continuously, run until a terminal count is reached or run until an interrupt event is triggered.
TriggerMode	None	Defines the required trigger input signal to cause a valid trigger enable of the timer
User Comments		Instance-specific comments.

8.3.3 Instance TimerXs

Description: 8, 16, 24 or 32-bit Timer
Instance type: Timer [v2.80]
Datasheet: online component datasheet for Timer

Table 18. Component Parameters for TimerXs

Parameter Name	Value	Description
CaptureAlternatingFall	false	Enables data capture on either edge but not until a valid falling edge is detected first.
CaptureAlternatingRise	false	Enables data capture on either edge but not until a valid rising edge is detected first.
CaptureCount	2	The CaptureCount parameter works as a divider on the hardware input "capture". A CaptureCount value of 2 would result in an actual capture taking place every other time the input "capture" is changed.
CaptureCounterEnabled	false	Enables the capture counter to count capture events (up to 127) before a capture is triggered.
CaptureMode	None	This parameter defines the capture input signal requirements to trigger a valid capture event
EnableMode	Software Only	This parameter specifies the methods in enabling the component. Hardware mode makes the enable input pin visible. Software mode may reduce the resource usage if not enabled.
FixedFunction	false	Configures the component to use fixed function HW block instead of the UDB implementation.
InterruptOnCapture	false	Parameter to check whether interrupt on a capture event is enabled or disabled.
InterruptOnFIFOFull	false	Parameter to check whether interrupt on a FIFO Full event is enabled disabled.
InterruptOnTC	true	Parameter to check whether interrupt on a TC is enabled or disabled.
NumberOfCaptures	1	Number of captures allowed until the counter is cleared or disabled.
Period	239999	Defines the timer period (This is also the reload value when terminal count is reached)

Parameter Name	Value	Description
Resolution	32	Defines the resolution of the hardware. This parameter affects how many bits are used in the Period counter and defines the maximum resolution of the internal component signals.
RunMode	Continuous	Defines the hardware to run continuously, run until a terminal count is reached or run until an interrupt event is triggered.
TriggerMode	None	Defines the required trigger input signal to cause a valid trigger enable of the timer
User Comments		Instance-specific comments.

8.4 Component type: UART [v2.50]

8.4.1 Instance UART

Description: Universal Asynchronous Receiver Transmitter
Instance type: UART [v2.50]
Datasheet: online component datasheet for UART

Table 19. Component Parameters for UART

Parameter Name	Value	Description
Address1	128	This parameter specifies the RX Hardware Address #1.
Address2	0	This parameter specifies the RX Hardware Address #2.
BaudRate	115200	Sets the target baud rate.
BreakBitsRX	13	Specifies the break signal length for the RX (detection) channel.
BreakBitsTX	13	Specifies the break signal length for the TX channel.
BreakDetect	false	Enables the break detect hardware.
CRCoutputsEn	false	Enables the CRC outputs.
EnIntRXInterrupt	false	Enables the internal RX interrupt configuration and the ISR.
EnIntTXInterrupt	false	Enables the internal TX interrupt configuration and the ISR.
FlowControl	None	Enable the flow control signals.
HalfDuplexEn	false	Enables half duplex mode on the RX Half of the UART module.
HwTXEnSignal	false	Enables the external TX enable signal output.
InternalClock	true	Enables the internal clock. This parameter removes the clock input pin.
InterruptOnTXComplete	false	This is an Interrupt mask used to enable/disable the interrupt on 'TX complete' event.

Parameter Name	Value	Description
InterruptOnTXFifoEmpty	false	This is an Interrupt mask used to enable/disable the interrupt on 'TX FIFO empty' event.
InterruptOnTXFifoFull	false	This is an Interrupt mask used to enable/disable the interrupt on 'TX FIFO full' event.
InterruptOnTXFifoNotFull	false	This is an Interrupt mask used to enable/disable the interrupt on 'TX FIFO not full' event.
IntOnAddressDetect	false	Enables the interrupt on hardware address detected event by default
IntOnAddressMatch	false	Enables the interrupt on hardware address match detected event by default
IntOnBreak	false	Enables the interrupt on break signal detected event by default
IntOnByteRcvd	true	Enables the interrupt on RX byte received event by default
IntOnOverrunError	false	Enables the interrupt on overrun error event by default
IntOnParityError	false	Enables the interrupt on parity error event by default
IntOnStopError	false	Enables the interrupt on stop error event by default
NumDataBits	8	Defines the number of data bits. Values can be 5, 6, 7 or 8 bits.
NumStopBits	1	Defines the number of stop bits. Values can be 1 or 2 bits.
OverSamplingRate	8	This parameter defines the over sampling rate.
ParityType	None	Sets the parity type as Odd, Even or Mark/Space
ParityTypeSw	false	This parameter allows the parity type to be changed through software by using the WriteControlRegister API
RXAddressMode	None	Configures the RX hardware address detection mode
RXBufferSize	4	The size of the RAM space allocated for the RX input buffer.
RXEnable	true	Enables the RX in the UART
TXBitClkGenDP	true	When enabled, this parameter enables the TX clock generation on DataPath resource. When disabled, TX clock is generated from Clock7.
TXBufferSize	4	The size of the RAM space allocated for the TX output buffer.
TXEnable	true	Enables the TX in the UART
Use23Polling	true	Allows the use of 2 out of 3 polling resources on the RX UART sampler.
User Comments		Instance-specific comments.

9 Other Resources

The following documents contain important information on Cypress software APIs that might be relevant to this design:

- Standard Types and Defines chapter in the System Reference Guide
  - Software base types
  - Hardware register types
  - Compiler defines
  - Cypress API return codes
  - Interrupt types and macros
- Registers
  - The full PSoC 5LP register map is covered in the PSoC 5LP Registers Technical Reference Manual
  - Register Access chapter in the System Reference Guide
    - CY_GET API routines
    - CY_SET API routines
- System Functions chapter in the System Reference Guide
  - General API routines
  - CyDelay API routines
  - CyVd Voltage Detect API routines
- Power Management
  - Power Supply and Monitoring chapter in the PSoC 5LP Technical Reference Manual
  - Low Power Modes chapter in the PSoC 5LP Technical Reference Manual
  - Power Management chapter in the System Reference Guide
    - CyPm API routines
- Watchdog Timer chapter in the System Reference Guide
  - CyWdt API routines
- Cache Management
  - Cache Controller chapter in the PSoC 5LP Technical Reference Manual
  - Cache chapter in the System Reference Guide
    - CyFlushCache() API routine