#\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

# Create Clock

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create\_clock -period 100MHz {clk}

set\_clock\_groups -asynchronous -group {clk}

create\_clock -name clk\_out -period 10 [get\_ports {clk\_out}]

create\_clock -period 10MHz {altera\_reserved\_tck}

set\_clock\_groups -asynchronous -group {altera\_reserved\_tck}

set\_false\_path -from [get\_clocks altera\_reserved\_tck] -to [get\_clocks clk]

set\_false\_path -from [get\_clocks clk] -to [get\_clocks altera\_reserved\_tck]

derive\_pll\_clocks -create\_base\_clocks

derive\_clock\_uncertainty

# Constrain the input I/O path

set\_input\_delay -clock clk -max 3 [all\_inputs]

set\_input\_delay -clock clk -min 2 [all\_inputs]

# Constrain the output I/O path

set\_output\_delay -clock clk -max 3 [all\_outputs]

set\_output\_delay -clock clk -min 2 [all\_outputs]

#set\_output\_delay -clock { clk\_100 } -max 6 [get\_ports {slwr}]

#set\_output\_delay -clock { clk\_100 } -min -3 [get\_ports {slwr}]

#set\_output\_delay -clock { clk\_100 } -max 6 [get\_ports {slrd}]

#set\_output\_delay -clock { clk\_100 } -min -3 [get\_ports {slrd}]

#set\_output\_delay -clock { clk\_100 } -max 6 [get\_ports {pktend}]

#set\_output\_delay -clock { clk\_100 } -min -3 [get\_ports {pktend}]

#set\_output\_delay -clock { clk\_100 } -max 6 [get\_ports {sloe}]

#set\_output\_delay -clock { clk\_100 } -min -3 [get\_ports {sloe}]

#set\_output\_delay -clock { clk\_100 } -max 6 [get\_ports {PMODE\_2}]

#set\_output\_delay -clock { clk\_100 } -min -3 [get\_ports {PMODE\_2}]

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#set\_input\_delay -clock { clk\_100 } -max 6 [get\_ports {flaga}]

#set\_input\_delay -clock { clk\_100 } -min -3 [get\_ports {flaga}]

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#set\_input\_delay -clock { clk\_100 } -max 6 [get\_ports {flagb}]

#set\_input\_delay -clock { clk\_100 } -min -3 [get\_ports {flagb}]

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#set\_input\_delay -clock { clk\_100 } -max 6 [get\_ports {flagc}]

#set\_input\_delay -clock { clk\_100 } -min -3 [get\_ports {flagc}]

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#set\_input\_delay -clock { clk\_100 } -max 6 [get\_ports {flagd}]

#set\_input\_delay -clock { clk\_100 } -min -3 [get\_ports {flagd}]

#set\_input\_delay -clock theclk -max 4 [get\_ports test\_in]

#set\_input\_delay -clock theclk -min 2 [get\_ports test\_in]

#set\_location\_assignment PIN\_AA18 -to clk

#set\_location\_assignment PIN\_L2 -to clk\_out

#set\_location\_assignment PIN\_AE4 -to reset\_in\_

#

#set\_location\_assignment PIN\_AA1 -to sloe

#set\_location\_assignment PIN\_U1 -to slcs

#set\_location\_assignment PIN\_AB1 -to slwr

#set\_location\_assignment PIN\_W5 -to slrd

#

#

#set\_location\_assignment PIN\_U8 -to pktend

#set\_location\_assignment PIN\_M4 -to PMODE[1]

#set\_location\_assignment PIN\_M3 -to PMODE[0]

#set\_location\_assignment PIN\_AE6 -to RESET

#

#set\_location\_assignment PIN\_N1 -to fdata[0]

#set\_location\_assignment PIN\_H2 -to fdata[1]

#set\_location\_assignment PIN\_J3 -to fdata[2]

#set\_location\_assignment PIN\_L1 -to fdata[3]

#set\_location\_assignment PIN\_K1 -to fdata[4]

#set\_location\_assignment PIN\_N2 -to fdata[5]

#set\_location\_assignment PIN\_N3 -to fdata[6]

#set\_location\_assignment PIN\_U3 -to fdata[7]

#set\_location\_assignment PIN\_U4 -to fdata[8]

#set\_location\_assignment PIN\_Y1 -to fdata[9]

#set\_location\_assignment PIN\_Y2 -to fdata[10]

#set\_location\_assignment PIN\_AA2 -to fdata[11]

#set\_location\_assignment PIN\_AB3 -to fdata[12]

#set\_location\_assignment PIN\_AB6 -to fdata[13]

#set\_location\_assignment PIN\_AB5 -to fdata[14]

#set\_location\_assignment PIN\_W4 -to fdata[15]

#set\_location\_assignment PIN\_Y5 -to flaga

#set\_location\_assignment PIN\_W8 -to flagb

#set\_location\_assignment PIN\_W7 -to flagc

#set\_location\_assignment PIN\_V8 -to flagd

#

#set\_location\_assignment PIN\_T8 -to faddr[1]

#set\_location\_assignment PIN\_T9 -to faddr[0]