Keysight D9020USBC USB3.2 Compliance Test Application

Methods of Implementation

KEYSIGHT TECHNOLOGIES

Notices

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USB3.2 Test Compliance Application—At a Glance

The Keysight D9020USBC USB3.2 Test Compliance Application helps you verify the USB3.2 device complies to the electrical requirements on the SuperSpeed physical layer as defined in the USB3.2 specification, with the Keysight Infiniium digital storage oscilloscopes. The USB3.2 Test Compliance Application:

- Lets you select individual or multiple tests to run.
- Lets you identify the device being tested and its configuration.
- Shows you how to make oscilloscope connections to the device under test.
- Automatically checks for proper oscilloscope configuration.
- Automatically sets up the oscilloscope for each test.
- Provides detailed information for each test that has been run and lets you specify the thresholds at which marginal or critical warnings appear.
- Creates a printable HTML report of the tests that have been run.

NOTE **The tests performed by the USB3.2 Test Compliance Application are intended to provide a quick check of the electrical health of the DUT. This testing is not a replacement for an exhaustive test validation plan.**

For more information, see:

- Chapter 1, “Installing the USB3.2 Test Compliance Application,” starting on page 9.
- Chapter 2, “Preparing to Take Measurements,” starting on page 15.
- Chapter 4, “5G Tests,” starting on page 33.
- Chapter 5, “10G Tests,” starting on page 71.

See Also

Compliance testing measurements are described in the *Universal Serial Bus 3.2 Specification, Revision 1.0*. For more information, see the USB3.2 standards web site at "www.usb.org".

Contents

1 Installing the USB3.2 Test Compliance Application

If you purchased the D9020USBC USB3.2 Test Compliance Application separately from your oscilloscope, you need to install the software and license key.

Installing the Software

1 Make sure you have the minimum required version of the Infiniium oscilloscope software.

   The compliance test application's release notes file describes the minimum required version.

   To check your current version of Infiniium oscilloscope software, choose **Help > About Infiniium...** from the main menu.

2 To obtain the USB3.2 Compliance Test Application, please go to Keysight website: http://www.keysight.com/find/D9020USBC

3 The link for USB3.2 Compliance Test Application will appear. Double-click it and follow the instructions to download and install the application software.

   Be sure to accept the installation of the .NET Framework software; it is required in order to run the USB3.2 Compliance Test Application.

Installing the License Key

To procure a license, you require the Host ID information that is displayed in the Keysight License Manager application installed on the same machine where you wish to install the license.

Using Keysight License Manager 5

To view and copy the Host ID from Keysight License Manager 5:

1 Launch Keysight License Manager on your machine, where you wish to run the Test Application and its features.

2 Copy the Host ID that appears on the top pane of the application. Note that x indicates numeric values.

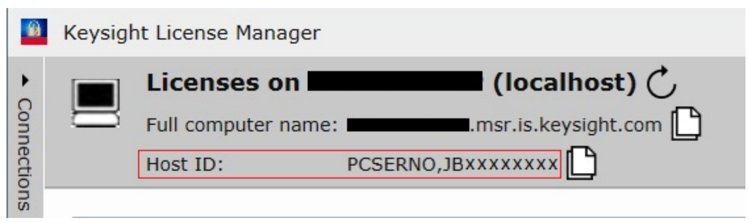


Figure 1 Viewing the Host ID information in Keysight License Manager 5

To install one of the procured licenses using Keysight License Manager 5 application,

1 Save the license files on the machine, where you wish to run the Test Application and its features.

2 Launch Keysight License Manager.

3 From the configuration menu, use one of the options to install each license file.

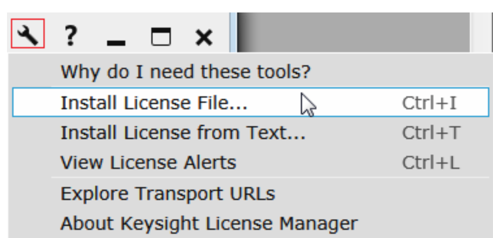


Figure 2 Configuration menu options to install licenses on Keysight License Manager 5

For more information regarding installation of procured licenses on Keysight License Manager 5, refer to Keysight License Manager 5 Supporting Documentation.

Using Keysight License Manager 6

To view and copy the Host ID from Keysight License Manager 6:

1 Launch Keysight License Manager 6 on your machine, where you wish to run the Test Application and its features.

2 Copy the Host ID, which is the first set of alphanumeric value (as highlighted in Figure 3) that appears in the Environment tab of the application. Note that x indicates numeric values.

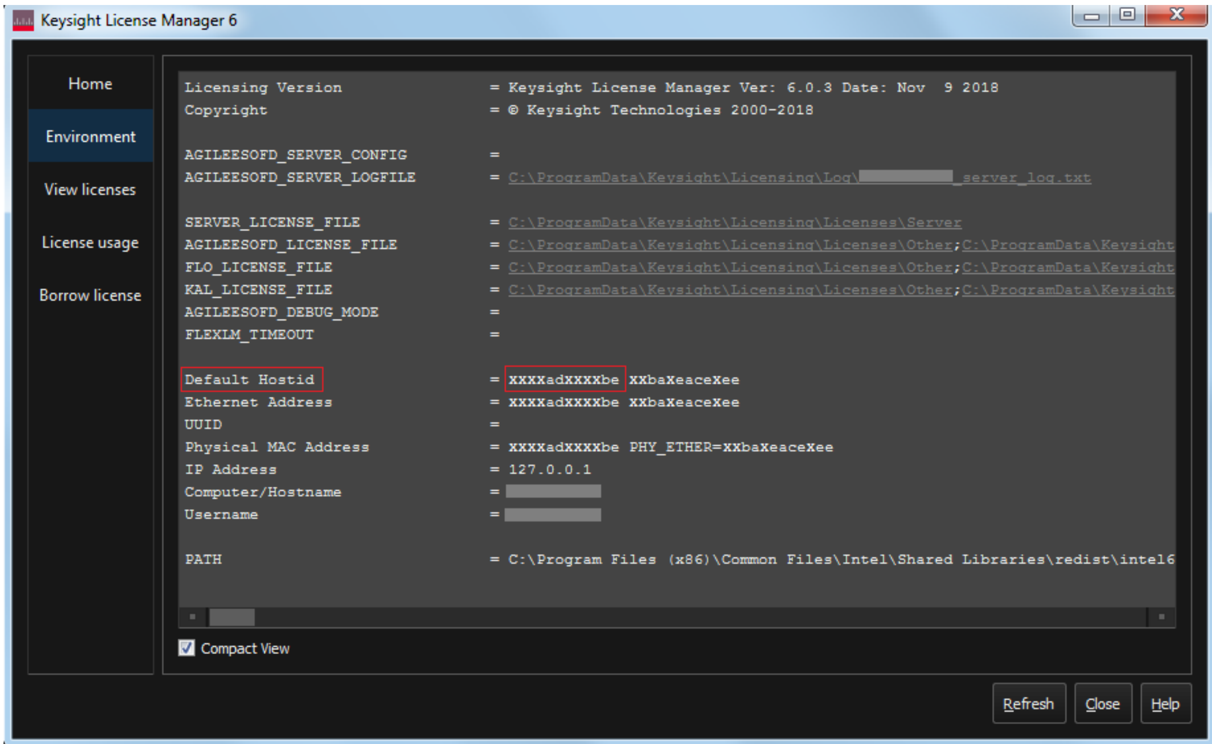


Figure 3 Viewing the Host ID information in Keysight License Manager 6

To install one of the procured licenses using Keysight License Manager 6 application,

1 Save the license files on the machine, where you wish to run the Test Application and its features.
2 Launch Keysight License Manager 6.
3 From the Home tab, use one of the options to install each license file.

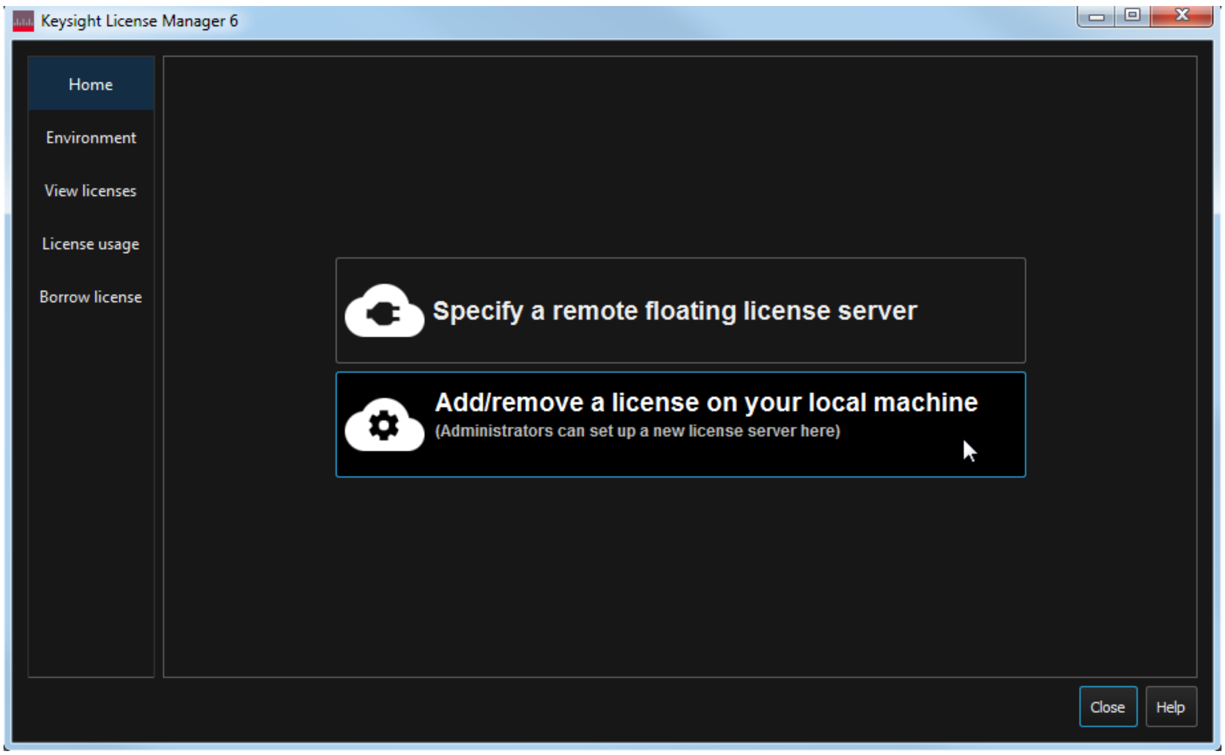


Figure 4 Home menu options to install licenses on Keysight License Manager 6

For more information regarding installation of procured licenses on Keysight License Manager 6, refer to Keysight License Manager 6 Supporting Documentation.

2 Preparing to Take Measurements

Before running the automated tests, you need to acquire the required equipment and software, and you should calibrate the oscilloscope. After the oscilloscope has been calibrated, you are ready to start the USB3.2 Test Compliance Application and perform measurements.

Required Equipment and Software

In order to run the USB3.2 Test Compliance Application, you need the following equipment and software:

- Keysight 90000A Series Infiniium Digital Storage Oscilloscope (DSO) or
  Keysight 90000A X-Series Infiniium Digital Storage Oscilloscope (DSO) or
  Keysight 90000A V-Series Infiniium Digital Storage Oscilloscope (DSO) or
  Keysight 90000A Q-Series Infiniium Digital Storage Oscilloscope (DSO) or
  Keysight 90000A Z-Series Infiniium Digital Storage Oscilloscope (DSO) or
  Keysight UXR Series Infiniium Oscilloscope.

- Keysight recommends using 13 GHz and higher bandwidth oscilloscope with at least 1M memory depth to run D9020USBC USB3.2 tests. The minimum required Infiniium oscilloscope software version is described in the compliance test application release notes. Keysight also recommends using a second monitor to view the automated test application.

- D9020USBC USB3.2 Test Compliance Application software and license.
- E2688A Serial Data Analysis and Clock Recovery software and license (optional).
- N5401A EZJIT Plus software and license (optional).
- Precision BNC to SMA adapter, quantity = 2.
- 50 ohm coaxial cable (24 inches or shorter), quantity = 2, OR
- 1169A Infiniimax probe, quantity = 2.
- U7242A USB 3.0 test fixture.
- Keyboard, quantity = 1 (provided with Keysight Infiniium oscilloscope).
- Mouse, quantity = 1 (provided with Keysight Infiniium oscilloscope).

NOTE

At least 16GHz bandwidth is required to run Gen2 tests.

NOTE

USB3.2 Compliance Test Application supports 2 channel scope.
In two channel mode, switch matrix is not available.

Calibrating the Oscilloscope

If you have not already calibrated the oscilloscope, refer to the documentation related to Keysight 90000A Series Infiniium Oscilloscopes and its compatible probes to know about the calibration procedures.

NOTE If the ambient temperature changes more than 5 degrees Celsius from the calibration temperature, internal calibration should be performed again. The delta between the calibration temperature and the present operating temperature is shown in the **Utilities > Calibration** menu.

NOTE If you switch cables between channels or other oscilloscopes, it is necessary to perform cable and probe calibration again. Keysight recommends that, once calibration is performed, you label the cables with the channel for which they were calibrated.

Connecting the USB 3.2 Test Fixture

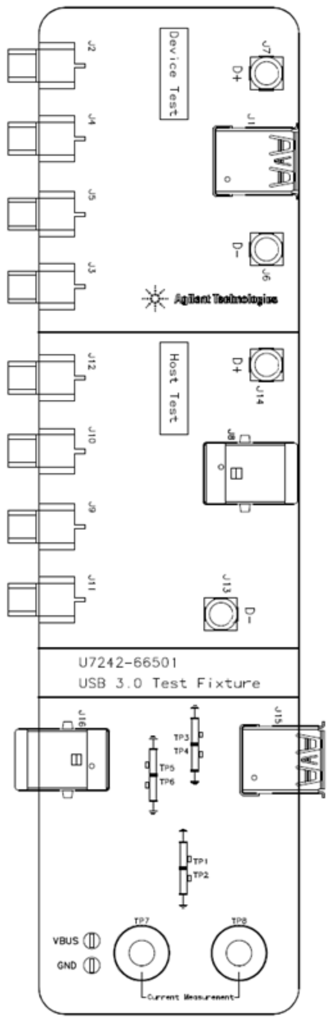
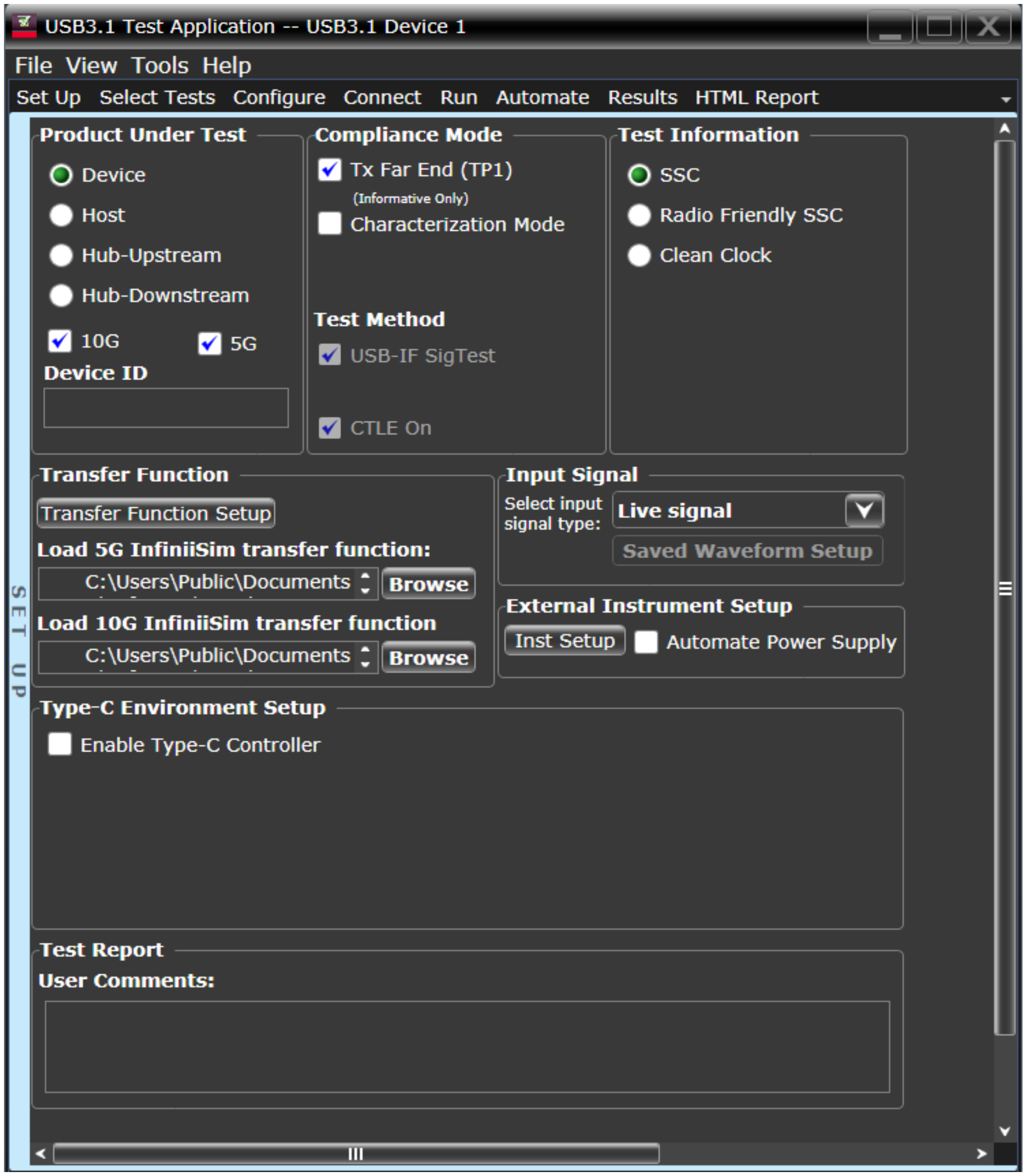


Figure 5 Block Diagram of U7242A USB 3.0 Test Fixture

The U7242A USB 3.0 test fixture is required to perform the USB3.2 electrical compliance test measurements. The fixture helps you to easily access the USB 3.0 test signals.

The connection to this test fixture depends on the type of device under test (DUT):



For Device test:

1 Connect DUT to J1 by using 4 inches USB 3.0 Standard-A to Standard-B cable.
2 Connect J6 and J7 to the oscilloscope to measure USB 2.0 signal.
3 Connect J2 and J3 to the oscilloscope to measure the SuperSpeed (USB 3.0) Transmitter signal.
4 Connect J4 and J5 to the oscilloscope to measure the SuperSpeed (USB 3.0) Receiver signal.

For Host test:

1 Connect DUT to J8 by using 4 inches USB 3.0 Standard-A to Standard-B cable.
2 Connect J13 and J14 to the oscilloscope to measure USB 2.0 signal.
3 Connect J11 and J12 to the oscilloscope to measure the SuperSpeed (USB 3.0) Transmitter signal.
4 Connect J9 and J10 to the oscilloscope to measure the SuperSpeed (USB 3.0) Receiver signal.

For Hub Upstream test:

1 Follow the connection as per the Device test.

For Hub Downstream test:

1 Follow the connection as per the Host test.

Starting the USB3.2 Test Compliance Application

Ensure that the USB3.2 Device Under Test (DUT) is operating and set to desired test modes.

To start the USB3.2 Test Compliance Application, from the Infiniium Oscilloscope's main menu, select **Analyze** > **Automated Test Apps** > **D9020USBC USB3 Test App**.

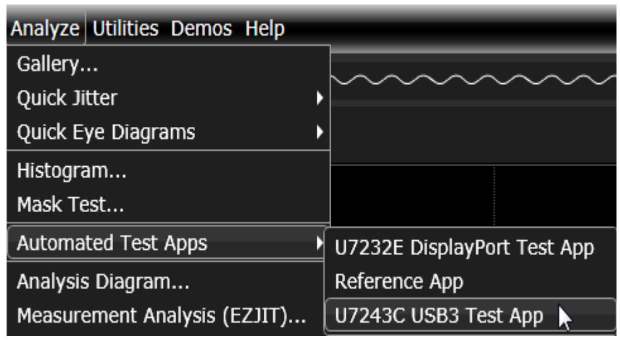


Figure 6 Starting the D9020USBC USB3 Test App

The USB3.2 Test Compliance Application launches with the **Set Up** tab as default.

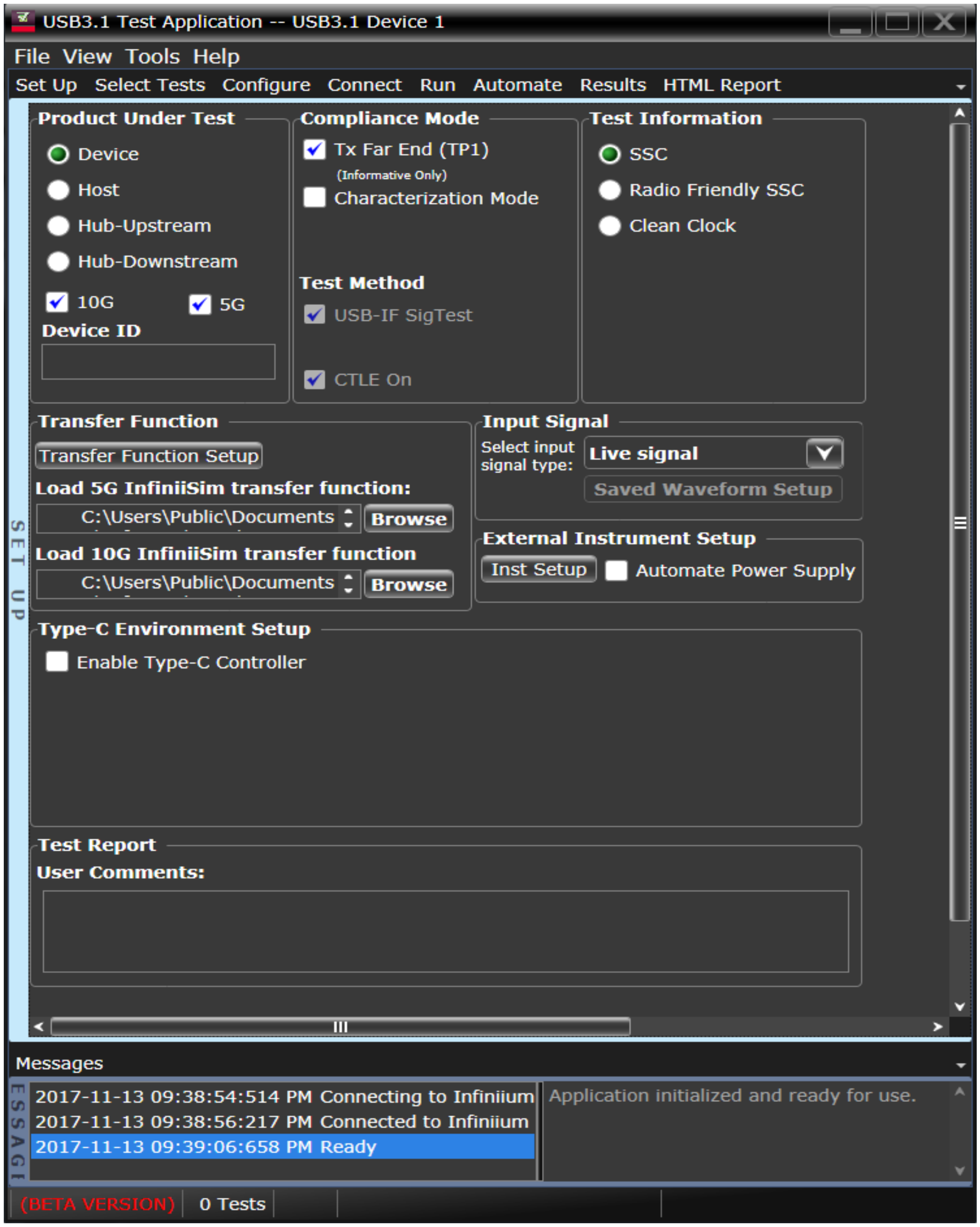


Figure 7 Default window of the USB3.2 Test App

Table 1 provides a brief description of the functionality of each tab in the USB 3.2 Test Application:

Table 1 Functionality of each tab on the USB 3.2 Test App

Tabs on the Test App	Functionality
Set Up	Lets you identify and set up the test environment, including information about the device under test. The **Device ID** and **Comments** are printed in the final HTML report.
Select Tests	Lets you select the tests you want to run. The tests are organized hierarchically so you can select all tests in a group. After tests are run, status indicators show which tests have passed, failed, or not been run, and there are indicators for the test groups.
Configure	Lets you configure test parameters (for example, channels used in test, voltage levels, etc.).
Connect	Shows you how to connect the oscilloscope to the device under test for the tests that are to be run.
Run	Lets you start the automated tests. If the connections to the device under test need to be changed while multiple tests are running, the tests pause, this tab shows you how to change the connection, and the Application waits for you to confirm that the connections have been changed before continuing.
Automate	Lets you construct scripts of commands that drive execution of the Application.
Results	Contains more detailed information about the tests that have been run. You can change the thresholds at which marginal or critical warnings appear.
HTML Report	Shows a compliance test report that can be exported or printed.

Type-C Controller

The usability of the current version of the Keysight D9020USBC USB3.2 Test Compliance Application has been extended to test the signals with the Type-C implementation in USB3.2 devices.

To enable this feature, click **Enable Type-C Controller** in the **Type-C Environment Setup** area of the **Set Up** tab.

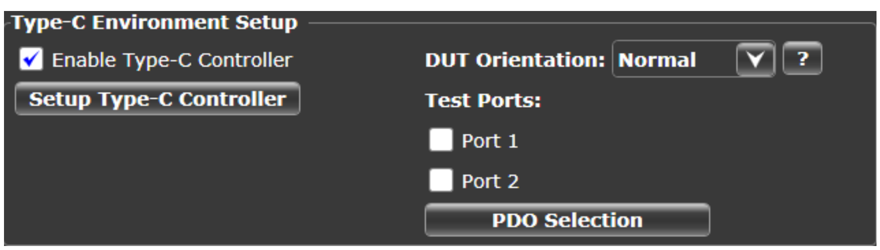


Figure 8 Enabling Type-C Environment Setup

For more information on the functionality of the various features of the USB3.2 Test Application along with the Type-C setup, refer to the *Keysight D9020USBC USB 3.2 Test Compliance Application Online Help*.

3 LFPS Tests

This chapter describes the LFPS tests available in USB3.2 Compliance Test Application in more detail; it contains information from (and refers to) the *Universal Serial Bus 3.2 Specification, Revision 1.0*, and it describes how the tests are performed.

Transmitter Low Frequency Periodic Signaling (LFPS) Tests

The Transmitter Low Frequency Periodic Signaling Tests include:

- LFPS Peak-Peak Differential Output Voltage Test
- LFPS Period (tPeriod) Test
- LFPS Burst Width (tBurst) Test
- LFPS Repeat Time Interval (tRepeat) Test
- LFPS Rise Time Test
- LFPS Fall Time Test
- LFPS Duty Cycle Test
- LFPS AC Common Mode Voltage

This section provides the Methods of Implementation (MOIs) for 5G Low Frequency Periodic Signaling (LFPS) tests using a Keysight 90000A Series Infiniium oscilloscope, USB 3.0 test fixture, and USB3.2 Test Compliance Application.

Connection Diagram See Appendix A, "Test Connection".

Test Reference from the Specification Table 6-29 and Table 6-30 of the USB 3.2 Specification, Revision 1.0

Table 6-29. Normative LFPS Electrical Specification

Symbol	Minimum	Typical	Maximum	Units	Comments
tPeriod	20		100	ns	
tPeriod for SuperSpeedPlus	20		80	ns	
$V_{CM-AC-LFPS}$			$V_{TX-CM-AC-PP-ACTIVE}$	mV	See Table 6-19
$V_{CM-LFPS-Active}$			10	mV	
$V_{TX-DIFF-PP-LFPS}$	800		1200	mV	Peak-peak differential amplitude
$V_{TX-DIFF-PP-LFPS-LP}$	400		600	mV	Low power peak-peak differential amplitude
tRiseFall2080			4	ns	Measured at TP2, as shown in Figure 6-20.
Duty cycle	40		60	%	Measured at compliance TP2, as shown in Figure 6-20.

Figure 9 Table 6-29 of USB 3.2 Specification Version 1.0

Table 6-30. LFPS Transmitter Timing for SuperSpeed Designs[1]

	tBurst				tRepeat		
	Min	Typ	Max	Minimum Number of LFPS Cycles[2]	Min	Typ	Max
Polling.LFPS	0.6 µs	1.0 µs	1.4 µs		6 µs	10 µs	14 µs
Ping.LFPS[8]	40 ns		200 ns	2	160 ms	200 ms	240 ms
Ping.LFPS for SuperSpeedPlus[9]	40 ns		160ns	2	160 ms	200 ms	240 ms
tReset[3]	80 ms	100 ms	120 ms				
U1 Exit[4,5]	900 ns[7]		2 ms				
U2 / Loopback Exit[4,5]	80 µs[7]		2 ms				

	tBurst				tRepeat		
	Min	Typ	Max	Minimum Number of LFPS Cycles[2]	Min	Typ	Max
U3 Wakeup[4,5]	80 µs[7]		10 ms				

Notes:

1. If the transmission of an LFPS signal does not meet the specification, the receiver behavior is undefined.
2. Only Ping.LFPS has a requirement for minimum number of LFPS cycles.
3. The declaration of Ping.LFPS depends on only the Ping.LFPS burst.
4. Warm Reset, U1/U2/Loopback Exit, and U3 Wakeup are all single burst LFPS signals. tRepeat is not applicable.
5. The minimum duration of an LFPS burst shall be transmitted as specified. The LFPS handshake process and timing are defined in Section 6.9.2.
6. A Port in U2 or U3 is not required to keep its transmitter DC common mode voltage. A port in U2 or U3 is not required to keep its transmitter DC common mode voltage but must not exceed the VTX-CM-IDLE-DELTA spec at TP1. This can be met by either managing the magnitude of the CM shift or the slew rate of the shift. Accordingly, LFPS detectors must tolerate positive and negative CM excursions up to VTX-CM-IDLE-DELTA without false detection. When a port begins U2 exit or U3 wakeup, it may start sending LFPS signal while establishing its transmitter DC common mode voltage. To make sure its link partner receives a proper LFPS signal, a minimum of 80 µs tBurst shall be transmitted. The same consideration also applies to a port receiving LFPS U2 exit or U3 wakeup signal.
7. A port is still required to detect U1 LFPS exit signal at a minimum of 300ns. The extra 300ns is provided as the guard band for successful U1 LFPS exit handshake.
8. This requirement applies to Gen 1x1 only designs.
9. This requirement applies to Gen 1x2, Gen 2x1 and Gen 2x2 designs.

Figure 10 Table 6-30 of USB 3.2 Specification Version 1.0

Test Conditions

Type of DUT	LFPS Test Mode
Gen 1	False

Test Overview

The purpose of this test is to evaluate the LFPS signal to ensure that the timing variables comply with the specification.

Test Procedure

1 Disconnect the USB 3.0 test fixture from the DUT.

2 Setup horizontal scaling with Reference to Center, Scale of 10us, position at 32us.

3 Setup Function 1 as subtraction of Channel 1 and Channel 3.
4 Setup Function 4 as common mode of Channel 1 and Channel 3.
5 Setup the trigger:
   a Trigger level to 200mV
   b Trigger mode as Pattern mode
   c Set trigger Logic as High on trigger channel
   d Setup trigger condition to range between 3us to 15 us
6 Setup the trigger to “Single”
7 Setup the Acquisition
   a Select Real Time mode
   b Set interpolation to OFF
   c Acquire points to AUTO
   d Sample rate to 40GSa/s
   e Bandwidth to 12GHz
8 Verify that the correct waveform has been acquired

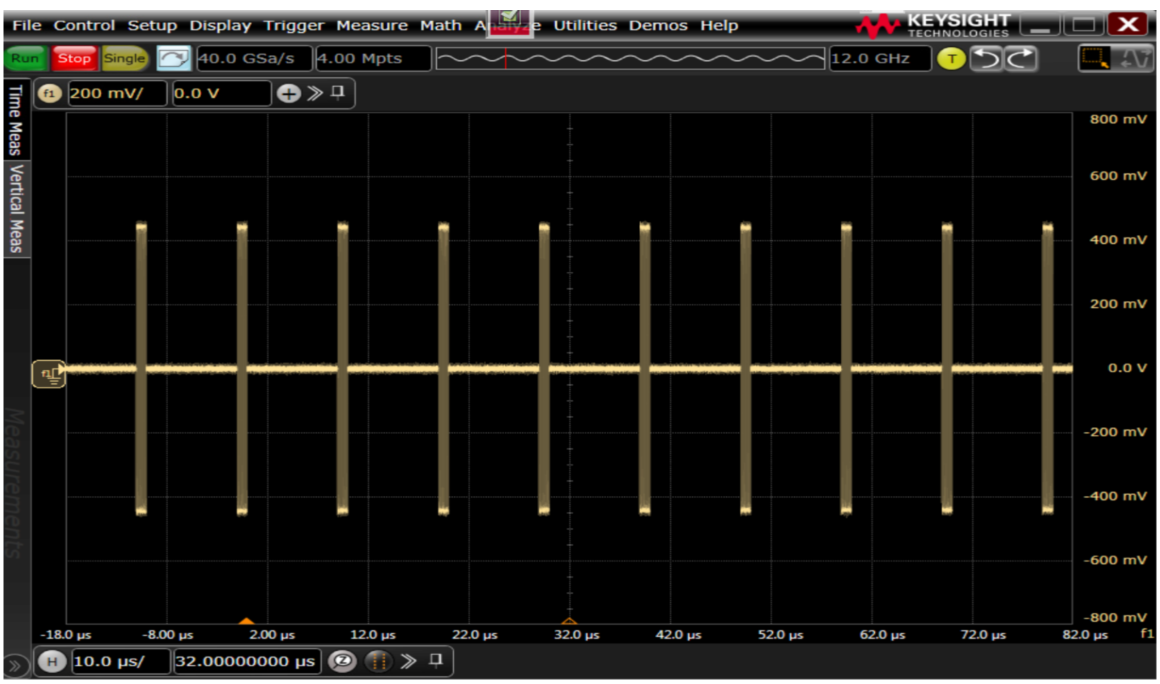


Figure 11 Acquiring the correct waveform

9 Set up the parameter measurement:
   a Get all locations for the Start Burst and the Stop Burst of the LFPS.
   b Burst Width Measurement is the Start edge – Stop edge of the selected Burst.

Figure 12 Burst Width Measurement

c Burst Interval is the Start edge of the next burst – Start edge of current Burst.

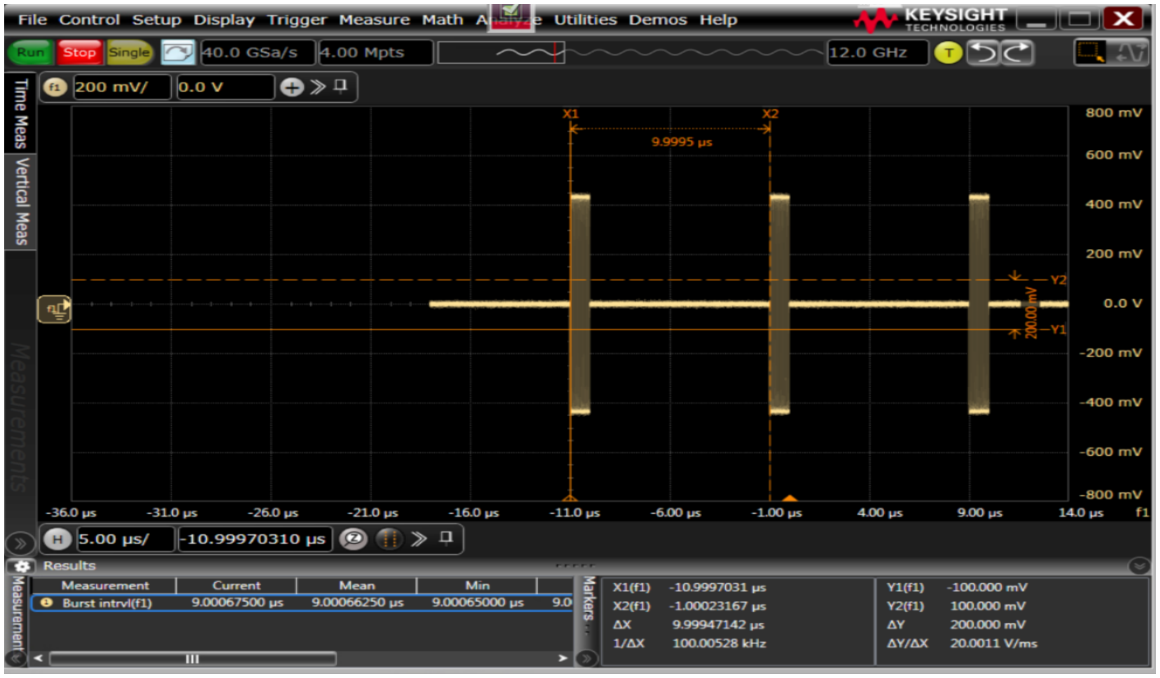


Figure 13 Burst Interval

d Measure the parameter below on each Burst. The measurement window on each Burst must be set to 100ns after the Burst start and 100ns before the Burst end. This is done to comply with CTS requirements.

i Differential Voltage

ii Period

iii Duty Cycle

iv Rise Time

v Fall Time

vi Common Mode Voltage

10 Report the measurement values

Expected / Observable Results

The timing measurement results must be within the conformance limit as specified in the USB 3.2 specification.

Test Conditions#2

Type of DUT	LFPS Test Mode
Gen 1	True

Test Overview

The purpose of this test is to evaluate the LFPS signal to ensure that the timing variables comply with the specification.

Test Procedure

1 Disconnect the USB 3.0 test fixture from the DUT.

2 Setup horizontal scaling with Reference to Center, Scale of 10us, position at 32us.

3 Setup Function 1 as subtraction of Channel 1 and Channel 3.

4 Setup Function 4 as common mode of Channel 1 and Channel 3.

5 Setup the trigger:
   a Trigger level to 200mV
   b Trigger mode as Pattern mode
   c Set trigger Logic as High on trigger channel
   d Setup trigger condition to range between 3us to 15 us
6 Setup the trigger to “Single”
7 Setup the Acquisition
   a Select Real Time mode
   b Set interpolation to OFF
   c Acquire points to AUTO
   d Sample rate to 40GSa/s
   e Bandwidth to 12GHz
8 Verify that the correct waveform has been acquired.
9 Save the waveform in binary format
10 Launch the SigTest tool
   a Ensure that the Test Mode is set to ‘CEM’
   b Ensure that the Technology is set to ‘usb_3-5gb’
   c Ensure that the Template File is set to ‘USB_3_LFPS’

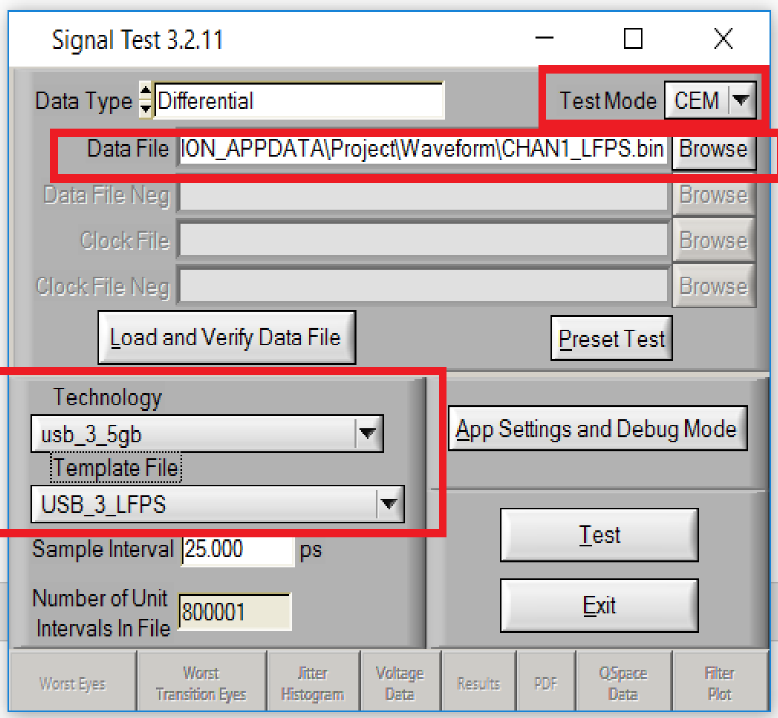


Figure 14 SigTest Tool settings for LFPS tests

11 Report Measurement using the report generated by SigTest tool.

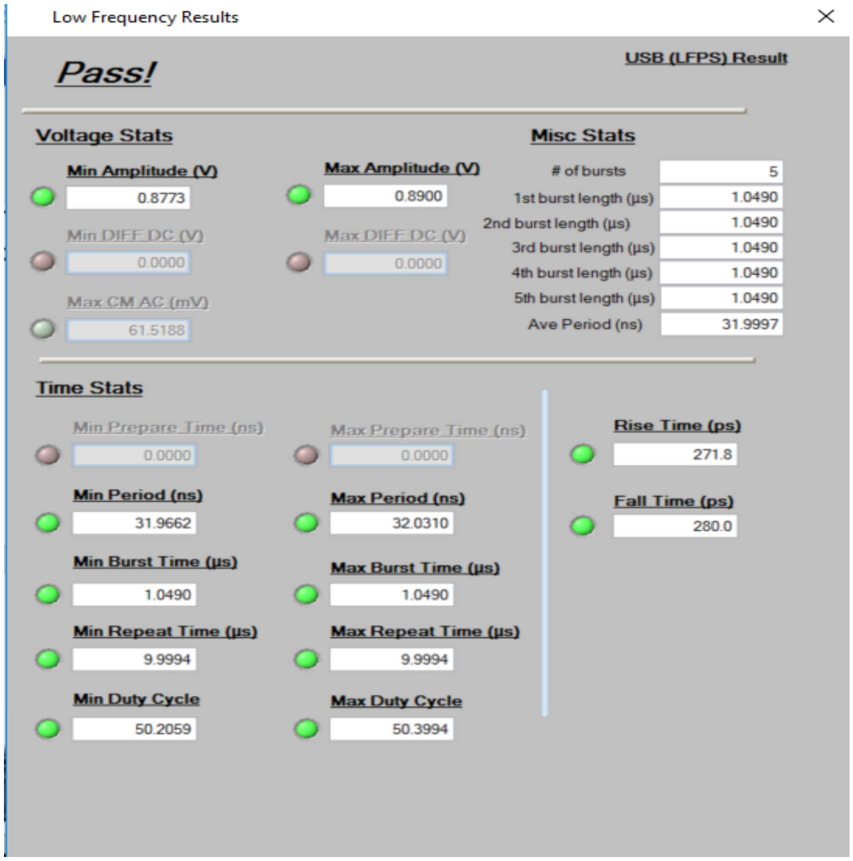


Figure 15 SigTest tool report for LFPS tests

Expected / Observable Results

The timing measurement results must be within the conformance limit as specified in the USB 3.2 specification.

4 5G Tests

This chapter describes the 5G tests that are performed by the USB3.2 Test Compliance Application in more detail; it contains information from (and refers to) the *Universal Serial Bus 3.2 Specification, Revision 1.0*, and it describes how the tests are performed.

5G Transmitter SSC Tests

The 5G Transmitter Spread Spectrum Clocking Tests include:

- Unit Interval (with SSC) Test
- SSC Deviation Test
- SSC Modulation Rate Test
- SSC Slew Rate Test

This section provides the Methods of Implementation (MOIs) for 5G Transmitter SSC tests using a Keysight 90000A Series Infiniium oscilloscope, USB 3.0 test fixture, and USB3.2 Test Compliance Application.

Connection Diagram See Appendix A, “Test Connection”.

Test Reference from the Specification Table 6-17 and Table 6-18 of the USB 3.2 Specification, revision 1.0.

Table 6-17. SSC Parameters

Symbol	Description	Limits		Units	Note
		Min	Max		
$t_{SSC\text{-}MOD\text{-}RATE}$	Modulation Rate	30	33	kHz	
$t_{SSC\text{-}FREQ\text{-}DEVIATION}$	SSC deviation	+0/-4000 +0/-2000	+0/-5000 +0/-3000	ppm	1, 2, 3 4

Note:

1. The data rate is modulated from 0 ppm to -5000 ppm of the nominal data rate frequency and scales with data rate.
2. This is measured below 2 MHz only.
3. Receiver compliance testing is done under the maximum spread condition.
4. Alternate limits apply to “radio friendly” clock mode which employs a clock whose center frequency is downshifted by 2000ppm.

Figure 16 Table 6-17 of USB 3.2 Specification Version 1.0

Table 6-18. Transmitter Normative Electrical Parameters

Symbol	Parameter	Gen 1 (5.0 GT/s)	Gen 2 (10 GT/s)	Units	Comments
UI	Unit Interval	199.94 (min) 200.06 (max)	99.97 (min) 100.03 (max)	ps	The specified UI is equivalent to a tolerance of ±300 ppm for each device. Period does not account for SSC induced variations.
		200.34 (min) 200.46 (max)	100.17 (min) 100.23 (max)	ps	Alternate limits apply to "radio friendly" clocking mode which employs a clock whose center frequency is downshifted by 2000ppm. This mode is to be used with a +0/-3000ppm spread.
$V_{TX-DIFF-PP}$	Differential p-p Tx voltage swing	0.8 (min) 1.2 (max)	0.8 (min) 1.2 (max)	V	Nominal is 1 V p-p
$V_{TX-DIFF-PP-LOW}$	Low-Power Differential p-p Tx voltage swing	0.4 (min) 1.2 (max)	0.4 (min) 1.2 (max)	V	Refer to Section 6.7.2. There is no de-emphasis requirement in this mode. De-emphasis is implementation specific for this mode.
$V_{TX-DE-RATIO}$	Tx de-emphasis	3.0 (min) 4.0 (max)	See section 6.7.5.2.	dB	Nominal is 3.5 dB for Gen 1 operation. Gen 2 transmitter equalization requirements are described in section 6.7.5.2.
$R_{TX-DIFF-DC}$	DC differential impedance	72 (min) 120 (max)	72 (min) 120 (max)	Ω	
$V_{TX-RCV-DETECT}$	The amount of voltage change allowed during Receiver Detection	0.6 (max)	0.6 (max)	V	Detect voltage transition should be an increase in voltage on the pin looking at the detect signal to avoid a high impedance requirement when an "off" receiver's input goes below ground.
$C_{AC-COUPLING}$	AC Coupling Capacitor	75 (min) 265 (max)	75 (min) 265 (max)	nF	All Transmitters shall be AC coupled. The AC coupling is required either within the media or within the transmitting component itself.
$t_{CDR\_SLEW\_MAX}$	Maximum slew rate	10	Not applicable	ms/s	See the jitter white paper for details on this measurement. This is a df/ft specification; refer to Section 6.5.4 for details.
SSC_{dfdt}	SSC df/dt	Not applicable	1250 (max)	ppm/µs	See note 1.
$V_{TX-CM-IDLE-DELTA}$	Transmitter idle common-mode voltage change	+600 (max) -600 (min)	+600 (max) -600 (min)	mV	The maximum allowed instantaneous common-mode voltage at TP2 while the transmitter is in U2 or U3 and not actively transmitting LFPS. Note that this is an absolute voltage spec referenced to the receive-side termination ground but serves the purpose of limiting the magnitude and/or slew rate of Tx common mode changes.

Note 1: Measured over a 0.5µs interval using CP10. The measurements shall be low pass filtered using a filter with 3 dB cutoff frequency that is 60 times the modulation rate. The filter stopband rejection shall be greater or equal to a second order low-pass of 20 dB per decade. Evaluation of the maximum df/dt is achieved by inspection of the low-pass filtered waveform.

Figure 17 Table 6-18 of USB 3.2 Specification Version 1.0

Unit Interval (with SSC) Test

Test Conditions

Reference Clock
Clean Clock

Test Overview The purpose of this test is to verify that the SSC of the transmitter complies with the specification.

Test Procedure

1. Set up the stimulus for 2-cycle LFPS ping.
2. Default the scope.
3. Setup Function 1 as subtraction of Channel 1 and Channel 3.
4. Set horizontal scale to 2ns, position at 0.
5. Setup the Acquisition
   a. Select Sampling Mode as “Real Time”
   b. Set interpolation to OFF
   c. Sample rate to 40GSa/s
   d. 8M points
   e. Bandwidth to 12GHz
6. Set Sweep as AUTO
7. Ping the DUT until CP1 is attained.
8. Setup horizontal scale to 20us, position at 0.
9. Stop the acquisition and save the waveform.
10. Set ‘Unit Interval Measurement’ to ON.
11. Set ‘Measurement Trend’ to ON.
12. Measure Vmax of the measurement trend.
13. Measure Vmin of the measurement trend.
14. Measure Vaverage of the measurement trend.
15. Record the measurement result.

Expected / Observable Results The measurement results for Unit Interval must be within the conformance limit as specified in the USB 3.2 specification.

SSC Deviation Test, SSC Modulation Rate Test, SSC Slew Rate Test

Test Conditions

Reference Clock
SSC

Test Overview The purpose of this test is to verify that the SSC of the transmitter complies with the specification.

Test Procedure

1 Set up the stimulus for 2-cycle LFPS ping.
2 Default the scope.
3 Setup Function 1 as subtraction of Channel 1 and Channel 3.
4 Set horizontal scale to 2ns, position at 0.
5 Setup the Acquisition
   a Select Sampling Mode as “Real Time”
   b Set interpolation to OFF
   c Sample rate to 40GSa/s
   d 8M points
   e Bandwidth to 12GHz
6 Set Sweep as AUTO
7 Ping the DUT until CP1 is attained.
8 Setup horizontal scale to 20us, position at 0.
9 Set ‘Unit Interval Measurement’ to ON.
10 Set ‘Measurement Trend’ to ON for function 1.
11 Save the measurement in CSV format.
12 The CSV waveform is processed within a MATLAB script.
   a Perform a second-order low pass filter. Cut-off frequency is set as 60 times of the modulation rate, 1.98MHz.

b Measure the Vtop and Vbase for every SSC triangle profile, as shown in Figure 18.

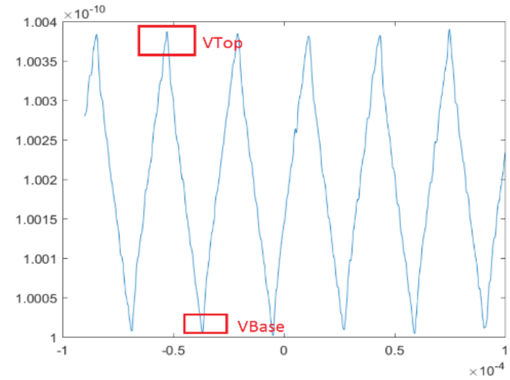


Figure 18 Vtop and Vbase measurements on an SCC triangle profile

c Measure the modulation rate, modulation rate is 1/tcycle. tcycle is defined as shown in Figure 19.

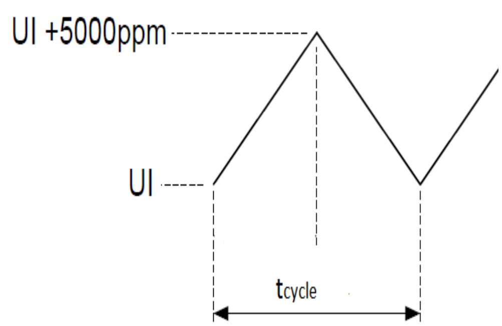


Figure 19 Measuring Modulation Rate

d Measure the Slew Rate of the SSC.

For the algorithm to determine the slew rate, refer to white paper USB 3.0 CDR Model White Paper, revision 0.5 available at “www.usb.org”.

13 Record the measurement result.

Expected / Observable Results

The measurement results for SSC must be within the conformance limit as specified in the USB 3.2 specification.

5G Transmitter Eye Far End (TP1) Tests

The 5G Transmitter Eye Far End (TP1) Tests include:

- 5G Far End Random Jitter
- 5G Far End Maximum Deterministic Jitter Test
- 5G Far End Total Jitter at BER- 12 Test
- 5G Far End Template Test
- 5G Far End Differential Output Voltage

This section provides the Methods of Implementation (MOIs) for 5G Transmitter Eye Far End (TP1) tests using a Keysight 90000A Series Infiniium oscilloscope, USB 3.0 test fixture, and USB3.2 Test Compliance Application.

Connection Diagram

See Appendix A, “Test Connection”.

Test Reference from the Specification

Table 6-16 and Table 6-20 (ECN for SSP System Jitter Budget) of the USB 3.2 Specification, revision 1.0.

Table 6-16. Informative Jitter Budgeting at the Silicon Pads[7]

Jitter Contribution (ps)	Gen 1 (5 GT/s)			Gen 2 (10 GT/s)		
	Rj[1,2]	Dj[3]	Tj[4] at 10^{-12}	Rj[1,2]	Dj[3]	Tj[4] at 10^{-12}
Tx[6]	2.42	41	75	1.00	17	31.1
Media[5]	2.13	45	75	0.00	36	36.0
Rx	2.42	57	91	1.00	27.1	41.2
Total	4.03	143	200	1.41	80.1	100

Notes:

1. Rj is the sigma value assuming a Gaussian distribution.
2. Rj Total is computed as the Root Sum Square of the individual Rj components.
3. Dj budget is using the Dual Dirac method.
4. Tj at a 10^{-12} BER is calculated as 14.068 * Rj + Dj.
5. The media budget includes the cancellation of ISI from the appropriate Rx equalization function.
6. Tx is measured after application of the JTF.
7. In this table, Tx jitter is defined at TP1, Rx jitter is defined at TP4, and media jitter is defined from TP1 to TP4.

Figure 20 Table 6-16 of USB 3.2 Specification Version 1.0

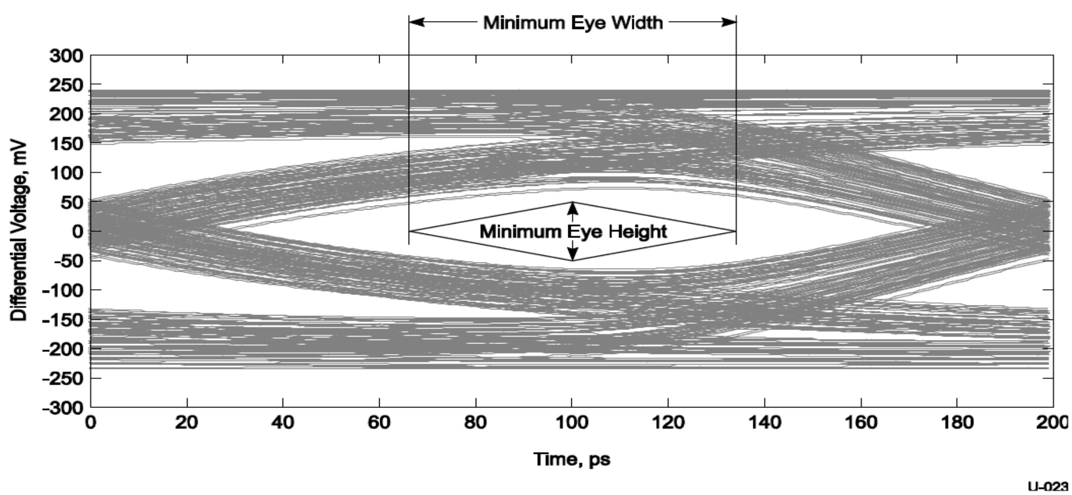
Table 6-20. Normative Transmitter Eye Mask at Test Point TP4

Signal Characteristic	5GT/s		10GT/s		Units	Note
	Minimum	Maximum	Minimum	Maximum		
Eye Height	100	1200	70	1200	mV	2, 3, 4
Dj		0.43		0.530	UI	1, 2, 3
Rj		0.23		0.141	UI	1, 5, 6
Tj		0.66		0.671	UI	1, 2, 3

Notes:

1. Measured over 10^6 consecutive UI and extrapolated to 10^{-12} BER.
2. Measured after receiver equalization function.
3. Measured at end of reference channel and cables at TP4 in Figure 6-20.
4. The eye height is to be measured at the minimum opening over the range from the center of the eye ± 0.05 UI.
5. The Rj specification is calculated as 14.069 times the RMS random jitter for 10^{-12} BER.
6. Measured at the output of the compliance breakout board without embedding the compliance cable and load board.

Figure 21 Table 6-20 of USB 3.2 Specification Version 1.0



Gen 1 eye mask

Figure 22 Gen 1 Eye Mask for 5G Transmitter Far End Eye (TP1) tests

5G Far End Random Jitter Test

Test Overview The purpose of this test is to verify that the Random Jitter of the transmitter complies with the specification.

Test Procedure

1 Set up the stimulus for 2-cycle LFPS ping.
2 Default the scope.
3 Setup Function 1 as subtraction of Channel 1 and Channel 3.
4 Set horizontal scale to 2ns, position at 0.
5 Ping the DUT until CP1 is attained.
6 Setup the Acquisition
   a Select Sampling Mode as “Real Time”
   b Set interpolation to OFF
   c Sample rate to 40GSa/s
   d 8M points
   e Bandwidth to 12GHz
7 Set Sweep as AUTO.
8 Setup horizontal scale to 20us, position at 0.
9 Stop the acquisition and save the waveform in binary format.
10 Launch SigTest tool.
11 Load the waveform file. Select the options for Technology and Template File as shown in Figure 23.
   a Test Mode set to ‘CEM’
   b Technology set to ‘USB_3_5gb’
   c Template File set to ‘USB_3_5Gb_CP1’

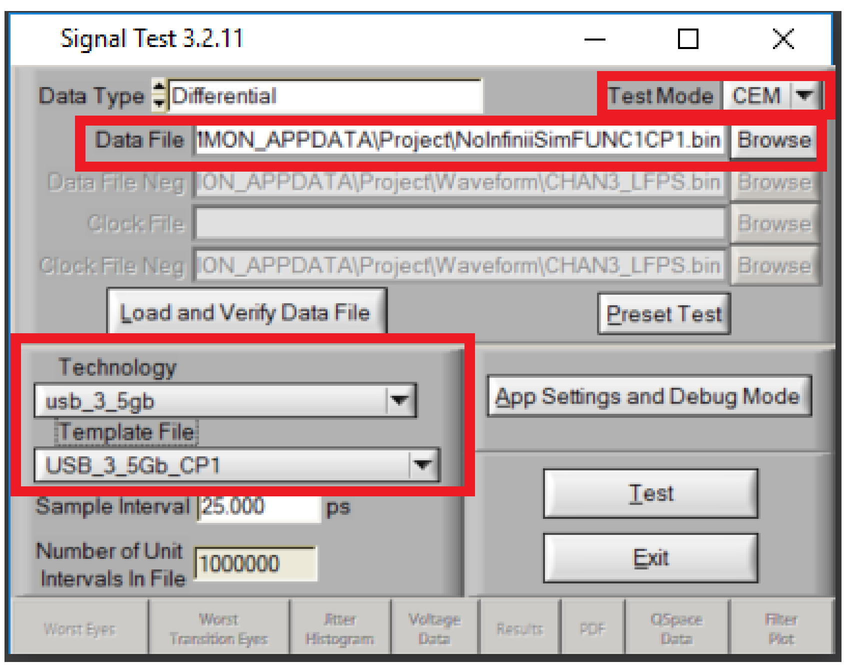


Figure 23 SigTest tool settings for measuring RJ

12 Record the measurement result for RJ.

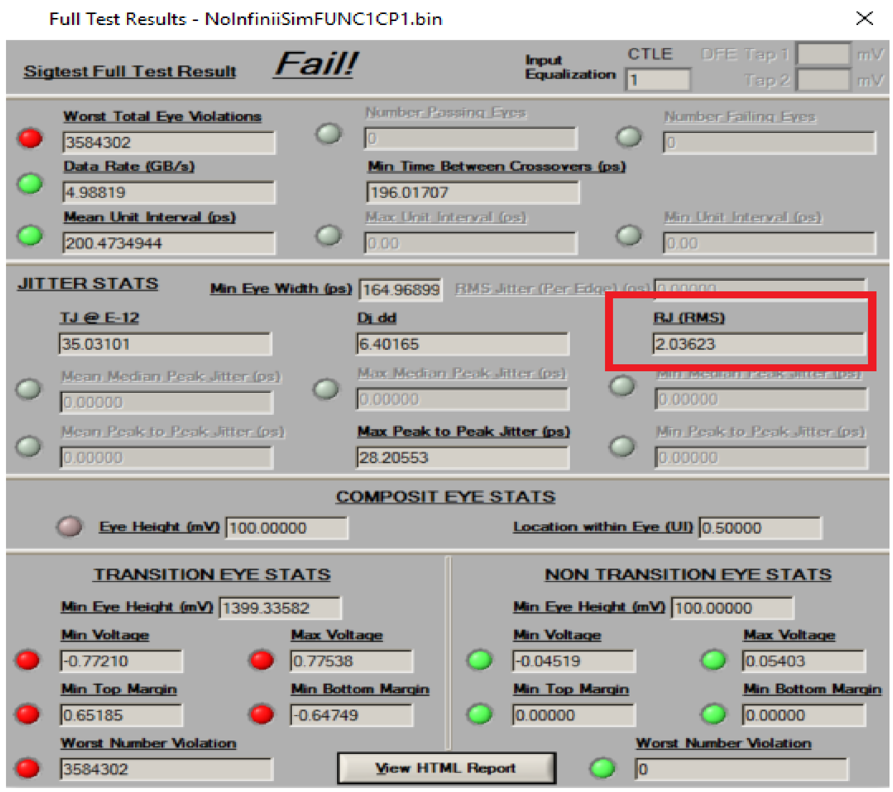


Figure 24 SigTest tool report for RJ measurement

Expected / Observable Results

The measurement results for Random Jitter must be within the conformance limit as specified in the USB 3.2 specification.

Test Condition

Test Method
SDA

Test Procedure

1 Set up the stimulus for 2-cycle LFPS ping.
2 Default the scope.
3 Setup Function 1 as subtraction of Channel 1 and Channel 3.
4 Set horizontal scale to 2ns, position at 0.
5 Ping the DUT until CP1 is attained.
6 Setup the Acquisition
   a Select Sampling Mode as “Real Time”
   b Set interpolation to OFF
   c Sample rate to 40GSa/s
   d 8M points
   e Bandwidth to 12GHz
7 Set Sweep as AUTO
8 Setup horizontal scale to 20us, position at 0.
9 Stop the acquisition and save the waveform.

10 Setup CTLE:
   a # of Poles: 2
   b Pole 1 Frequency: 1.95GHz
   c Pole 2 Frequency: 5.0GHz
   d Zero Frequency: 650MHz
   e DC Gain: 0.667
11 Setup Clock Recovery:
   2nd order PLL, data rate of 5Gbps, loop bandwidth of 4.9MHz, damping factor of 0.707
12 Setup EZJIT Complete:
   a Set CTLE as source
   b Enable Jitter Mode on EZJIT+
   c BER Level: 1E-12
   d Measurement: TIE (Phase)
   e Edges: Both
   f RJ Bandwidth: Narrow
   g RJ Method: Spectral Only
   h Pattern Length: Periodic, Auto
13 Obtain RJ reading.

Expected / Observable Results The measurement results for Random Jitter must be within the conformance limit as specified in the USB 3.2 specification.

5G Far End Maximum Deterministic Jitter, 5G Far End Total Jitter At BER-12, 5G Far End Template Test, 5G Far End Differential Output Voltage Test

Test Overview The purpose of this test is to verify that the Far End Maximum Deterministic Jitter, Far End Total Jitter At BER-12, Far End Template Test and Far End Differential Output Voltage of the transmitter complies with the specification.

Test Condition

Test Method
USB-IF SigTest

Test Procedure

1 Set up the stimulus for 2-cycle LFPS ping.
2 Default the scope.
3 Setup Function 1 as subtraction of Channel 1 and Channel 3.
4 Set horizontal scale to 2ns, position at 0.
5 Ping the DUT until CP0 is attained.
6 Setup the Acquisition
   a Select Sampling Mode as “Real Time”
   b Set interpolation to OFF
   c Sample rate to 40GSa/s
   d 8M points
   e Bandwidth to 12GHz
7 Setup InfiniiSim. See Appendix A, “InfiniiSim Setup for 5G” for settings.
8 Set Sweep as AUTO.
9 Setup horizontal scale to 20us, position at 0.
10 Stop the acquisition and save the waveform in binary format.
11 Launch SigTest tool.
12 Load the waveform file. Select the options for Technology and Template File as shown in Figure 25.
   a Test Mode set to ‘CEM’
   b Technology set to ‘USB_3_5gb’
   c Template File set to ‘USB_3_5Gb_CP0_RjIN’
   d Set Random Jitter

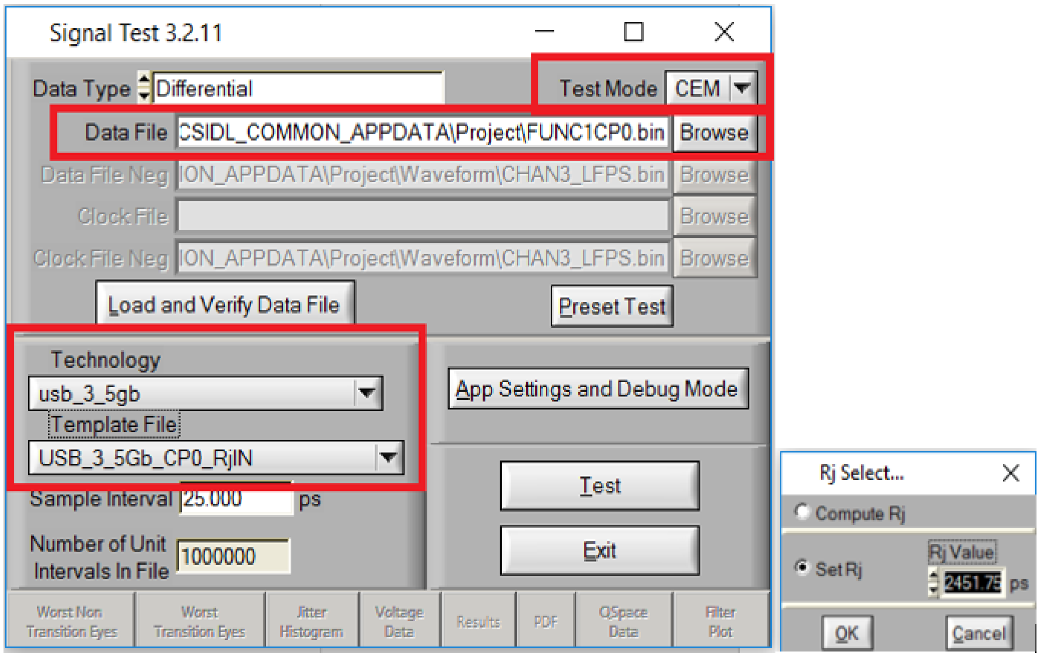


Figure 25 SigTest tool settings for measuring DJ, TJ and Eye Height

13 Record the measurement result for DJ, TJ and Eye Height.

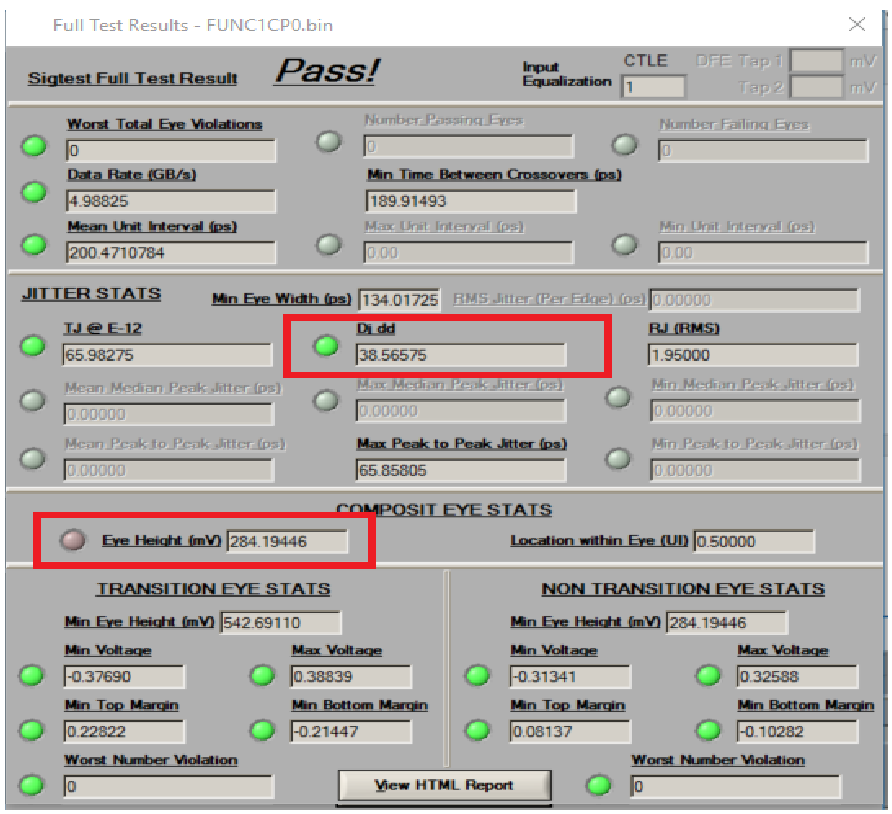


Figure 26 SigTest tool report for DJ, TJ and Eye Height measurement

Expected / Observable Results The measurement results for Deterministic Jitter, Total Jitter and Eye Height must be within the conformance limit as specified in the USB 3.2 specification.

5G Far End Maximum Deterministic Jitter and 5G Far End Total Jitter At BER-12 Test

Test Condition

Test Method
SDA

Test Procedure

1 Set up the stimulus for 2-cycle LFPS ping.
2 Default the scope.
3 Setup Function 1 as subtraction of Channel 1 and Channel 3.
4 Set horizontal scale to 2ns, position at 0.
5 Ping the DUT until CP0 is attained.
6 Setup the Acquisition
   a Select Sampling Mode as “Real Time”
   b Set interpolation to OFF
   c Sample rate to 40GSa/s
   d 8M points
7 Setup InfiniiSim. See Appendix A, “InfiniiSim Setup for 5G” for settings.
8 Set Sweep as AUTO.
9 Setup horizontal scale to 20us, position at 0.
10 Stop the acquisition and save the waveform in binary format.
11 Setup CTLE:
   a # of Poles: 2
   b Pole 1 Frequency: 1.95GHz
   c Pole 2 Frequency: 5.0GHz
   d Zero Frequency: 650MHz
   e DC Gain: 0.667
12 Setup Clock Recovery:
   2nd order PLL, data rate of 5Gbps, loop bandwidth of 4.9MHz, damping factor of 0.707
13 Setup EZJIT Complete:
   a Set CTLE as source
   b Enable Jitter Mode on EZJIT+
   c BER Level: 1E-12
   d Measurement: TIE (Phase)
   e Edges: Both
   f RJ Bandwidth: Narrow
   g RJ Method: Spectral Only
   h Pattern Length: Arbitrary
   i ISI Filter Lead: -2
   j ISI Filter Lag: 18

Expected / Observable Results

The measurement results for Total Jitter, Deterministic Jitter, Eye Width and Extrapolated Eye Height must be within the conformance limit as specified in the USB 3.2 specification.

5G Far End Template Test and 5G Far End Differential Output Voltage Test

Test Condition

Test Method
SDA

Test Procedure

1 Set up the stimulus for 2-cycle LFPS ping.
2 Default the scope.
3 Setup Function 1 as subtraction of Channel 1 and Channel 3.
4 Set horizontal scale to 2ns, position at 0.
5 Ping the DUT until CP0 is attained.
6 Setup the Acquisition
   a Select Sampling Mode as “Real Time”
   b Set interpolation to OFF
   c Sample rate to 40GSa/s
   d 8M points
7 Setup InfiniiSim. See Appendix A, “InfiniiSim Setup for 5G” for settings.
8 Set Sweep as AUTO.
9 Setup horizontal scale to 20us, position at 0.
10 Stop the acquisition and save the waveform.
11 Setup CTLE:
   a # of Poles: 2
   b Pole 1 Frequency: 1.95GHz
   c Pole 2 Frequency: 5.0GHz
   d Zero Frequency: 650MHz
   e DC Gain: 0.667
12 Setup Clock Recovery:
   2nd order PLL, data rate of 5Gbps, loop bandwidth of 4.9MHz, damping factor of 0.707
13 Enable Mask Test:
   a Load Mask
   b Set Source as CTLE
   c Set Color Grade to ON
   d Set Infinite Persistent to ON
   e Set Mask Scaling:
   - Horizontal Scaling: -100ps
   - Delta: 200ps
   f Set Mask Vertical Scaling:
   - 1 Level: 600mV
   - 0 Level: -600mV
   g Enable “Bind 1 & 0 Levels”
   h Enable “Real-Time Eye”
14 Run Mask Test.
15 Measure Eye Height and Eye Width.

Expected / Observable Results

The signal must pass the Mask Test and the Differential Output Voltage must be within the conformance limits as specified in the USB 3.2 specification.

5G Transmitter Eye Short Channel Tests

The 5G Transmitter Eye Short Channel Tests include:

- 5G Short Channel Random Jitter
- 5G Short Channel Maximum Deterministic Jitter Test
- 5G Short Channel Total Jitter at BER- 12 Test
- 5G Short Channel Template Test
- 5G Short Channel Differential Output Voltage

This section provides the Methods of Implementation (MOIs) for 5G Transmitter Eye Short Channel tests using a Keysight 90000A Series Infiniium oscilloscope, USB 3.0 test fixture, and USB3.2 Test Compliance Application.

Connection Diagram See Appendix A, “Test Connection”.

Test Reference from the Specification Table 6-16 and Table 6-20 (ECN for SSP System Jitter Budget) of the USB 3.2 Specification, revision 1.0.

Table 6-16. Informative Jitter Budgeting at the Silicon Pads[7]

Jitter Contribution (ps)	Gen 1 (5 GT/s)			Gen 2 (10 GT/s)		
	Rj[1,2]	Dj[3]	Tj[4] at 10^{-12}	Rj[1,2]	Dj[3]	Tj[4] at 10^{-12}
Tx[6]	2.42	41	75	1.00	17	31.1
Media[5]	2.13	45	75	0.00	36	36.0
Rx	2.42	57	91	1.00	27.1	41.2
Total	4.03	143	200	1.41	80.1	100

Notes:

1. Rj is the sigma value assuming a Gaussian distribution.
2. Rj Total is computed as the Root Sum Square of the individual Rj components.
3. Dj budget is using the Dual Dirac method.
4. Tj at a 10^{-12} BER is calculated as 14.068 * Rj + Dj.
5. The media budget includes the cancellation of ISI from the appropriate Rx equalization function.
6. Tx is measured after application of the JTF.
7. In this table, Tx jitter is defined at TP1, Rx jitter is defined at TP4, and media jitter is defined from TP1 to TP4.

Figure 27 Table 6-16 of USB 3.2 Specification Version 1.0

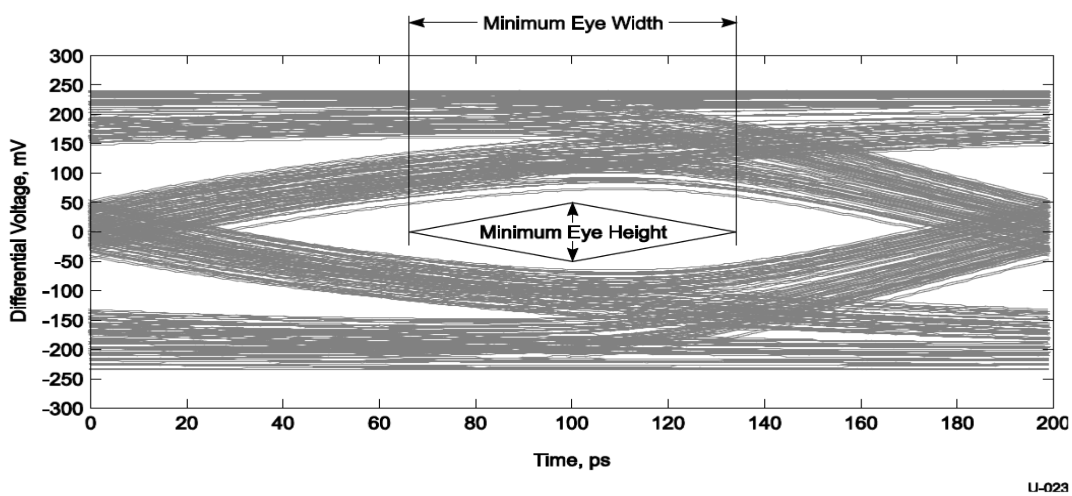
Table 6-20. Normative Transmitter Eye Mask at Test Point TP4

Signal Characteristic	5GT/s		10GT/s		Units	Note
	Minimum	Maximum	Minimum	Maximum		
Eye Height	100	1200	70	1200	mV	2, 3, 4
Dj		0.43		0.530	UI	1, 2, 3
Rj		0.23		0.141	UI	1, 5, 6
Tj		0.66		0.671	UI	1, 2, 3

Notes:

1. Measured over 10^{6} consecutive UI and extrapolated to 10^{-12} BER.
2. Measured after receiver equalization function.
3. Measured at end of reference channel and cables at TP4 in Figure 6-20.
4. The eye height is to be measured at the minimum opening over the range from the center of the eye ± 0.05 UI.
5. The Rj specification is calculated as 14.069 times the RMS random jitter for 10^{-12} BER.
6. Measured at the output of the compliance breakout board without embedding the compliance cable and load board.

Figure 28 Table 6-20 of USB 3.2 Specification Version 1.0



Gen 1 eye mask

Figure 29 Gen 1 Eye Mask for 5G Transmitter Short Channel tests

5G Short Channel Random Jitter Test

Test Condition

Test Method
USB-IF SigTest

Test Overview

The purpose of this test is to verify that the Short Channel Random Jitter of the transmitter complies with the specification.

Test Procedure

1 Set up the stimulus for 2-cycle LFPS ping.
2 Default the scope.
3 Setup Function 1 as subtraction of Channel 1 and Channel 3.
4 Set horizontal scale to 2ns, position at 0.
5 Ping the DUT until CP1 is attained.
6 Setup the Acquisition
   a Select Sampling Mode as “Real Time”
   b Set interpolation to OFF
   c Sample rate to 40GSa/s
   d 8M points
   e Bandwidth to 12GHz
7 Set Sweep as AUTO.
8 Setup horizontal scale to 20us, position at 0.
9 Stop the acquisition and save the waveform in binary format.
10 Launch SigTest tool.
11 Load the waveform file. Select the options for Technology and Template File as shown in Figure 30.
   a Test Mode set to ‘CEM’
   b Technology set to ‘USB_3_5gb’
   c Template File set to ‘USB_3_5Gb_CP1_SHORT’

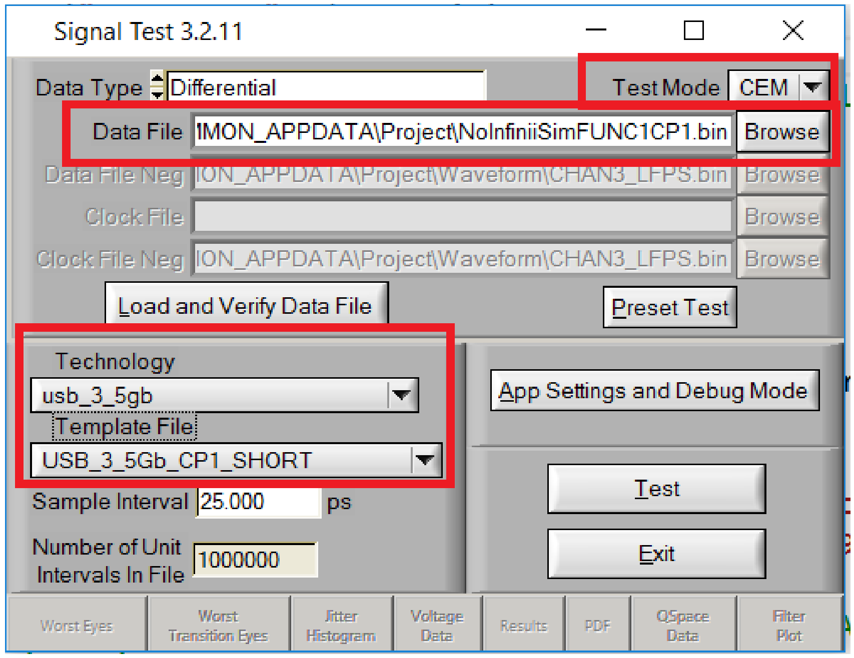


Figure 30 SigTest tool settings for measuring Short Channel RJ

12 Record the measurement result for Short Channel RJ.

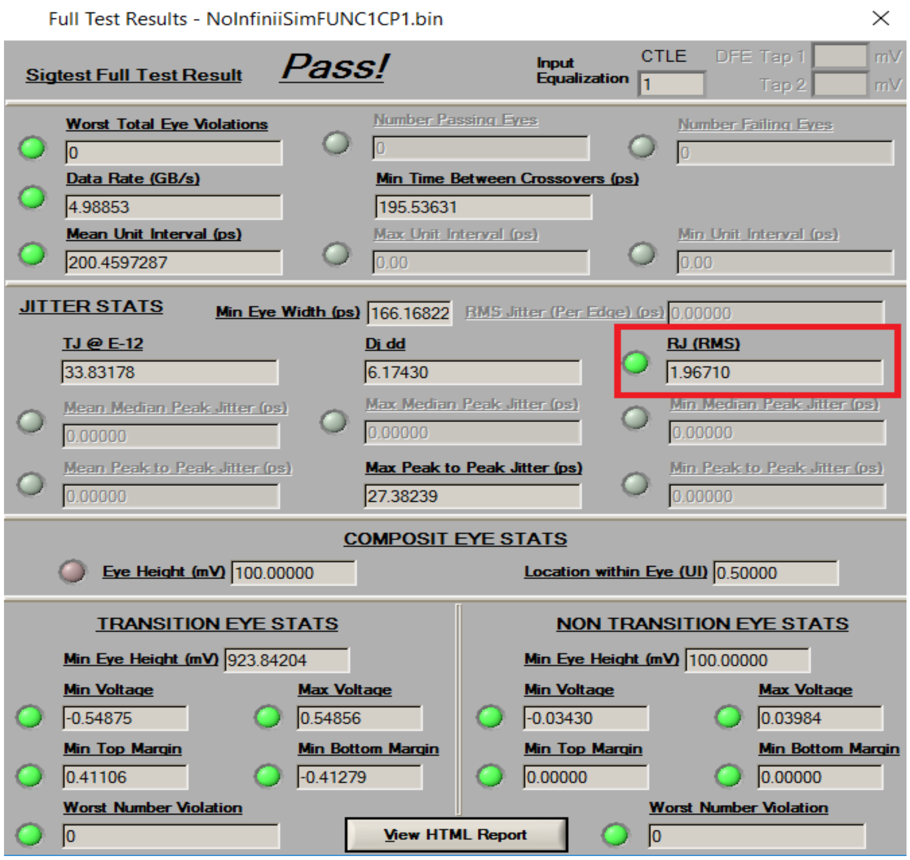


Figure 31 SigTest tool report for Short Channel RJ measurement

Expected / Observable Results

The measurement results for Short Channel Random Jitter must be within the conformance limit as specified in the USB 3.2 specification.

5G Short Channel Maximum Deterministic Jitter, 5G Short Channel Total Jitter At BER- 12, 5G Short Channel Template Test and 5G Short Channel Differential Output Voltage

Test Conditions

Test Method
USB-IF SigTest

Test Procedure

1 Set up the stimulus for 2-cycle LFPS ping.
2 Default the scope.
3 Setup Function 1 as subtraction of Channel 1 and Channel 3.
4 Set horizontal scale to 2ns, position at 0.
5 Ping the DUT until CP0 is attained.
6 Setup the Acquisition
   a Select Sampling Mode as “Real Time”
   b Set interpolation to OFF
   c Sample rate to 40GSa/s
   d 8M points
   e Bandwidth to 12GHz
7 Set Sweep as AUTO
8 Setup horizontal scale to 20us, position at 0.
9 Stop the acquisition and save the waveform in binary format.
10 Launch SigTest tool.
11 Load the waveform file. Select the options for Technology and Template File as shown in Figure 32.
   a Test Mode set to ‘CEM’
   b Technology set to ‘USB_3_5gb’
   c Template File set to ‘USB_3_5Gb_CP0_RjIN_SHORT’
   d Set Random Jitter

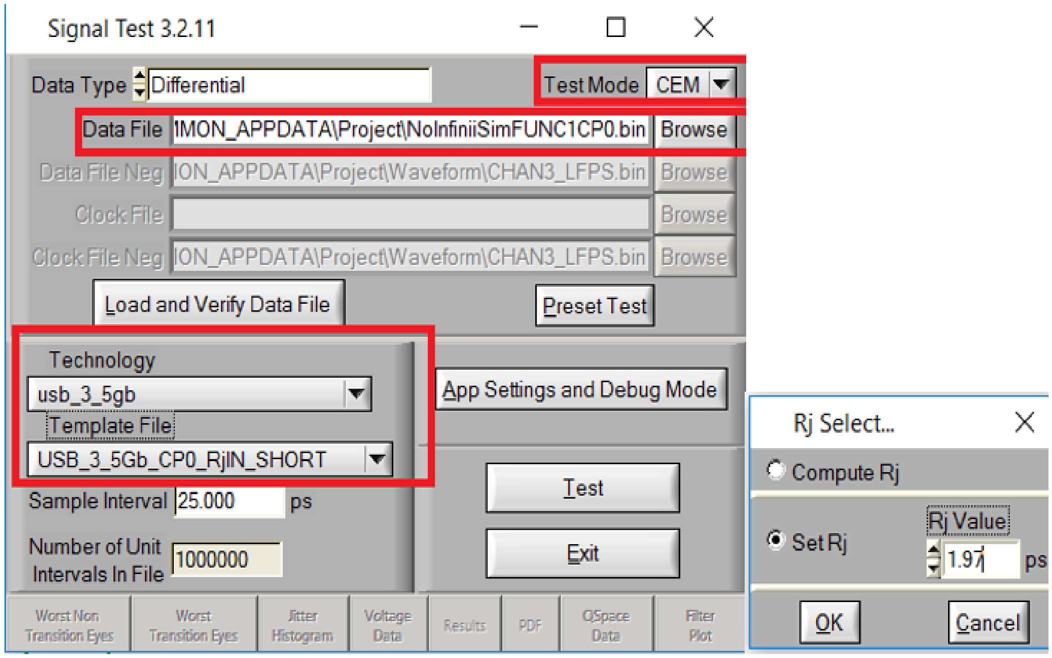


Figure 32 SigTest tool settings for measuring DJ, TJ and Eye Height

12 Record the measurement result for DJ, TJ, and Eye Height.

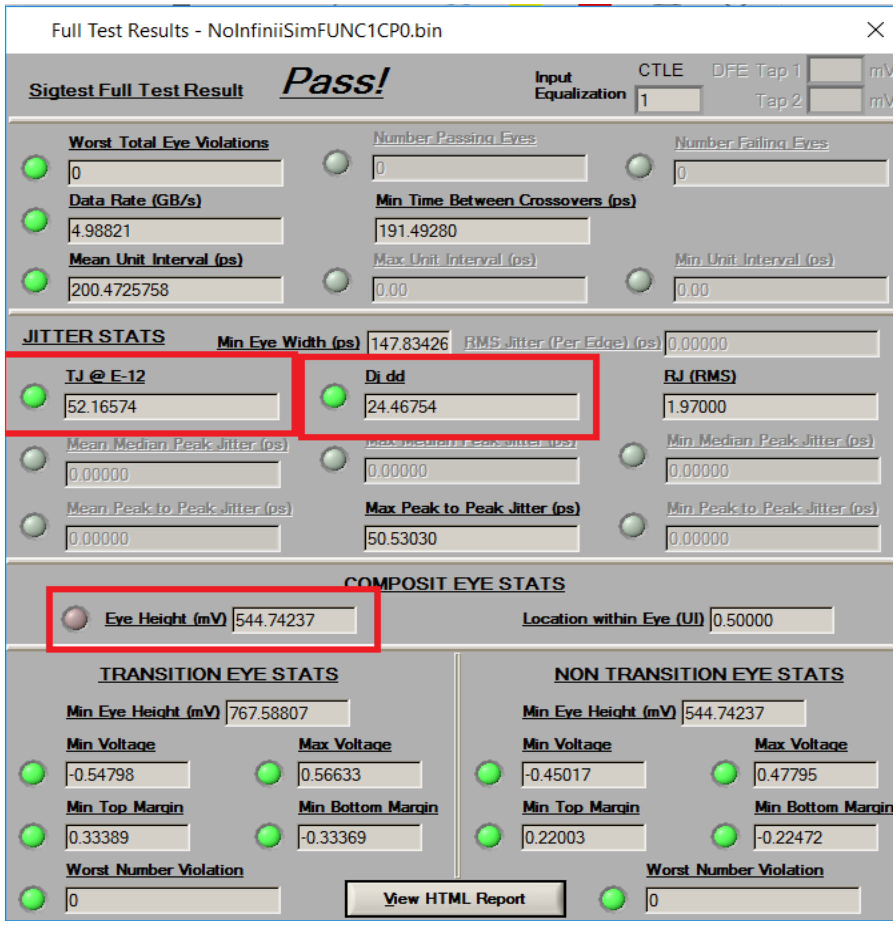


Figure 33 SigTest tool report for Short Channel DJ, TJ and Eye Height measurement

Expected / Observable Results

The measurement results for Short Channel Deterministic Jitter, Total Jitter and Eye Height must be within the conformance limit as specified in the USB 3.2 specification.

5G Transmitter Eye Near End Tests

The 5G Transmitter Eye Near End Tests include:

- 5G Near End Random Jitter
- 5G Near End Maximum Deterministic Jitter Test
- 5G Near End Total Jitter at BER- 12 Test
- 5G Near End Template Test
- 5G Near End Differential Output Voltage

This section provides the Methods of Implementation (MOIs) for 5G Transmitter Eye Near End tests using a Keysight 90000A Series Infiniium oscilloscope, USB 3.0 test fixture, and USB3.2 Test Compliance Application.

Connection Diagram

See Appendix A, “Test Connection”.

Test Reference from the Specification

Table 6-16 (ECN for SSP System Jitter Budget) of the USB 3.2 Specification, revision 1.0.

Table 6-16. Informative Jitter Budgeting at the Silicon Pads[7]

Jitter Contribution (ps)	Gen 1 (5 GT/s)			Gen 2 (10 GT/s)		
	Rj[1,2]	Dj[3]	Tj[4] at 10^{-12}	Rj[1,2]	Dj[3]	Tj[4] at 10^{-12}
Tx[6]	2.42	41	75	1.00	17	31.1
Media[5]	2.13	45	75	0.00	36	36.0
Rx	2.42	57	91	1.00	27.1	41.2
Total	4.03	143	200	1.41	80.1	100

Notes:

1. Rj is the sigma value assuming a Gaussian distribution.
2. Rj Total is computed as the Root Sum Square of the individual Rj components.
3. Dj budget is using the Dual Dirac method.
4. Tj at a 10^{-12} BER is calculated as 14.068 * Rj + Dj.
5. The media budget includes the cancellation of ISI from the appropriate Rx equalization function.
6. Tx is measured after application of the JTF.
7. In this table, Tx jitter is defined at TP1, Rx jitter is defined at TP4, and media jitter is defined from TP1 to TP4.

Figure 34 Table 6-16 of USB 3.2 Specification Version 1.0

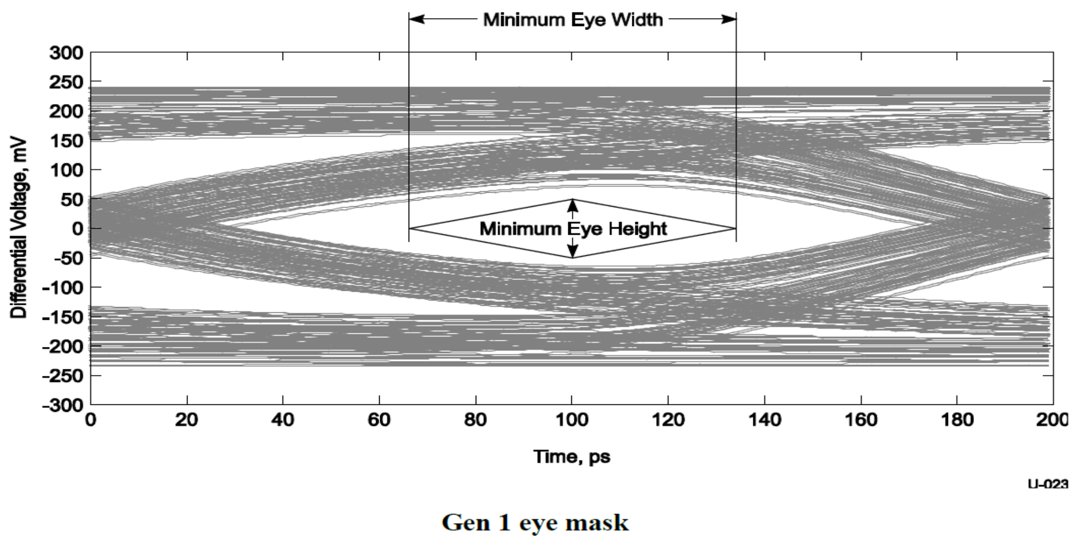


Figure 35 Gen 1 Eye Mask for 5G Transmitter Near End tests

5G Near End Random Jitter Test

Test Overview

The purpose of this test is to verify that the Near End Random Jitter of the transmitter complies with the specification.

Test Condition

Test Method
SDA

Test Procedure

1. Set up the stimulus for 2-cycle LFPS ping.
2. Default the scope.
3. Setup Function 1 as subtraction of Channel 1 and Channel 3.
4. Set horizontal scale to 2ns, position at 0.
5. Ping the DUT until CP1 is attained.
6. Setup the Acquisition
   - *a* Select Sampling Mode as “Real Time”
   - *b* Set interpolation to OFF
   - *c* Sample rate to 40GSa/s
   - *d* 8M points
   - *e* Bandwidth to 12GHz
7. Set Sweep as AUTO
8. Setup horizontal scale to 20us, position at 0.
9. Stop the acquisition and save the waveform.
10. Setup Clock Recovery:
    2nd order PLL, data rate of 5Gbps, loop bandwidth of 4.9MHz, damping factor of 0.707
11. Setup EZJIT Complete:
    - *a* Set FUNC1 as source
    - *b* Enable Jitter Mode on EZJIT+
    - *c* BER Level: 1E-12
    - *d* Measurement: TIE (Phase)
    - *e* Edges: Both
    - *f* RJ Bandwidth: Narrow
    - *g* RJ Method: Spectral Only
    - *h* Pattern Length: Periodic, Auto
12. Obtain Near End RJ reading.

Expected / Observable Results

The measurement results for Near End Random Jitter must be within the conformance limit as specified in the USB 3.2 specification.

5G Near End Maximum Deterministic Jitter and 5G Near End Total Jitter At BER-6 Test

Test Condition

Test Method
SDA

Test Procedure

1 Set up the stimulus for 2-cycle LFPS ping.
2 Default the scope.
3 Setup Function 1 as subtraction of Channel 1 and Channel 3.
4 Set horizontal scale to 2ns, position at 0.
5 Ping the DUT until CP0 is attained.
6 Setup the Acquisition
   a Select Sampling Mode as “Real Time”
   b Set interpolation to OFF
   c Sample rate to 40GSa/s
   d 8M points
7 Set Sweep as AUTO.
8 Setup horizontal scale to 20us, position at 0.
9 Stop the acquisition and save the waveform.
10 Setup Clock Recovery:
   2nd order PLL, data rate of 5Gbps, loop bandwidth of 4.9MHz, damping factor of 0.707
11 Setup EZJIT Complete:
   a Set FUNC1 as source
   b Enable Jitter Mode on EZJIT+
   c BER Level: 1E-12
   d Measurement: TIE (Phase)
   e Edges: Both
   f RJ Bandwidth: Narrow
   g RJ Method: Spectral Only
   h Pattern Length: Arbitrary
   i ISI Filter Lead: -2
   j ISI Filter Lag: 18

Expected / Observable Results

The measurement results for Total Jitter, Deterministic Jitter, Eye Width and Eye Height must be within the conformance limit as specified in the USB 3.2 specification.

5G Near End Template Test and 5G Near End Differential Output Voltage Test

Test Condition

Test Method
SDA

Test Procedure

1 Set up the stimulus for 2-cycle LFPS ping.
2 Default the scope.
3 Setup Function 1 as subtraction of Channel 1 and Channel 3.
4 Set horizontal scale to 2ns, position at 0.
5 Ping the DUT until CP0 is attained.
6 Setup the Acquisition
   a Select Sampling Mode as “Real Time”
   b Set interpolation to OFF
   c Sample rate to 40GSa/s
   d 8M points
7 Setup InfiniiSim. See Appendix A, “InfiniiSim Setup for 5G” for settings.
8 Set Sweep as AUTO.
9 Setup horizontal scale to 20us, position at 0.
10 Stop the acquisition and save the waveform.
11 Setup Clock Recovery:
   2nd order PLL, data rate of 5Gbps, loop bandwidth of 4.9MHz, damping factor of 0.707
12 Enable Mask Test:
   a Load Mask
   b Set Source as FUNC1
   c Set Color Grade to ON
   d Set Infinite Persistent to ON
   e Set Mask Scaling:
   - Horizontal Scaling: -100ps
   - Delta: 200ps
   f Set Mask Vertical Scaling:
   - 1 Level: 600mV
   - 0 Level: -600mV
   g Enable “Bind 1 & 0 Levels”
   h Enable “Real-Time Eye”
13 Run Mask Test.
14 Measure Eye Height and Eye Width.

Expected / Observable Results

The signal must pass the Mask Test and the Differential Output Voltage must be within the conformance limits as specified in the USB 3.2 specification.

5G BLR Clock Switch Test

The 5G BLR Clock Switch Test includes:

- 5G SSC df/dt

This section provides the Methods of Implementation (MOIs) for Clock Switch test using a Keysight 90000A Series Infiniium oscilloscope, USB 3.0 test fixture, and USB3.2 Compliance Test Application.

Connection Diagram See Appendix A, “Test Connection”.

Test Reference from the Specification USB 3.2 Specification, Rev 1.0, Section 6.7.1, Table 6-18

Table 6-18. Transmitter Normative Electrical Parameters

Symbol	Parameter	Gen 1 (5.0 GT/s)	Gen 2 (10 GT/s)	Units	Comments
UI	Unit Interval	199.94 (min) 200.06 (max)	99.97 (min) 100.03 (max)	ps	The specified UI is equivalent to a tolerance of ±300 ppm for each device. Period does not account for SSC induced variations.
		200.34 (min) 200.46 (max)	100.17 (min) 100.23 (max)	ps	Alternate limits apply to "radio friendly" clocking mode which employs a clock whose center frequency is downshifted by 2000ppm. This mode is to be used with a +0/-3000ppm spread.
$V_{TX-DIFF-PP}$	Differential p-p Tx voltage swing	0.8 (min) 1.2 (max)	0.8 (min) 1.2 (max)	V	Nominal is 1 V p-p
$V_{TX-DIFF-PP-LOW}$	Low-Power Differential p-p Tx voltage swing	0.4 (min) 1.2 (max)	0.4 (min) 1.2 (max)	V	Refer to Section 6.7.2. There is no de-emphasis requirement in this mode. De-emphasis is implementation specific for this mode.
$V_{TX-DE-RATIO}$	Tx de-emphasis	3.0 (min) 4.0 (max)	See section 6.7.5.2.	dB	Nominal is 3.5 dB for Gen 1 operation. Gen 2 transmitter equalization requirements are described in section 6.7.5.2.
$R_{TX-DIFF-DC}$	DC differential impedance	72 (min) 120 (max)	72 (min) 120 (max)	Ω	
$V_{TX-RCV-DETECT}$	The amount of voltage change allowed during Receiver Detection	0.6 (max)	0.6 (max)	V	Detect voltage transition should be an increase in voltage on the pin looking at the detect signal to avoid a high impedance requirement when an "off" receiver's input goes below ground.
$C_{AC-COUPLING}$	AC Coupling Capacitor	75 (min) 265 (max)	75 (min) 265 (max)	nF	All Transmitters shall be AC coupled. The AC coupling is required either within the media or within the transmitting component itself.
$t_{CDR\_SLEW\_MAX}$	Maximum slew rate	10	Not applicable	ms/s	See the jitter white paper for details on this measurement. This is a df/ft specification; refer to Section 6.5.4 for details.
SSC_{dfdt}	SSC df/dt	Not applicable	1250 (max)	ppm/µs	See note 1.
$V_{Tx-CM-IDLE-DELTA}$	Transmitter idle common-mode voltage change	+600 (max) -600 (min)	+600 (max) -600 (min)	mV	The maximum allowed instantaneous common-mode voltage at TP2 while the transmitter is in U2 or U3 and not actively transmitting LFPS. Note that this is an absolute voltage spec referenced to the receive-side termination ground but serves the purpose of limiting the magnitude and/or slew rate of Tx common mode changes.

Note 1: Measured over a 0.5µs interval using CP10. The measurements shall be low pass filtered using a filter with 3 dB cutoff frequency that is 60 times the modulation rate. The filter stopband rejection shall be greater or equal to a second order low-pass of 20 dB per decade. Evaluation of the maximum df/dt is achieved by inspection of the low-pass filtered waveform.

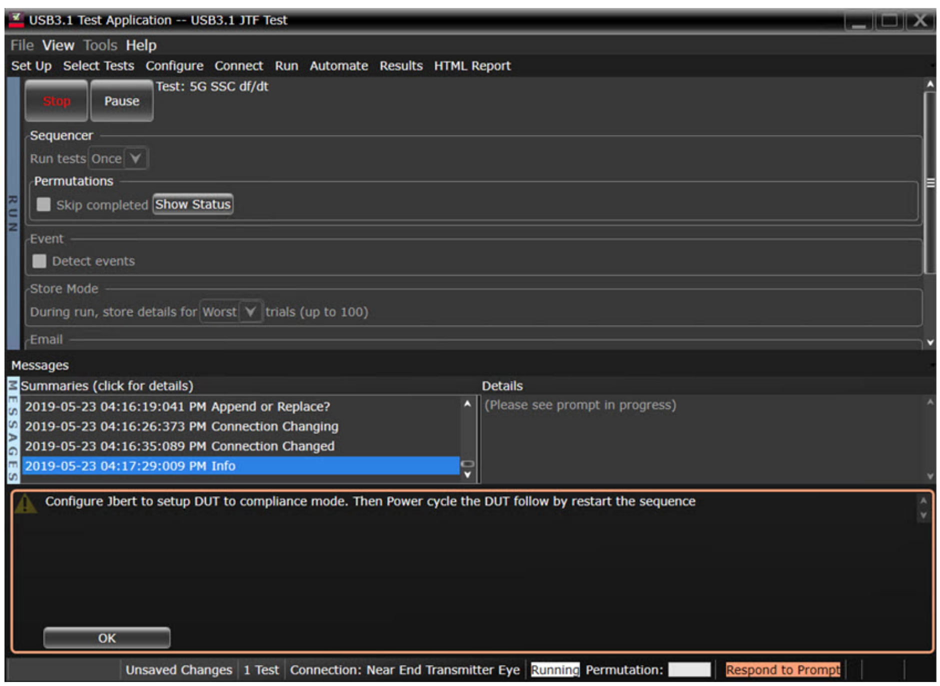
Figure 36 Table 6-18 of USB 3.2 Specification Rev 1.0

Test Conditions This test is applicable to only **5G** data rate and **BLR** retimer mode.

Test Overview The purpose of this test is to verify that the measured SSC deviation is within the conformance limits specified in Table 6-18 of the USB 3.2 Specification.

Test Procedure

1 Set up M8020A
2 Set the scope to default setting
3 Setup Function 1 as subtraction of Channel 1 and Channel 3
4 Set horizontal scale to 50 µs, positioned at -50 µs
5 Setup the acquisition
6 Setup triggers on channel 4 to detect clock switch event
7 Verify that clock switch event is being captured before clicking **OK** to the prompt. User can load a customized JBERT sequence for the DUT during this prompt.



8 Click **OK** to proceed with the clock switch test, the application will capture waveform and process by Matlab script.

Expected / Observable Results The measurement results for 5G SSC df/dt test must be within the conformance limit as specified in the USB 3.2 specification.

5G Jitter Transfer Function Test

The 5G Jitter Transfer Function Test includes:

- 5G JTF

This section provides the Methods of Implementation (MOIs) for 5G Jitter Transfer Function Test using a Keysight 90000A Series Infiniium oscilloscope, USB 3.0 test fixture, and USB3.2 Test Compliance Application.

Connection Diagram See Appendix A, "Test Connection".

Test Reference from the Specification USB 3.2 Specification, Rev 1.0, Appendix E.5, Table E-3

Table E-3. Bit-Level Re-timer Jitter Transfer Function Requirements

Term	Gen 1x1	Notes
Jitter Gain for f<500kHz	0.1dB (max)	Normative requirement.
Jitter Gain for f>500kHz	0.0dB (max)	Normative requirement.
Term	**Gen 1x1**	**Notes**
JSF 3dB frequency	2MHz (max)	Overall JTF is expected to meet a −20 dB/decade slope above the JSF 3 dB frequency.

Figure 37 Table E-3 of USB 3.2 Specification Revision 1.0

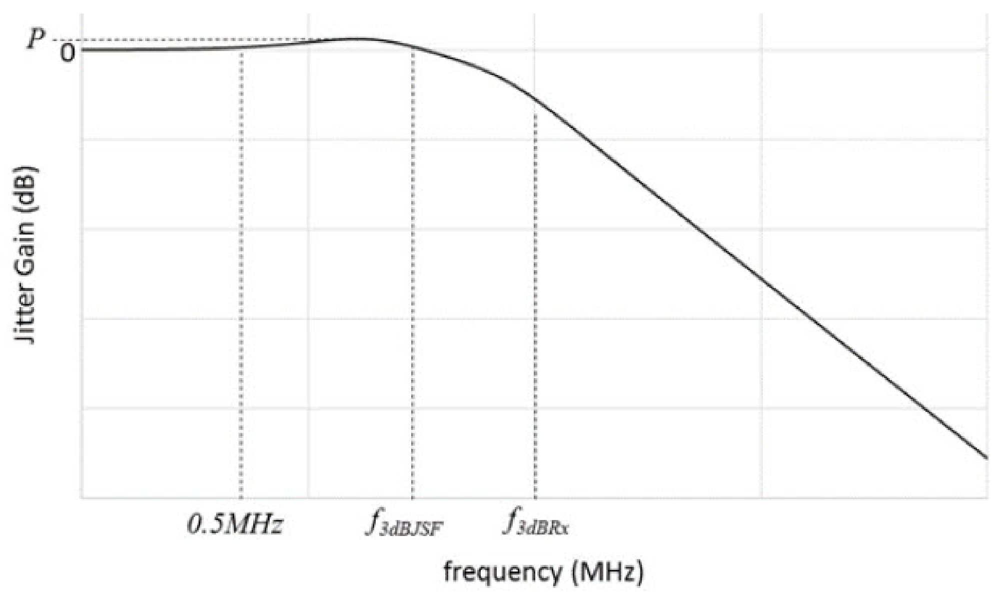


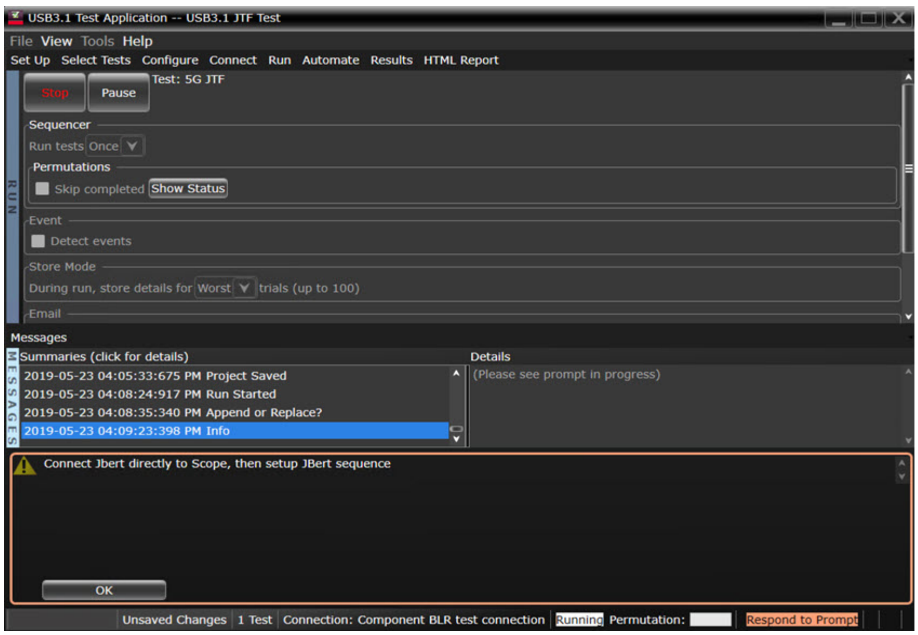
Figure 38 Jitter Transfer Illustration (Figure E-16, USB 3.2 Specification Revision 1.0)

Test Conditions This test is only available for **5G** data rate and **BLR** retimer mode.

Test Overview The purpose of this test is to verify ratio of Pj.

Test Procedure

1 Set up M8020A
2 Set the scope to default setting
3 Setup Function 1 as subtraction of Channel 1 and Channel 3.
4 Set horizontal scale to 50 µs, position at 0 µs.
5 Setup the Acquisition
6 Run the test, the following message prompt appears, JBERT will pre-load with a default sequence.



7 Measurements are made with direct connection between scope and JBERT
8 Click “OK” to continue with the test. The test will sweep across different frequencies to read the jitter measurement using EZJIT plus.

Expected / Observable Results The measurement results for 5G Jitter Transfer Function Test must be within the conformance limit as specified in the USB 3.2 specification.

5G Transmitter Voltage Level Tests

The 5G Transmitter Voltage Level Tests include:

- De-emphasis ratio
- Peak-peak Differential Output Voltage using CP8
- Tx AC Common Mode Voltage Active

This section provides the Methods of Implementation (MOIs) for Voltage Level tests using a Keysight 90000A Series Infiniium oscilloscope, USB 3.0 test fixture, and USB3.2 Test Compliance Application.

Connection Diagram See Appendix A, “Test Connection”.

Test Reference from the Specification Table 6-18, Table 6-19, and Table 6-21 of the USB 3.2 Specification, revision 1.0.

Table 6-18. Transmitter Normative Electrical Parameters

Symbol	Parameter	Gen 1 (5.0 GT/s)	Gen 2 (10 GT/s)	Units	Comments
UI	Unit Interval	199.94 (min) 200.06 (max) 200.34 (min) 200.46 (max)	99.97 (min) 100.03 (max) 100.17 (min) 100.23 (max)	ps ps	The specified UI is equivalent to a tolerance of ±300 ppm for each device. Period does not account for SSC induced variations. Alternate limits apply to "radio friendly" clocking mode which employs a clock whose center frequency is downshifted by 2000ppm. This mode is to be used with a +0/-3000ppm spread.
$V_{TX-DIFF-PP}$	Differential p-p Tx voltage swing	0.8 (min) 1.2 (max)	0.8 (min) 1.2 (max)	V	Nominal is 1 V p-p
$V_{TX-DIFF-PP-LOW}$	Low-Power Differential p-p Tx voltage swing	0.4 (min) 1.2 (max)	0.4 (min) 1.2 (max)	V	Refer to Section 6.7.2. There is no de-emphasis requirement in this mode. De-emphasis is implementation specific for this mode.
$V_{TX-DE-RATIO}$	Tx de-emphasis	3.0 (min) 4.0 (max)	See section 6.7.5.2.	dB	Nominal is 3.5 dB for Gen 1 operation. Gen 2 transmitter equalization requirements are described in section 6.7.5.2.
$R_{TX-DIFF-DC}$	DC differential impedance	72 (min) 120 (max)	72 (min) 120 (max)	Ω	
$V_{TX-RCV-DETECT}$	The amount of voltage change allowed during Receiver Detection	0.6 (max)	0.6 (max)	V	Detect voltage transition should be an increase in voltage on the pin looking at the detect signal to avoid a high impedance requirement when an "off" receiver's input goes below ground.
$C_{AC-COUPLING}$	AC Coupling Capacitor	75 (min) 265 (max)	75 (min) 265 (max)	nF	All Transmitters shall be AC coupled. The AC coupling is required either within the media or within the transmitting component itself.
$t_{CDR\_SLEW\_MAX}$	Maximum slew rate	10	Not applicable	ms/s	See the jitter white paper for details on this measurement. This is a df/ft specification; refer to Section 6.5.4 for details.
SSC_{dfdt}	SSC df/dt	Not applicable	1250 (max)	ppm/µs	See note 1.
$V_{TX-CM-IDLE-DELTA}$	Transmitter idle common-mode voltage change	+600 (max) -600 (min)	+600 (max) -600 (min)	mV	The maximum allowed instantaneous common-mode voltage at TP2 while the transmitter is in U2 or U3 and not actively transmitting LFPS. Note that this is an absolute voltage spec referenced to the receive-side termination ground but serves the purpose of limiting the magnitude and/or slew rate of Tx common mode changes.

Note 1: Measured over a 0.5µs interval using CP10. The measurements shall be low pass filtered using a filter with 3 dB cutoff frequency that is 60 times the modulation rate. The filter stopband rejection shall be greater or equal to a second order low-pass of 20 dB per decade. Evaluation of the maximum df/dt is achieved by inspection of the low-pass filtered waveform.

Figure 39 Table 6-18 of USB 3.2 Specification Version 1.0

Table 6-19. Transmitter Informative Electrical Parameters at TP1 (unless otherwise specified)

Symbol	Parameter	5.0 GT/s	10 GT/s	Units	Comments
$t_{MIN-PULSE-Dj}$	Deterministic min pulse	0.96	0.96	UI	Tx pulse width variation that is deterministic
$t_{MIN-PULSE-Tj}$	Tx min pulse	0.90	0.90	UI	Min Tx pulse at 10^{-12} including Dj and Rj
t_{TX-EYE}	Transmitter Eye	0.625 (min)	0.646 (min)	UI	Includes all jitter sources
$t_{TX-DJ-DD}$	Tx deterministic jitter	0.205 (max)	0.170 (max)	UI	Deterministic jitter only assuming the Dual Dirac distribution
$C_{TX-PARASITIC}$	Tx input capacitance for return loss	1.25 (max)	1.1 (max)	pf	Parasitic capacitance to ground
R_{TX-DC}	Transmitter DC common mode impedance	18 (min) 30 (max)	18 (min) 30 (max)	Ω	DC impedance limits to guarantee Receiver detect behavior. Measured with respect to AC ground over a voltage of 0-500 mV.
$I_{TX-SHORT}$	Transmitter short-circuit current limit	60 (max)	60 (max)	mA	The total current Transmitter can supply when shorted to ground.
$V_{TX-DC-CM}$	Transmitter DC common-mode voltage	0 (min) 2.2 (max)	0 (min) 2.2 (max)	V	The instantaneous allowed DC common-mode voltages at the connector side of the AC coupling capacitors.
$V_{TX-CM-AC-PP\_ACTIVE}$	Tx AC common mode voltage active	100	100 (max)	mV (p-p)	Maximum mismatch from Txp + Txn for both time and amplitude.
$V_{TX-CM-DC-ACTIVE-IDLE-DELTA}$	Absolute DC Common Mode Voltage between U1 and U0	200 (max)	200 (max)	mV	
$V_{TX-IDLE-DIFF-AC-PP}$	Electrical Idle Differential Peak –Peak Output Voltage	0 (min) 10 (max)	0 (min) 10 (max)	mV	
$V_{TX-IDLE-DIFF-DC}$	DC Electrical Idle Differential Output Voltage	0 (min) 10 (max)	0 (min) 10 (max)	mV	Voltage shall be low pass filtered to remove any AC component. This limits the common mode error when resuming U1 to U0.

Figure 40 Table 6-19 of USB 3.2 Specification Version 1.0

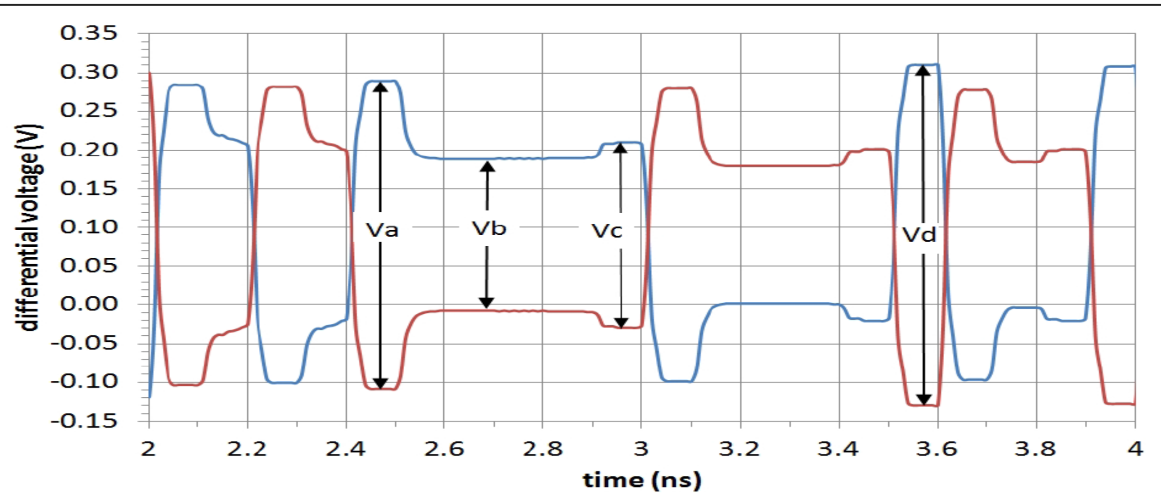
Table 6-21. Gen 2 Transmitter Equalization Settings

Parameter	Value	Comments
Preshoot (dB)	2.2 ± 1.0	Normative requirement[1]
De-emphasis (dB)	−3.1 ± 1.0	Normative requirement[1]
C_{-1}	−0.083	Informative – for reference only
C_1	−0.125	Informative – for reference only
Nominal Boost (dB)	4.7	Informative – for reference only
Va/Vd	0.834	Informative – for reference only
Vb/Vd	0.584	Informative – for reference only
Vc/Vd	0.750	Informative – for reference only

Notes:

1. Measured at the output of the compliance breakout board in Figure 6-24.

Figure 41 Table 6-21 of USB 3.2 Specification Version 1.0



Preshoot = 20log(Vc/Vb)

De-emphasis = 20log(Vb/Va)

Figure 42 5G Transmitter Voltage Level Test measurement signal

Test Conditions

Characterization Mode	Tx Near End (TP0)
Checked	Checked

Test Overview

The purpose of this test is to evaluate the De-emphasis ratio, differential output voltage and common mode voltage and to ensure that they comply with the specification.

Test Procedure

1. Set up the stimulus for 2-cycle LFPS ping.
2. Default the scope.
3. Setup Function 1 as subtraction of Channel 1 and Channel 3.
4. Set horizontal scale to 2ns, position at 0.
5. Set the trigger to “Auto Sweep”

6 Setup the Acquisition
7 Set interpolation to OFF
8 Set Acquire points to AUTO
9 Set Sampling rate to 40GSa/s
10 Set horizontal scale to 20ns, position at 0.
11 Ping the DUT until CP7 is attained.
12 The amplitude will be the Top reading - Base reading. See Figure 43, which shows an example for amplitude measurement using Histogram.

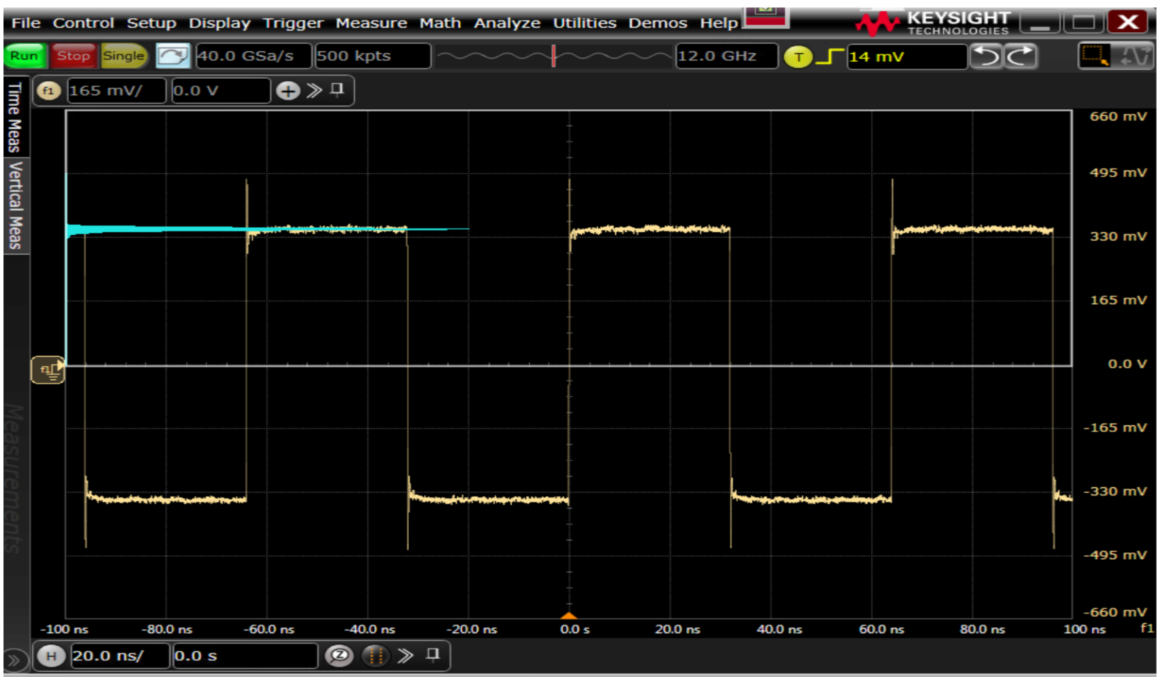


Figure 43 Measuring Amplitude using Histogram

13 Ping the DUT until CP8 is attained.
14 Repeat step 12 to measure the amplitude.
15 Calculate the De-emphasis ratio using the equation:

De-emphasis ratio = 20log(CP8/CP7)

16 Record the measurement for De-emphasis ratio and differential voltage of CP8.
17 Ping the DUT until CP0 is attained.
18 Setup Function 4 as Common Mode of Channel 1 and Channel 3.
19 Measure Vpp of Function 4.
20 Record the measurement results.

Expected / Observable Results

The measurement results for De-emphasis, Amplitude of CP8 and Tx Command Mode Voltage must be within the conformance limit as specified in the USB 3.2 specification.

5 10G Tests

This chapter describes the 10G tests that are performed by the USB3.2 Test Compliance Application in more detail; it contains information from (and refers to) the *Universal Serial Bus 3.2 Specification, Revision 1.0*, and it describes how the tests are performed.

KEYSIGHT TECHNOLOGIES

10G Skew Measurement for Retimer Test

The 10G Skew Measurement Retimer Test includes:

- Skew Measurement Test (Information Only)

This section provides the Methods of Implementation (MOIs) for Skew Measurement for Retimer Test using a Keysight 90000A Series Infiniium oscilloscope, USB 3.0 test fixture, and USB3.2 Test Compliance Application.

Connection Diagram See Appendix A, “Test Connection”.

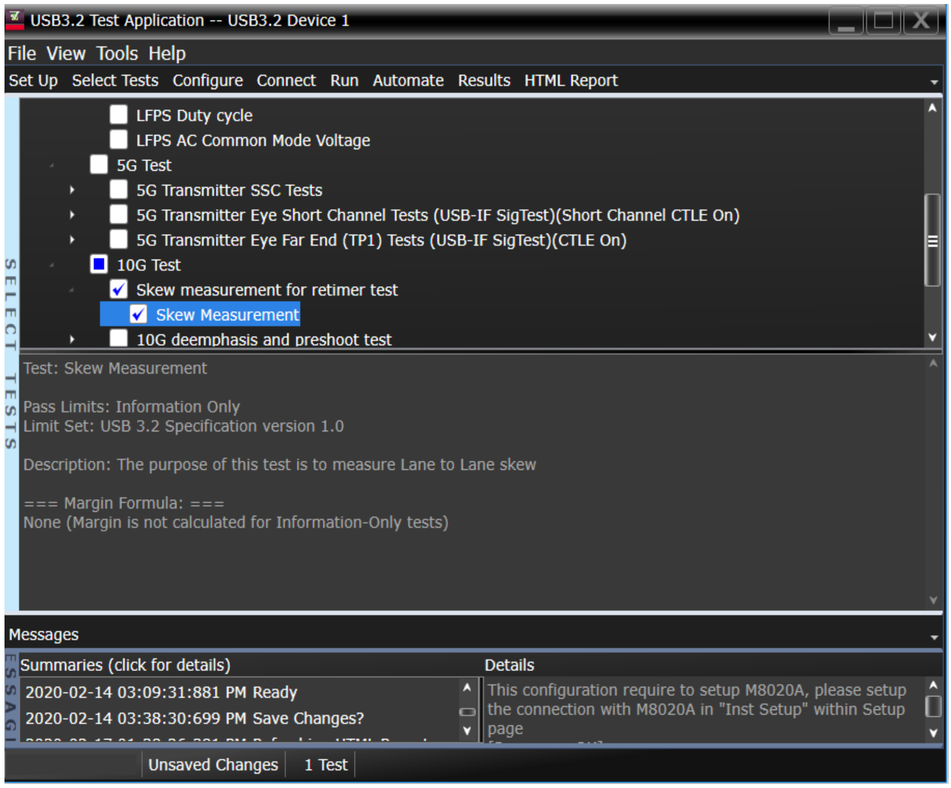
Test Reference from the Specification Not applicable (information only test)

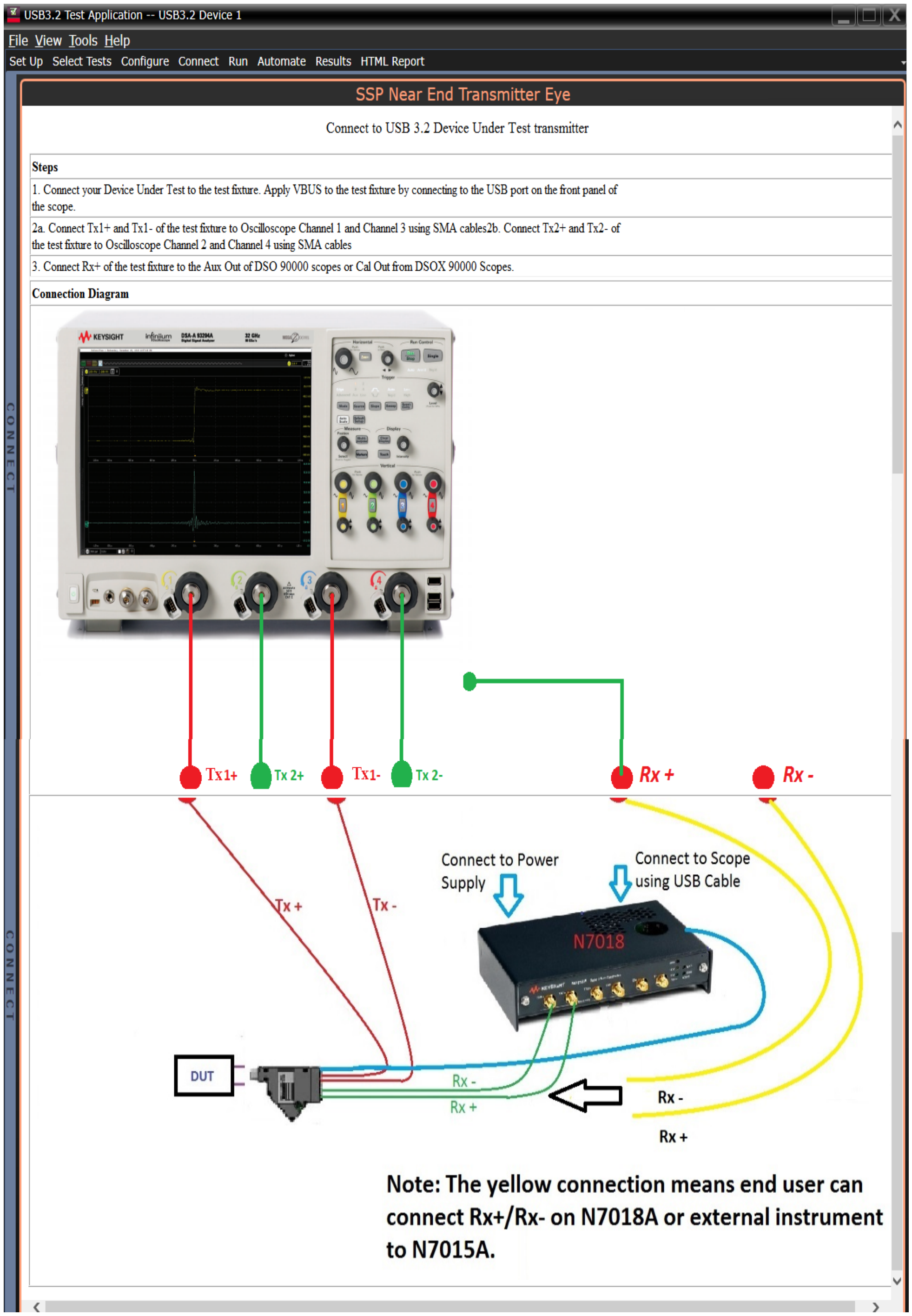
Test Overview The purpose of this test is to measure lane to lane skew.

Test Procedure

1 Set Scope to Default.
2 Connect your Device Under Test to the test fixture. Apply VBUS to the test fixture by connecting to the USB port on the front panel of the scope.
3 Connect Tx1+ and Tx1- of the test fixture to Oscilloscope Channel 1 and Channel 3 using SMA cables2b. Connect Tx2+ and Tx2- of the test fixture to Oscilloscope Channel 2 and Channel 4 using SMA cables
4 Connect Rx+ of the test fixture to the Aux Out of DSO 90000 scopes or Cal Out from DSOX 90000 Scopes.

5 Run Skew Measurement test from the test application





6 After running the test, lane to lane skew measurement value should be available.

Expected / Observable Results The result of the test includes skew measurement value from lane to lane.

10G SCD and LBPS Tests

The 10G LBPS Tests include:

- 10G LBPS tPWM
- 10G LBPS tLFPS_0
- 10G LBPS tLFPS_1

The 10G SCD Tests include:

- 10G SuperSpeedPlus Capability Declaration (SCD1)
- 10G SuperSpeedPlus Capability Declaration (SCD2)
- 10G SCD Rise Time
- 10G SCD Fall Time
- 10G SCD Duty Cycle
- 10G SCD Period
- 10G SCD tRepeat
- 10G SCD tBurst
- 10G SCD Differential Voltage
- 10G SCD Common Mode Voltage

This section provides the Methods of Implementation (MOIs) for 10G LBPS and 10G SCD tests using a Keysight 90000A Series Infiniium oscilloscope, USB 3.0 test fixture, and USB3.2 Test Compliance Application.

10G LBPS Tests

Connection Diagram

See Appendix A, “Test Connection”.

Test Reference from the Specification

Table 6-33 of the USB 3.2 Specification, revision 1.0.

Table 6-33. LBPS Transmit and Receive Specification

	Unit	Transmit			Receive		
		Min	TYP	Max	Min	TYP	Max
tPWM	µs	2	2.2	2.4			
tLFPS-0	µs	0.5		0.80	0.45		0.85
tLFPS-1	µs	1.33		1.80	1.28		1.85

Figure 44 Table 6-33 of USB 3.2 Specification Version 1.0

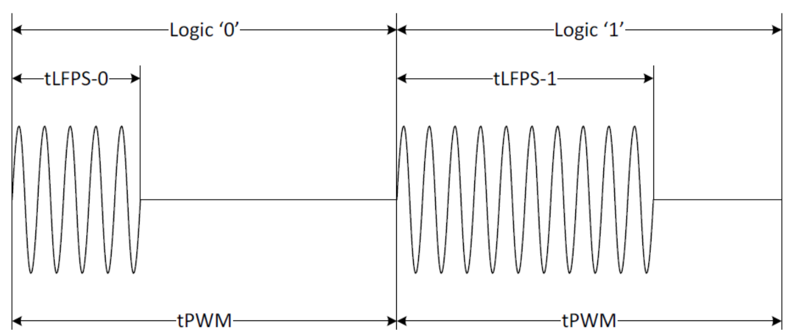


Figure 6-34. Logic Representation of LBPS

Figure 45 Figure 6-34 of USB 3.2 Specification Version 1.0

Test Overview

The purpose of this test is to evaluate the LBPS signal to ensure that the timing variables comply with the specification.

Test Procedure

1 Set up the stimulus connection on the **Set Up** tab.
2 Disconnect the USB 3.0 test fixture from the DUT.
3 Close the HSETT tool.
4 Setup horizontal scaling with Reference to Right, Scale of 30us, position at 200us.
5 Setup Function 1 as subtraction of Channel 1 and Channel 3.
6 Setup Function 4 as common mode of Channel 1 and Channel 3.
7 Setup the trigger:
   a Trigger level to 200mV
   b Hold off to 500us
   c Trigger mode as Pattern mode
   d Set trigger Logic as Low on trigger channel
   e Setup trigger condition to range between 2us to 5 us
8 Setup the trigger to “Single”

9 Setup the Acquisition
   a Select Real Time mode
   b Set interpolation to OFF
   c Acquire points to AUTO
   d Sample rate to 1GSa/s
10 Set stimulus to ON.
11 Verify that the correct waveform has been acquired. The highlighted area in Figure 46 is the LBPS signal.

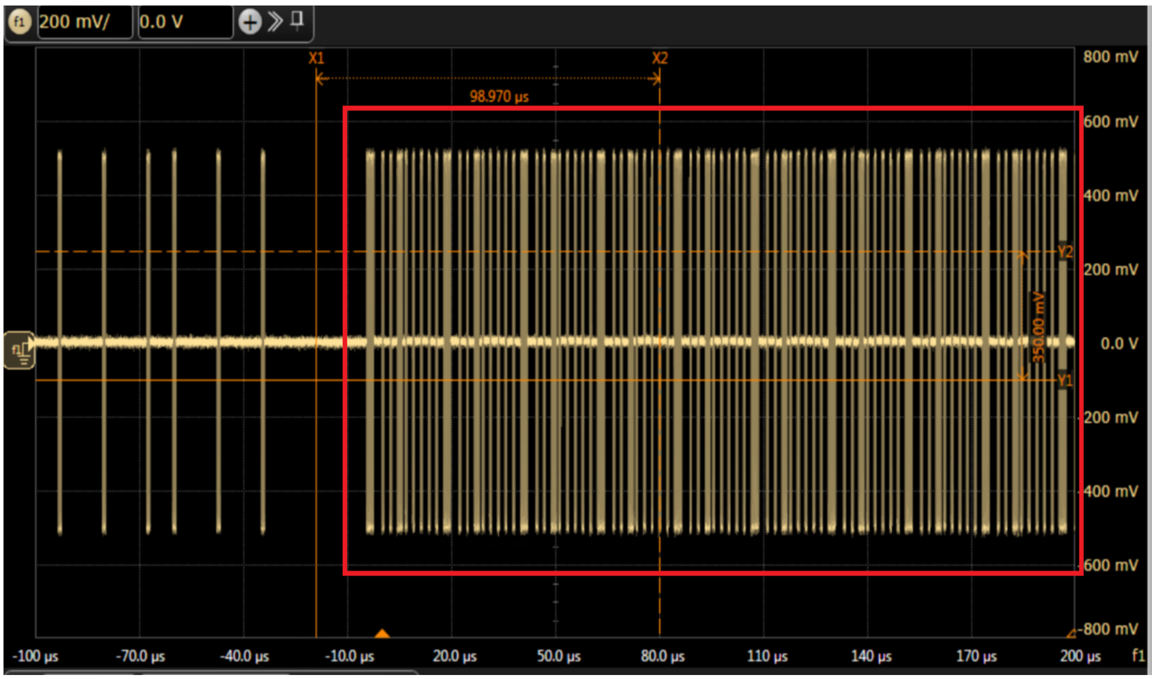


Figure 46 LBPS signal on the acquired waveform in 10G LBPS tests

12 Set up the parameter measurement:
   a Get all locations for the Start Burst and the Stop Burst of the LBPS waveform.
   b Burst Width Measurement is the Start edge – Stop edge of the selected Burst.
   c Burst Interval is the Start edge of the next burst – Start edge of current Burst.
   d Measure the parameter below on the LBPS signal. Refer to *Universal Serial Bus 3.2 Specification, Revision 1.0* for examples pertaining to tPWM, tLFPS_0 and tLFPS_1.
13 Report the measurement values.

Expected / Observable Results

The measurement results for tPWM, tLFPS_0 and tLFPS_1 must be within the conformance limit as specified in the USB 3.2 specification.

10G SuperSpeedPlus Capability Declaration (SCD) Tests

Connection Diagram See Appendix A, “Test Connection”.

Test Reference from the Specification Table 6-29, Table 6-30, and Table 6-32 of the USB 3.2 Specification, revision 1.0.

Table 6-29. Normative LFPS Electrical Specification

Symbol	Minimum	Typical	Maximum	Units	Comments
tPeriod	20		100	ns	
tPeriod for SuperSpeedPlus	20		80	ns	
$V_{CM-AC-LFPS}$			$V_{TX-CM-AC-PP-ACTIVE}$	mV	See Table 6-19
$V_{CM-LFPS-Active}$			10	mV	
$V_{TX-DIFF-PP-LFPS}$	800		1200	mV	Peak-peak differential amplitude
$V_{TX-DIFF-PP-LFPS-LP}$	400		600	mV	Low power peak-peak differential amplitude
tRiseFall2080			4	ns	Measured at TP2, as shown in Figure 6-20.
Duty cycle	40		60	%	Measured at compliance TP2, as shown in Figure 6-20.

Figure 47 Table 6-29 of USB 3.2 Specification Version 1.0

Table 6-30. LFPS Transmitter Timing for SuperSpeed Designs[1]

	tBurst				tRepeat		
	Min	Typ	Max	Minimum Number of LFPS Cycles[2]	Min	Typ	Max
Polling.LFPS	0.6 µs	1.0 µs	1.4 µs		6 µs	10 µs	14 µs
Ping.LFPS[8]	40 ns		200 ns	2	160 ms	200 ms	240 ms
Ping.LFPS for SuperSpeedPlus[9]	40 ns		160ns	2	160 ms	200 ms	240 ms
tReset[3]	80 ms	100 ms	120 ms				
U1 Exit[4,5]	900 ns[7]		2 ms				
U2 / Loopback Exit[4,5]	80 µs[7]		2 ms				

	tBurst				tRepeat		
	Min	Typ	Max	Minimum Number of LFPS Cycles[2]	Min	Typ	Max
U3 Wakeup[4,5]	80 µs[7]		10 ms				

Notes:

1. If the transmission of an LFPS signal does not meet the specification, the receiver behavior is undefined.
2. Only Ping.LFPS has a requirement for minimum number of LFPS cycles.
3. The declaration of Ping.LFPS depends on only the Ping.LFPS burst.
4. Warm Reset, U1/U2/Loopback Exit, and U3 Wakeup are all single burst LFPS signals. tRepeat is not applicable.
5. The minimum duration of an LFPS burst shall be transmitted as specified. The LFPS handshake process and timing are defined in Section 6.9.2.
6. A Port in U2 or U3 is not required to keep its transmitter DC common mode voltage. A port in U2 or U3 is not required to keep its transmitter DC common mode voltage but must not exceed the VTX-CM-IDLE-DELTA spec at TP1. This can be met by either managing the magnitude of the CM shift or the slew rate of the shift. Accordingly, LFPS detectors must tolerate positive and negative CM excursions up to VTX-CM-IDLE-DELTA without false detection. When a port begins U2 exit or U3 wakeup, it may start sending LFPS signal while establishing its transmitter DC common mode voltage. To make sure its link partner receives a proper LFPS signal, a minimum of 80 µs tBurst shall be transmitted. The same consideration also applies to a port receiving LFPS U2 exit or U3 wakeup signal.
7. A port is still required to detect U1 LFPS exit signal at a minimum of 300ns. The extra 300ns is provided as the guard band for successful U1 LFPS exit handshake.
8. This requirement applies to Gen 1x1 only designs.
9. This requirement applies to Gen 1x2, Gen 2x1 and Gen 2x2 designs.

Figure 48 Table 6-30 of USB 3.2 Specification Version 1.0

Table 6-32. Binary Representation of Polling.LFPS

tRepeat (us)	Logic value
6~9	‘0’
11~14	‘1’
9~11	illegal

Figure 6-35. Example of Binary Representation based on Polling.LFPS

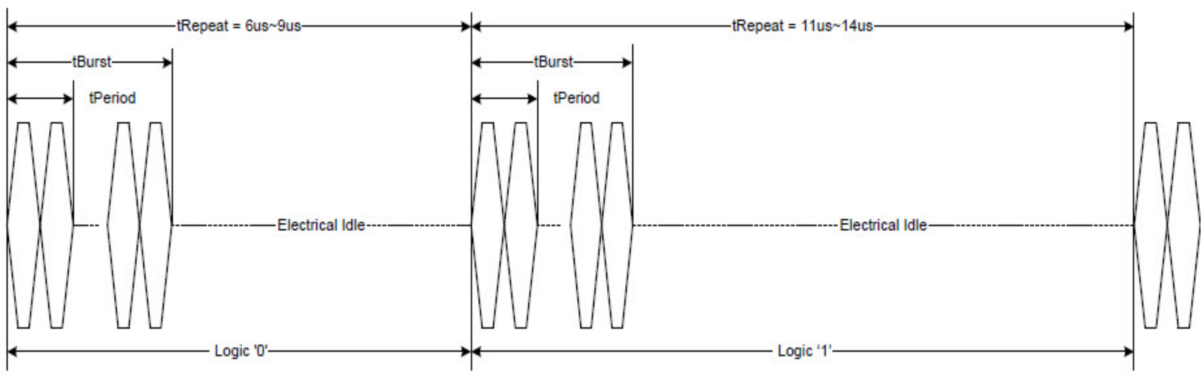


Figure 49 Table 6-32 and Figure 6-35 of USB 3.2 Specification Version 1.0

Test Overview The purpose of this test is to evaluate the SCD signal to ensure that the timing variables comply with the specification.

Test Procedure

1 Set up the stimulus connection on the **Set Up** tab.
2 Disconnect the USB 3.0 test fixture from the DUT.
3 Close the HSETT tool.
4 Setup horizontal scaling with Reference to Right, Scale of 150us, position at -5us.
5 Setup Function 1 as subtraction of Channel 1 and Channel 3.
6 Setup Function 4 as common mode of Channel 1 and Channel 3.
7 Setup the trigger:
   - *a* Trigger level to 200mV
   - *b* Hold off to 500us
   - *c* Trigger mode as Pattern mode
   - *d* Set trigger Logic as Low on trigger channel
   - *e* Setup trigger condition to range between 2us to 5 us
8 Setup the trigger to “Single”
9 Setup the Acquisition
   - *a* Select Real Time mode
   - *b* Set interpolation to OFF
   - *c* Acquire points to AUTO
   - *d* Sample rate to 40GSa/s
   - *e* Bandwidth: 12GHz

10 Set stimulus to ON.

11 Verify that the correct waveform has been acquired. The highlighted area in Figure 50 is the SCD signal.

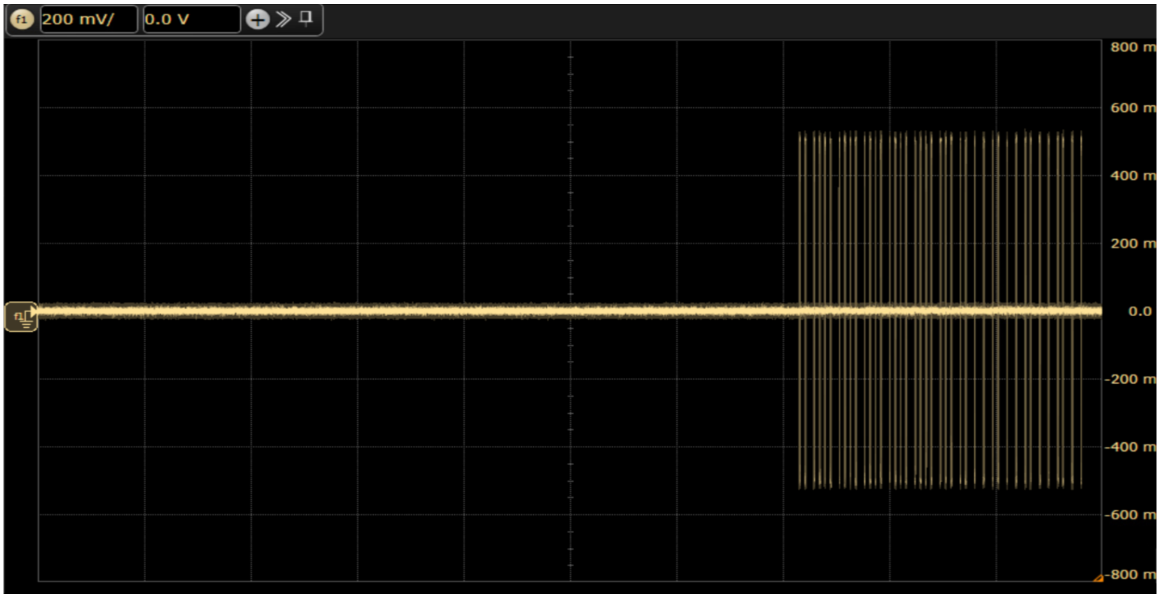


Figure 50 SCD signal on the acquired waveform in 10G SCD tests

12 Set up the parameter measurement:

  a Get all locations for the Start Burst and the Stop Burst of the SCD waveform.

  b Burst Width Measurement is the Start edge – Stop edge of the selected Burst.

  c Measure tRepeat, where tRepeat is the Burst Interval (Start edge of the next burst - Start edge of current burst) measurement.

13 Decode SCD1 from the waveform.

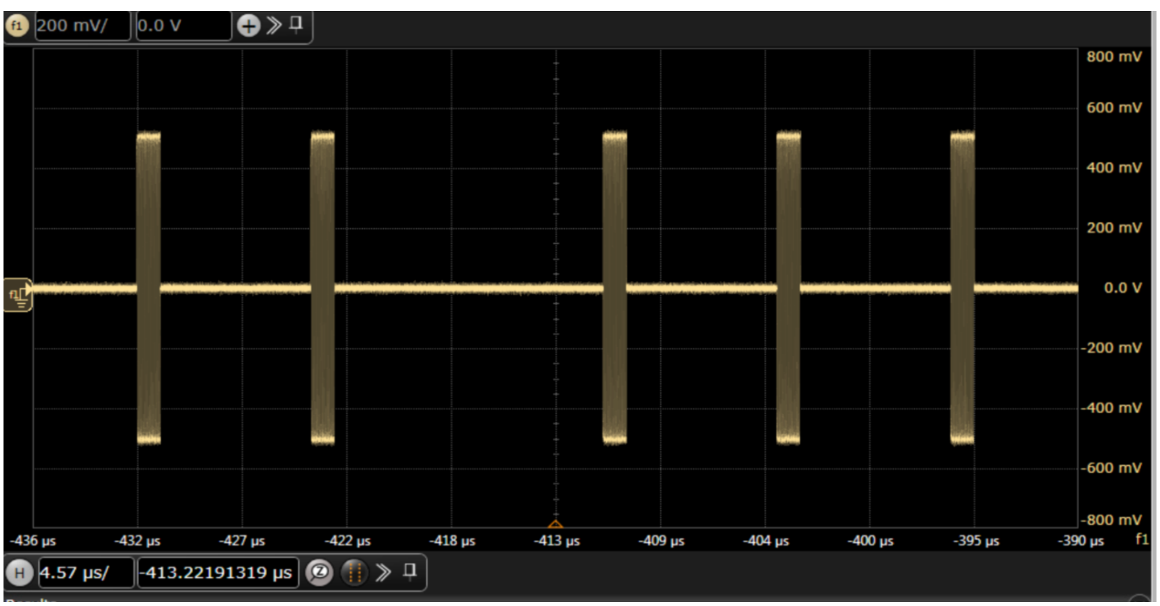


Figure 51 Decoding SCD1

14 Decode SCD2 from the waveform.

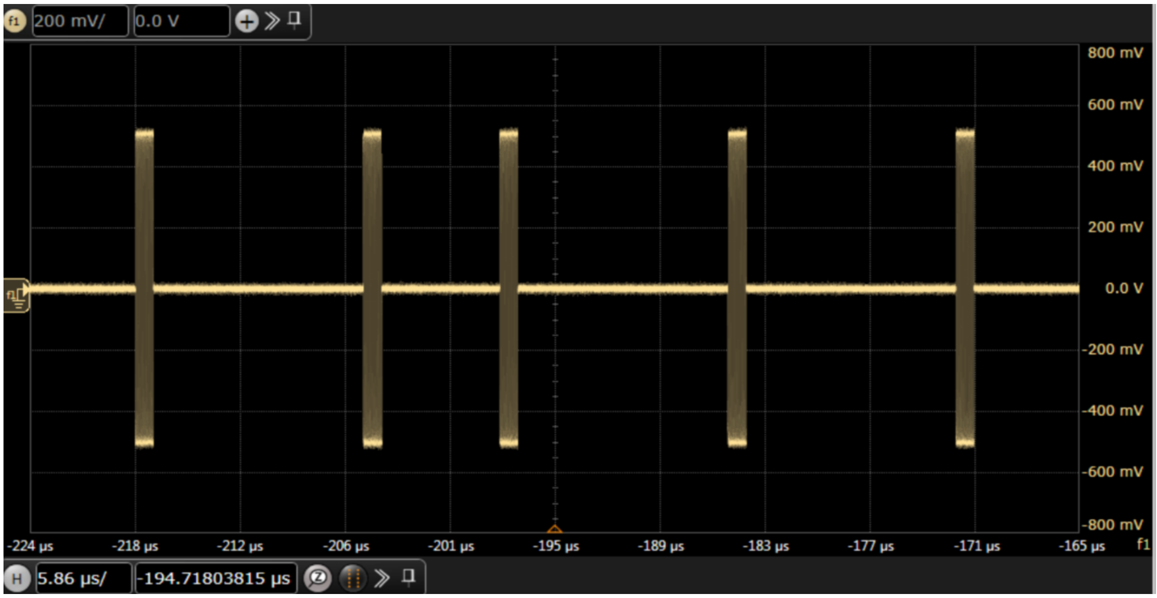


Figure 52 Decoding SCD2

15 Measure the parameters listed below on each Burst. The measurement window on each Burst must be set to 100ns after the Burst start and 100ns before the Burst end. This is done to comply with the CTS requirements.

a Differential Voltage

b Period

c Duty Cycle

d Rise Time

e Fall Time

f Common Mode Voltage

16 Report the measurement values.

Expected / Observable Results

- SCD pattern must be correct. SCD1 pattern is ‘0010’ and SCD2 pattern is ‘1101’.
- The timing measurement results must be within the conformance limit as specified in the USB 3.2 specification.

10G Deemphasis and Preshoot Tests

The 10G Deemphasis and Preshoot Tests include:

- Deemphasis
- Preshoot

This section provides the Methods of Implementation (MOIs) for Transmitter SSC te=sts using a Keysight 90000A Series Infiniium oscilloscope, USB 3.0 test fixture, and USB3.2 Test Compliance Application.

Connection Diagram See Appendix A, “Test Connection”.

Test Reference from the Specification Section 6.7.5.2, Table 6-21 of the USB 3.2 Specification, revision 1.0.

Table 6-21. Gen 2 Transmitter Equalization Settings

Parameter	Value	Comments
Preshoot (dB)	2.2 ± 1.0	Normative requirement[1]
De-emphasis (dB)	−3.1 ± 1.0	Normative requirement[1]
C_{-1}	−0.083	Informative – for reference only
C_1	−0.125	Informative – for reference only
Nominal Boost (dB)	4.7	Informative – for reference only
Va/Vd	0.834	Informative – for reference only
Vb/Vd	0.584	Informative – for reference only
Vc/Vd	0.750	Informative – for reference only

Notes:

1. Measured at the output of the compliance breakout board in Figure 6-24.

Figure 53 Table 6-21 of USB 3.2 Specification Version 1.0

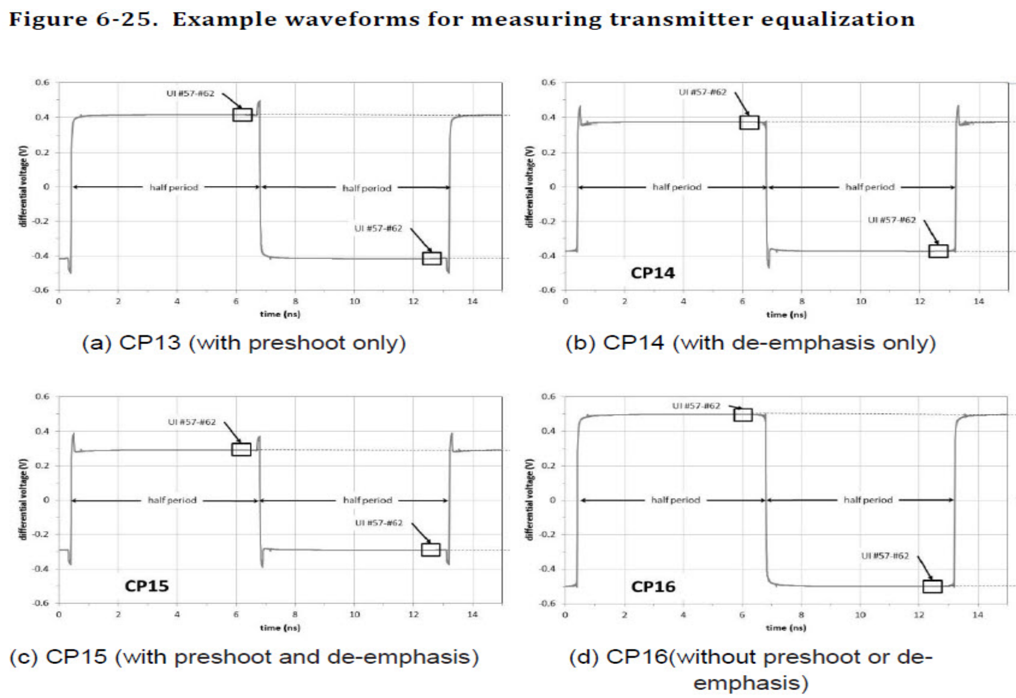


Figure 54 Waveforms with and without Deemphasis and Preshoot

Measurement of the preshoot and de-emphasis is done using CP13, CP14 and CP15. Va, Vc and Vb are obtained using CP13, CP14 and CP15 as shown in Figure 6-23. Preshoot and de-emphasis are calculated using equations (10) and (11).

$$(10) \quad preshoot = 20\log_{10}\left(V_{CP14} / V_{CP15} \right) = 20\log_{10}\left(\frac{-C_{-1} + C_0 + C_1}{C_{-1} + C_0 + C_1} \right)$$

$$(11) \quad deemphasis = 20\log_{10}\left(V_{CP15} / V_{CP13} \right) = 20\log_{10}\left(\frac{C_{-1} + C_0 + C_1}{C_{-1} + C_0 - C_1} \right)$$

Figure 55 Equations for Preshoot and Deemphasis

Test Condition#1

TxEQ Test Mode
True

Test Overview The purpose of this test is to evaluate Preshoot and Deemphasis and that they comply with the specification, using the SigTest tool.

Test Procedure

1 Set up the stimulus for 2-cycle LFPS ping.
2 Default the scope.
3 Setup Function 1 as subtraction of Channel 1 and Channel 3.
4 Set horizontal scale to 2ns, position at 0.
5 Set trigger to AUTO Sweep.

6 Setup the Acquisition
   a Set interpolation to OFF
   b Set acquire points to Auto
   c Sample rate to 40GSa/s
   d Bandwidth to 12GHz
7 Ping the DUT until CP13 is attained. Save the waveform in binary format.
8 Ping the DUT until CP14 is attained. Save the waveform in binary format.
9 Ping the DUT until CP15 is attained. Save the waveform in binary format.
10 Launch SigTest tool.
   a From the drop-down options, select USB 3.2 TxEQ.

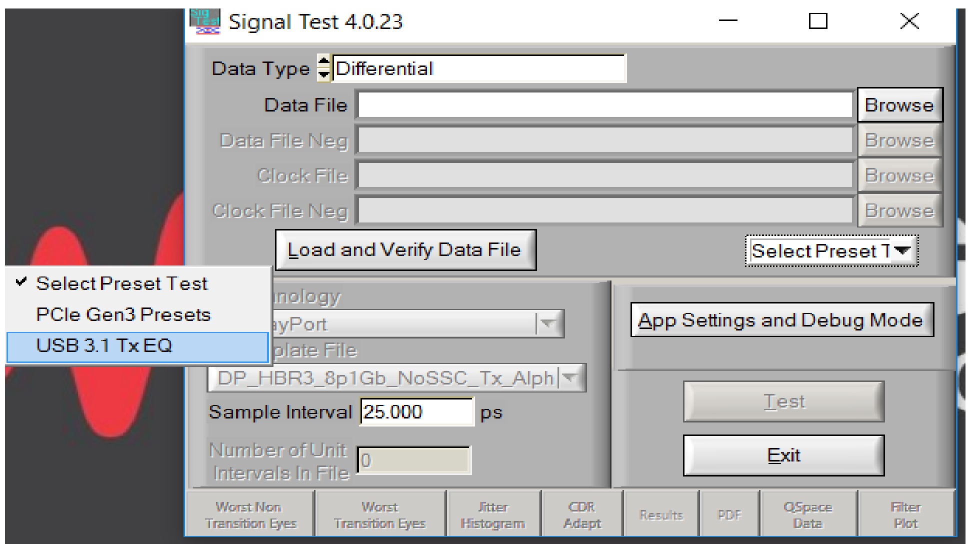


Figure 56 Selecting Preset option in the SigTest tool

   b Place all waveform files (saved in the previous steps) in a common folder.
   c Select “All Files in Folder” option.
   d Browse to the folder that contains all waveform files.

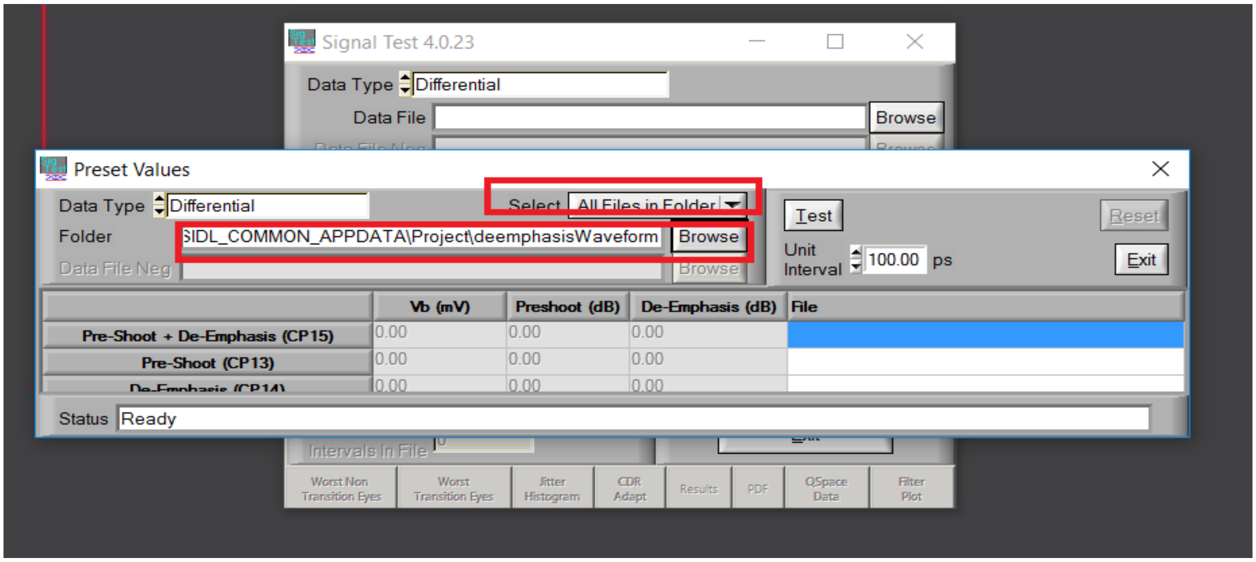


Figure 57 Selecting Waveform Files in the SigTest tool

e Click the “Test” button.

f Record the results.

Expected / Observable Results

The measurement results for Preshoot and Deemphasis must be within the conformance limit as specified in the USB 3.2 specification.

Test Condition#2

TxEQ Test Mode
False

Test Procedure

1 Set up the stimulus for 2-cycle LFPS ping.
2 Default the scope.
3 Setup Function 1 as subtraction of Channel 1 and Channel 3.
4 Set horizontal scale to 2ns, position at 0.
5 Set trigger to AUTO Sweep.
6 Setup the Acquisition
   a Set interpolation to OFF
   b Set acquire points to Auto
   c Sample rate to 40 GSa/s
7 Ping the DUT until CP13 is attained.
8 The top is measured between UI#57 to UI#62.
9 The base is measured between UI#57 to UI#62.
10 The amplitude is measured as Top reading - Base reading. Refer to Figure 54 (or Figure 6-23 of USB 3.2 Specification, revision 1.0).
11 Ping the DUT until CP14 is attained.
12 Repeat steps from step 8 to step 10.
13 Ping the DUT until CP15 is attained.
14 Repeat steps from step 8 to step 10.
15 Calculate Preshoot and Deemphasis using equations shown in Figure 55.

16 Record the measurement result.

Expected / Observable Results

The measurement results for Preshoot and Deemphasis must be within the conformance limit as specified in the USB 3.2 specification.

10G Transmitter SSC Tests

The 10G Transmitter Spread Spectrum Clocking (SSC) Tests include:

- Unit Interval (with SSC) Test
- SSC Deviation Test
- SSC Modulation Rate Test
- SSC df/dt Test

This section provides the Methods of Implementation (MOIs) for 5G Transmitter SSC tests using a Keysight 90000A Series Infiniium oscilloscope, USB 3.0 test fixture, and USB3.2 Test Compliance Application.

Connection Diagram See Appendix A, “Test Connection”.

Test Reference from the Specification Table 6-17 and Table 6-18 of the USB 3.2 Specification, revision 1.0.

Table 6-17. SSC Parameters

Symbol	Description	Limits		Units	Note
		Min	Max		
$t_{SSC-MOD-RATE}$	Modulation Rate	30	33	kHz	
$t_{SSC-FREQ-DEVIATION}$	SSC deviation	+0/-4000 +0/-2000	+0/-5000 +0/-3000	ppm	1, 2, 3 4

Note:

1. The data rate is modulated from 0 ppm to -5000 ppm of the nominal data rate frequency and scales with data rate.
2. This is measured below 2 MHz only.
3. Receiver compliance testing is done under the maximum spread condition.
4. Alternate limits apply to “radio friendly” clock mode which employs a clock whose center frequency is downshifted by 2000ppm.

Figure 58 Table 6-17 of USB 3.2 Specification Version 1.0

Table 6-18. Transmitter Normative Electrical Parameters

Symbol	Parameter	Gen 1 (5.0 GT/s)	Gen 2 (10 GT/s)	Units	Comments
UI	Unit Interval	199.94 (min) 200.06 (max) 200.34 (min) 200.46 (max)	99.97 (min) 100.03 (max) 100.17 (min) 100.23 (max)	ps ps	The specified UI is equivalent to a tolerance of ±300 ppm for each device. Period does not account for SSC induced variations. Alternate limits apply to "radio friendly" clocking mode which employs a clock whose center frequency is downshifted by 2000ppm. This mode is to be used with a +0/-3000ppm spread.
$V_{TX\text{-}DIFF\text{-}PP}$	Differential p-p Tx voltage swing	0.8 (min) 1.2 (max)	0.8 (min) 1.2 (max)	V	Nominal is 1 V p-p
$V_{TX\text{-}DIFF\text{-}PP\text{-}LOW}$	Low-Power Differential p-p Tx voltage swing	0.4 (min) 1.2 (max)	0.4 (min) 1.2 (max)	V	Refer to Section 6.7.2. There is no de-emphasis requirement in this mode. De-emphasis is implementation specific for this mode.
$V_{TX\text{-}DE\text{-}RATIO}$	Tx de-emphasis	3.0 (min) 4.0 (max)	See section 6.7.5.2.	dB	Nominal is 3.5 dB for Gen 1 operation. Gen 2 transmitter equalization requirements are described in section 6.7.5.2.
$R_{TX\text{-}DIFF\text{-}DC}$	DC differential impedance	72 (min) 120 (max)	72 (min) 120 (max)	Ω	
$V_{TX\text{-}RCV\text{-}DETECT}$	The amount of voltage change allowed during Receiver Detection	0.6 (max)	0.6 (max)	V	Detect voltage transition should be an increase in voltage on the pin looking at the detect signal to avoid a high impedance requirement when an "off" receiver's input goes below ground.
$C_{AC\text{-}COUPLING}$	AC Coupling Capacitor	75 (min) 265 (max)	75 (min) 265 (max)	nF	All Transmitters shall be AC coupled. The AC coupling is required either within the media or within the transmitting component itself.
$t_{CDR\_SLEW\_MAX}$	Maximum slew rate	10	Not applicable	ms/s	See the jitter white paper for details on this measurement. This is a df/ft specification; refer to Section 6.5.4 for details.
SSC_{dfdt}	SSC df/dt	Not applicable	1250 (max)	ppm/µs	See note 1.
$V_{Tx\text{-}CM\text{-}IDLE\text{-}DELTA}$	Transmitter idle common-mode voltage change	+600 (max) -600 (min)	+600 (max) -600 (min)	mV	The maximum allowed instantaneous common-mode voltage at TP2 while the transmitter is in U2 or U3 and not actively transmitting LFPS. Note that this is an absolute voltage spec referenced to the receive-side termination ground but serves the purpose of limiting the magnitude and/or slew rate of Tx common mode changes.

Note 1: Measured over a 0.5µs interval using CP10. The measurements shall be low pass filtered using a filter with 3 dB cutoff frequency that is 60 times the modulation rate. The filter stopband rejection shall be greater or equal to a second order low-pass of 20 dB per decade. Evaluation of the maximum df/dt is achieved by inspection of the low-pass filtered waveform.

Figure 59 Table 6-18 of USB 3.2 Specification Version 1.0

Unit Interval (with SSC) Test

Test Conditions

Reference Clock
Clean Clock

Test Overview The purpose of this test is to verify that the SSC of the transmitter complies with the specification.

Test Procedure

1 Set up the stimulus for 2-cycle LFPS ping.
2 Default the scope.
3 Setup Function 1 as subtraction of Channel 1 and Channel 3.
4 Set horizontal scale to 2ns, position at 0.
5 Setup the Acquisition
   a Select Sampling Mode as "Real Time"
   b Set interpolation to OFF
   c Sample rate to 80GSa/s
   d 16M points
   e Bandwidth to 25GHz
6 Set Sweep as AUTO
7 Ping the DUT until CP10 is attained.
8 Setup horizontal scale to 20us, position at 0.
9 Stop the acquisition and save the waveform.
10 Set 'Unit Interval Measurement' to ON.
11 Set 'Measurement Trend' to ON.
12 Measure Vmax of the measurement trend.
13 Measure Vmin of the measurement trend.
14 Measure Vaverage of the measurement trend.
15 Record the measurement result.

Expected / Observable Results The measurement results for Unit Interval must be within the conformance limit as specified in the USB 3.2 specification.

SSC Deviation Test, SSC Modulation Rate Test, SSC df/dt Test

Test Conditions#1

Reference Clock	SSC Test Mode
SSC	True

Test Overview The purpose of this test is to verify that the SSC of the transmitter complies with the specification.

Test Procedure

1 Set up the stimulus for 2-cycle LFPS ping.
2 Default the scope.
3 Setup Function 1 as subtraction of Channel 1 and Channel 3.
4 Set horizontal scale to 2ns, position at 0.
5 Setup the Acquisition
   a Select Sampling Mode as “Real Time”
   b Set interpolation to OFF
   c Sample rate to 80GSa/s
   d 16M points
   e Bandwidth to 25GHz
6 Set Sweep as AUTO
7 Ping the DUT until CP10 is attained.
8 Setup horizontal scale to 20us, position at 0.
9 Stop the acquisition and save the waveform in binary format.

10 Launch SigTest tool.
   a Load the waveform file.
   b Ensure that SSC template is selected. See Figure 60.

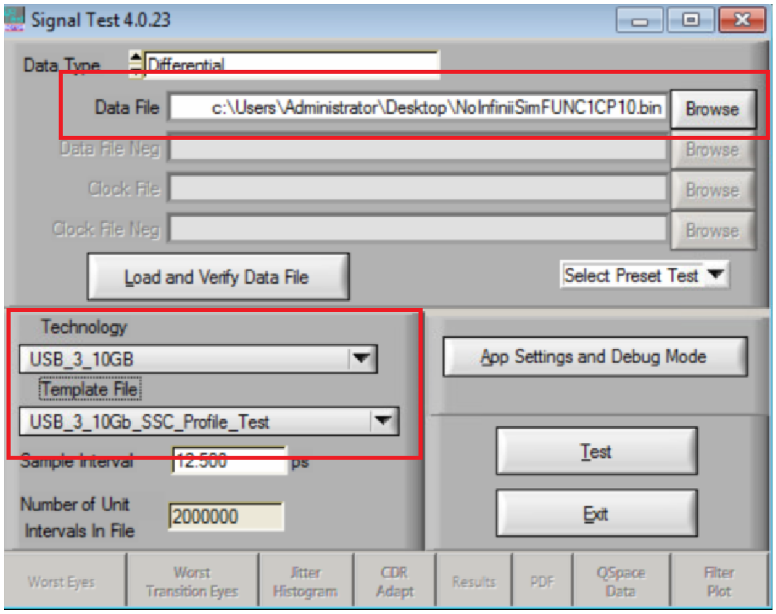


Figure 60 Selecting the SSC Template File on the SigTest tool

11 Record the measurement result.

Test Conditions#2

Reference Clock	SSC Test Mode
SSC	False

Test Procedure

1 Set up the stimulus for 2-cycle LFPS ping.
2 Default the scope.
3 Setup Function 1 as subtraction of Channel 1 and Channel 3.
4 Set horizontal scale to 2ns, position at 0.
5 Setup the Acquisition
   a Select Sampling Mode as “Real Time”
   b Set interpolation to OFF
   c Sample rate to 80GSa/s
   d 16M points
   e Bandwidth to 25GHz
6 Set Sweep as AUTO
7 Ping the DUT until CP10 is attained.
8 Setup horizontal scale to 20us, position at 0.
9 Stop the acquisition.
10 Set ‘Unit Interval Measurement’ to ON.
11 Set ‘Measurement Trend’ to ON for function 1.
12 Save the measurement in CSV format.

13 The CSV waveform is processed within a MATLAB script.

a Perform a second-order low pass filter. Cut-off frequency is set as 60 times of the modulation rate, 1.98MHz.

b Measure the Vtop and Vbase for every SSC triangle profile, as shown in Figure 61.

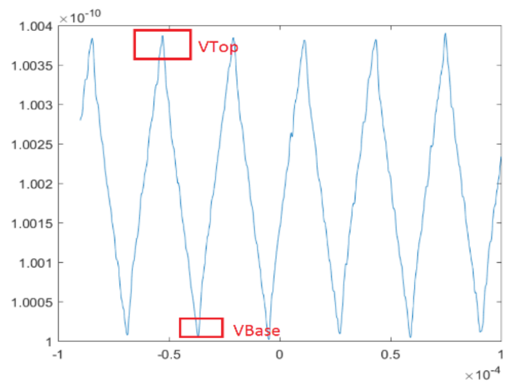


Figure 61 Vtop and Vbase measurements on an SCC triangle profile

c Measure the modulation rate, modulation rate is 1/tcycle. tcycle is defined as shown in Figure 62.

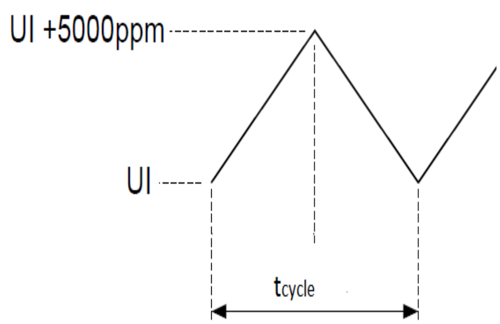


Figure 62 Measuring Modulation Rate

d Measure the rate of change over 0.5us interval. Convert the resulting value's unit to ppm/us.

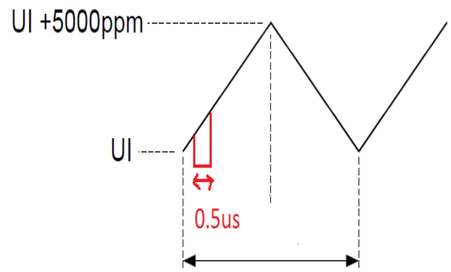


Figure 63 Measuring Rate of change

14 Record the measurement result.

Expected / Observable Results

The measurement results for SSC must be within the conformance limit as specified in the USB 3.2 specification.

10G Eye Measurement Test

The 10G Eye Measurement Test includes:

- CTLE_Adc Selection

This section provides the Methods of Implementation (MOIs) for 10G Eye Measurement test using a Keysight 90000A Series Infiniium oscilloscope, USB 3.0 test fixture, and USB3.2 Test Compliance Application.

Connection Diagram See Appendix A, “Test Connection”.

Test Reference from the Specification ECN CTLE of the USB 3.2 Specification, revision 1.0.

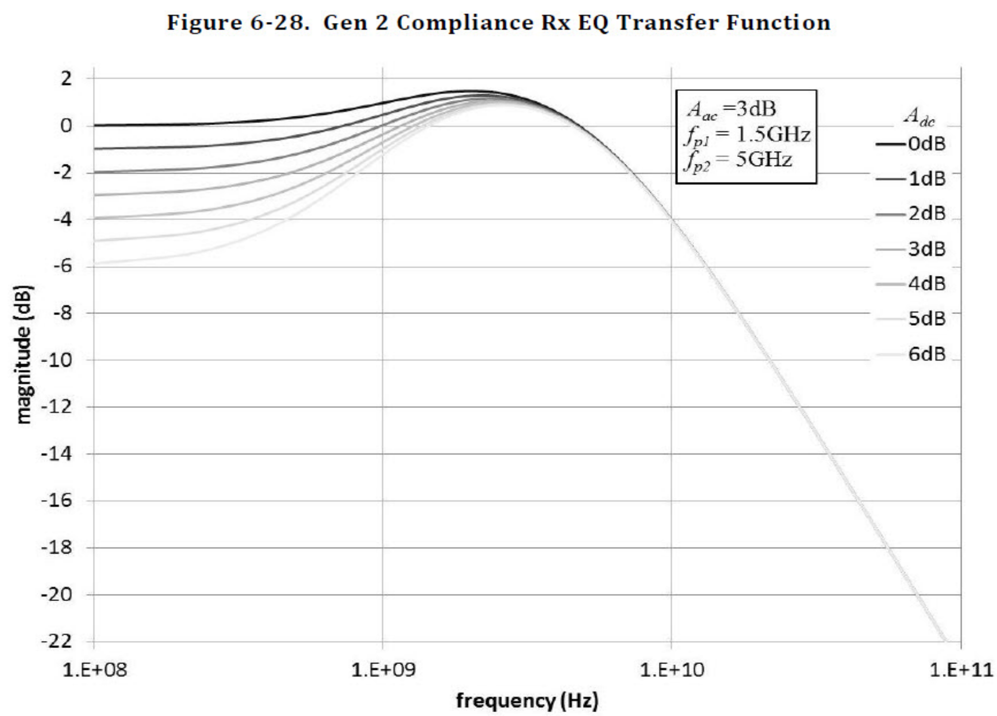


Figure 64 Figure 6-28 of USB 3.2 Specification Version 1.0

Test Condition

Test Method
SDA

Test Overview The purpose of this test is to obtain the DC Gain that yields the best Eye opening, which complies with the specification.

Test Procedure

1. Set up the stimulus for 2-cycle LFPS ping.
2. Default the scope.
3. Setup Function 1 as subtraction of Channel 1 and Channel 3.
4. Set horizontal scale to 2ns, position at 0.
5. Ping the DUT until CP10 is attained.

6 Setup the Acquisition
   a Select Sampling Mode as "Real Time"
   b Set interpolation to OFF
   c Sample rate to 80GSa/s
   d 16M points
   e Bandwidth to 25GHz
7 Set Sweep as AUTO.
8 Setup horizontal scale to 20us, position at 0.
9 Stop the acquisition and save the waveform.
10 Setup Clock Recovery:
   2nd order PLL, Nominal data rate of 10Gbps, loop bandwidth of 7.5MHz, damping factor of 0.707
11 Setup CTLE:
   a # of Poles: USB3.2
   b Pole 1 Frequency: 1.5GHz
   c Pole 2 Frequency: 5.0GHz
   d AC Gain: 1.413
   e DC Gain: 10^(DC/20), where the default value of DC is 0dB
12 Enable Mask Test:
   a Load Mask
   b Set Source as CTLE
   c Set Color Grade to ON
   d Set Infinite Persistent to ON
   e Set Mask Scaling:
   - Horizontal Scaling: -50ps
   - Delta: 100ps
   f Set Mask Vertical Scaling:
   - 1 Level: 600mV
   - 0 Level: -600mV
   g Enable "Bind 1 & 0 Levels"
   h Enable "Real-Time Eye"
13 Repeat steps from step 11 to step 12 after changing the value of DC from 0dB to -6dB.
14 Record the value of DC that yields the best Eye opening.

Expected / Observable Results

The DC Gain must yield the best Eye opening, which must conform to the USB 3.2 specification.

10G Transmitter Random Jitter Tests

The 10G Transmitter Random Jitter Test includes:

- 10G Random Jitter

This section provides the Methods of Implementation (MOIs) for 10G Transmitter Random Jitter test using a Keysight 90000A Series Infiniium oscilloscope, USB 3.0 test fixture, and USB3.2 Test Compliance Application.

Connection Diagram See Appendix A, “Test Connection”.

Test Reference from the Specification Table 6-16 and Table 6-20 of the USB 3.2 Specification, revision 1.0.

Table 6-16. Informative Jitter Budgeting at the Silicon Pads[7]

Jitter Contribution (ps)	Gen 1 (5 GT/s)			Gen 2 (10 GT/s)		
	Rj[1,2]	Dj[3]	Tj[4] at 10^{-12}	Rj[1,2]	Dj[3]	Tj[4] at 10^{-12}
Tx[6]	2.42	41	75	1.00	17	31.1
Media[5]	2.13	45	75	0.00	36	36.0
Rx	2.42	57	91	1.00	27.1	41.2
Total	4.03	143	200	1.41	80.1	100

Notes:

1. Rj is the sigma value assuming a Gaussian distribution.
2. Rj Total is computed as the Root Sum Square of the individual Rj components.
3. Dj budget is using the Dual Dirac method.
4. Tj at a 10^{-12} BER is calculated as 14.068 * Rj + Dj.
5. The media budget includes the cancellation of ISI from the appropriate Rx equalization function.
6. Tx is measured after application of the JTF.
7. In this table, Tx jitter is defined at TP1, Rx jitter is defined at TP4, and media jitter is defined from TP1 to TP4.

Figure 65 Table 6-16 of USB 3.2 Specification Version 1.0

10G Random Jitter Test

Test Condition#1

Test Method
USB-IF SigTest

Test Overview The purpose of this test is to verify that the Short Channel Random Jitter of the transmitter complies with the specification.

Test Procedure

1 Set up the stimulus for 2-cycle LFPS ping.
2 Default the scope.
3 Setup Function 1 as subtraction of Channel 1 and Channel 3.
4 Set horizontal scale to 2ns, position at 0.
5 Ping the DUT until CP10 is attained.
6 Setup the Acquisition
   a Select Sampling Mode as “Real Time”
   b Set interpolation to OFF
   c Sample rate to 80GSa/s
   d 16M points
   e Bandwidth to 25GHz
7 Set Sweep as AUTO.
8 Setup horizontal scale to 20us, position at 0.
9 Stop the acquisition and save the waveform in binary format.
10 Launch SigTest tool.
11 Load the waveform file. Select the options for Technology and Template File as shown in Figure 66.
   a Technology set to ‘USB_3_10GB’
   b Template File set to ‘USB_3_10Gb_CP10_Tx_Rj_Test’

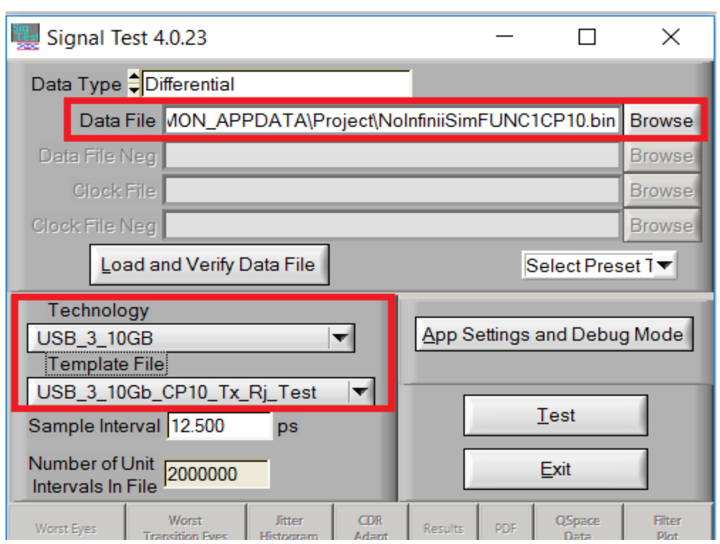


Figure 66 SigTest tool settings for measuring 10G RJ

12 Record the measurement result for the 10G RJ.

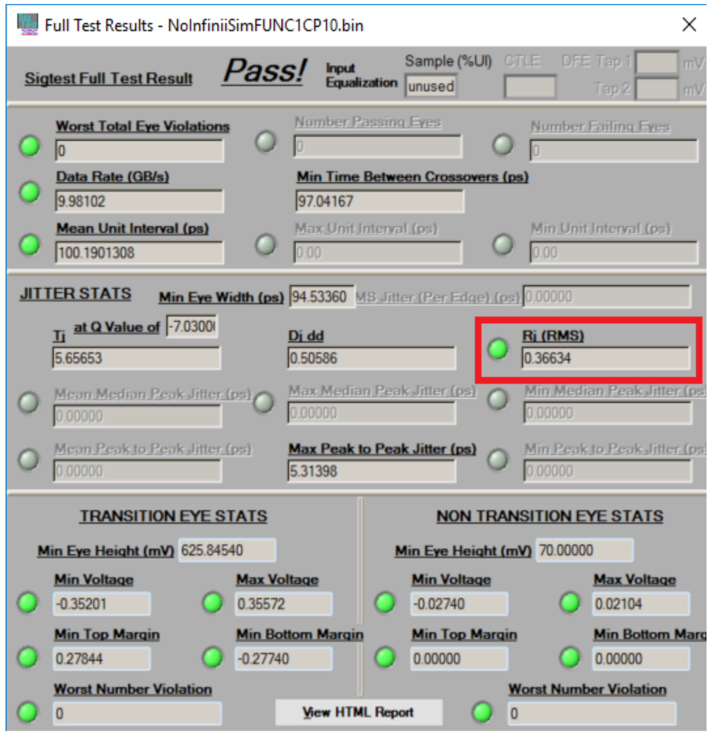


Figure 67 SigTest tool report for 10G RJ measurement

Expected / Observable Results

The measurement results for 10G Random Jitter must be within the conformance limit as specified in the USB 3.2 specification.

Test Condition#2

Test Method
SDA

Test Procedure

1 Set up the stimulus for 2-cycle LFPS ping.
2 Default the scope.
3 Setup Function 1 as subtraction of Channel 1 and Channel 3.
4 Set horizontal scale to 2ns, position at 0.
5 Ping the DUT until CP10 is attained.
6 Setup the Acquisition
   a Select Sampling Mode as “Real Time”
   b Set interpolation to OFF
   c Sample rate to 80GSa/s
   d 16M points
   e Bandwidth to 25GHz
7 Set Sweep as AUTO.
8 Setup horizontal scale to 20us, position at 0.
9 Stop the acquisition and save the waveform.

10 Setup CTLE:
  a # of Poles: USB3.2
  b Pole 1 Frequency: 1.5GHz
  c Pole 2 Frequency: 5.0GHz
  d AC Gain: 1.413
  e DC Gain: 10^(DC/20) (See "10G Eye Measurement Test" on page 95 for the optimum value of DC)
11 Setup Clock Recovery:
  2nd order PLL, data rate of 10Gbps, loop bandwidth of 7.5MHz, damping factor of 0.707
12 Setup EZJIT Complete:
  a Set CTLE as source
  b Enable Jitter Mode on EZJIT+
  c BER Level: 1E-6
  d Measurement: TIE (Phase)
  e Edges: Both
  f RJ Bandwidth: Narrow
  g RJ Method: Spectral Only
  h Pattern Length: Periodic, Auto
13 Obtain RJ reading.

Expected / Observable Results

The measurement results for 10G Random Jitter must be within the conformance limit as specified in the USB 3.2 specification.

10G Transmitter Eye Far End (TP1) Tests

The 10G Transmitter Eye Far End (TP1) Tests include:

- 10G Far End Maximum Deterministic Jitter Test
- 10G Far End Total Jitter at BER- 6 Test
- 10G Far End Template Test
- 10G Far End Differential Output Voltage
- Extrapolated Eye Height
- Minimum Eye Width

This section provides the Methods of Implementation (MOIs) for 10G Transmitter Eye Far End (TP1) tests using a Keysight 90000A Series Infiniium oscilloscope, USB 3.0 test fixture, and USB3.2 Test Compliance Application.

Connection Diagram See Appendix A, “Test Connection”.

Test Reference from the Specification Table 6-16 and Table 6-20 (ECN for SSP System Jitter Budget) of the USB 3.2 Specification, revision 1.0.

Table 6-20. Normative Transmitter Eye Mask at Test Point TP4

Signal Characteristic	5GT/s		10GT/s		Units	Note
	Minimum	Maximum	Minimum	Maximum		
Eye Height	100	1200	70	1200	mV	2, 3, 4
Dj		0.43		0.530	UI	1, 2, 3
Rj		0.23		0.141	UI	1, 5, 6
Tj		0.66		0.671	UI	1, 2, 3

Notes:

1. Measured over 10^6 consecutive UI and extrapolated to 10^{-12} BER.
2. Measured after receiver equalization function.
3. Measured at end of reference channel and cables at TP4 in Figure 6-20.
4. The eye height is to be measured at the minimum opening over the range from the center of the eye ± 0.05 UI.
5. The Rj specification is calculated as 14.069 times the RMS random jitter for 10^{-12} BER.
6. Measured at the output of the compliance breakout board without embedding the compliance cable and load board.

Figure 68 Table 6-20 of USB 3.2 Specification Version 1.0

NOTE According to the USB 3.2 Specification, Version 1.0 CTS, the Eye Width and the Extrapolated Eye Height measurement requires computing the Data Eye using CP9 using Rj as input from the CP10 waveform and compare it against requirements for a 70mV Eye Height and a 48.0ps Eye Width both at 10E-6 BER.

6.8.2.2.2 Reference DFE

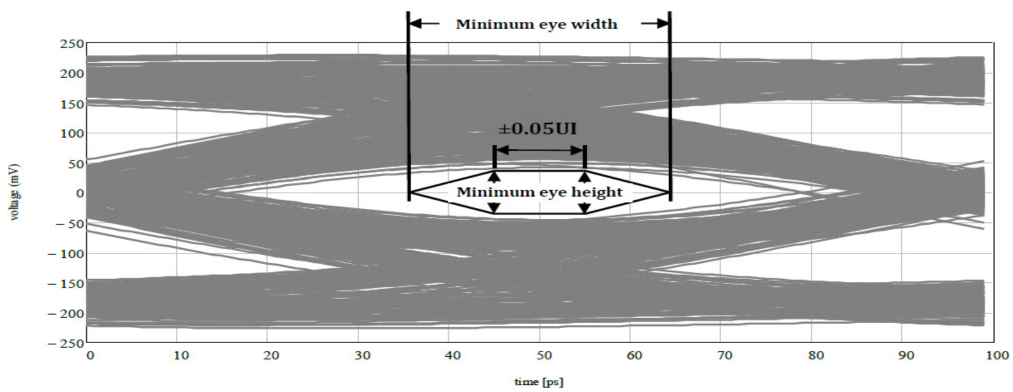
In addition to the 1st order CTLE, a one-tap reference DFE is used in transmitter compliance testing. The DFE behavior is described by equation (15) and Figure 6-29. The limits on d_1 are 0 to 50mV.

$$y_k = x_k - d_1 \operatorname{sgn}(y_{k-1}) \qquad (15)$$

where
- y_k is the DFE differential output voltage
- y^*_k is the decision function output voltage, $|y^*_k| = 1$
- x_k is the DFE differential input voltage
- d_1 is the DFE feedback coefficient
- k is the sample index in UI

Figure 69 Equation for Reference DFE

Figure 6-17. Eye Masks



Gen 2 eye mask

Figure 70 Gen 2 Eye Mask for 10G Transmitter Eye Far End (TP1) tests

10G Far End Maximum Deterministic Jitter, 10G Far End Total Jitter At BER-6, 10G Far End Template Test, Extrapolated Eye Height, Minimum Eye Width

Test Overview The purpose of this test is to verify that the measured Deterministic Jitter and Total Jitter comply with the specification.

Test Condition

Test Method
USB-IF SigTest

Test Procedure

1 Set up the stimulus for 2-cycle LFPS ping.
2 Default the scope.
3 Setup Function 1 as subtraction of Channel 1 and Channel 3.
4 Set horizontal scale to 2ns, position at 0.
5 Ping the DUT until CP9 is attained.
6 Setup the Acquisition
   a Select Sampling Mode as “Real Time”
   b Set interpolation to OFF
   c Sample rate to 80GSa/s
   d 16M points
   e Bandwidth to 25GHz
7 Setup InfiniiSim. See Appendix A, “InfiniiSim Setup for 10G” for settings.
8 Set Sweep as AUTO.
9 Setup horizontal scale to 20us, position at 0.
10 Stop the acquisition and save the waveform in binary format.
11 Launch SigTest tool.
12 Load the waveform file. Select the options for Technology and Template File as shown in Figure 71.
   a Technology set to ‘USB_3_10GB’
   b Template File set to ‘USB_3_10Gb_CP9_Tx’
   c Set Random Jitter

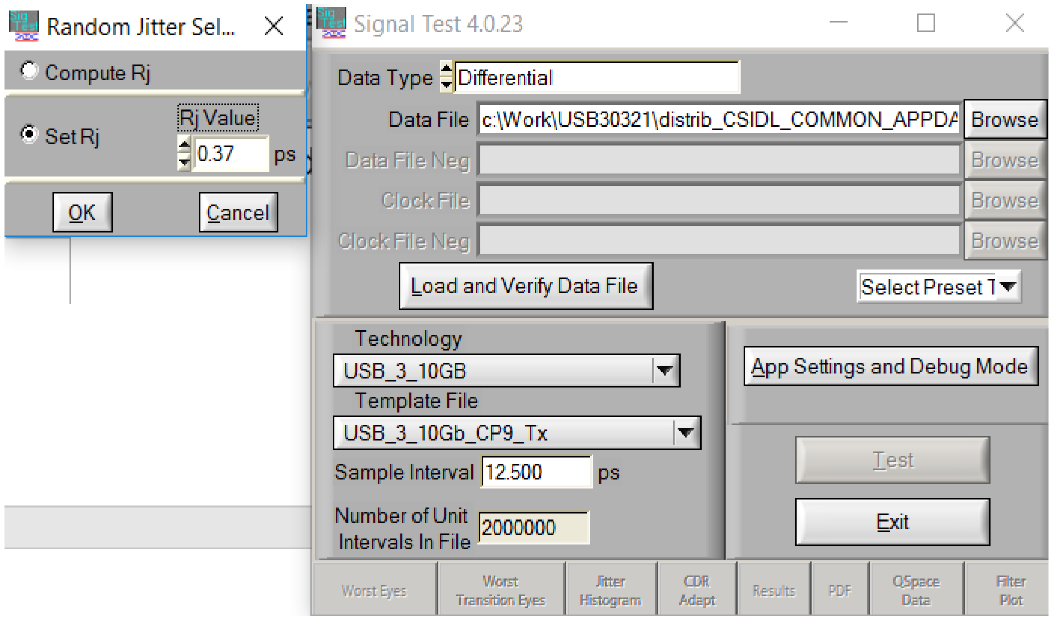


Figure 71 SigTest tool settings for measuring DJ, TJ, Eye Width and Extrapolated Eye Height

13 Record the measurement result for DJ, TJ, Eye Width and Extrapolated Eye Height.

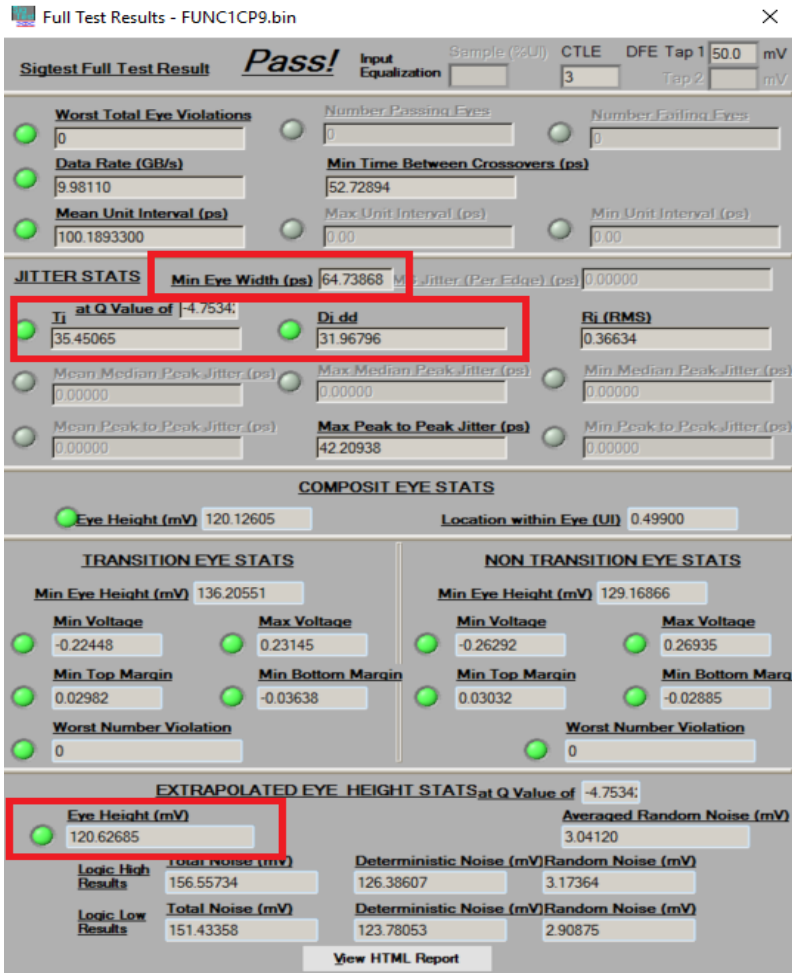


Figure 72 SigTest tool report for DJ, TJ, Eye Width and Eye Height measurement

Expected / Observable Results

The measurement results for Deterministic Jitter, Total Jitter, Eye Width and Extrapolated Eye Height must be within the conformance limit as specified in the USB 3.2 specification.

10G Far End Maximum Deterministic Jitter and 10G Far End Total Jitter At BER-6 Test

Test Condition

Test Method
SDA

Test Procedure

1 Set up the stimulus for 2-cycle LFPS ping.
2 Default the scope.
3 Setup Function 1 as subtraction of Channel 1 and Channel 3.
4 Set horizontal scale to 2ns, position at 0.
5 Ping the DUT until CP9 is attained.
6 Setup the Acquisition
   a Select Sampling Mode as “Real Time”
   b Set interpolation to OFF
   c Sample rate to 80GSa/s
   d 16M points
7 Setup InfiniiSim. See Appendix A, “InfiniiSim Setup for 10G” for settings.
8 Set Sweep as AUTO.
9 Setup horizontal scale to 20us, position at 0.
10 Stop the acquisition and save the waveform.
11 Setup CTLE:
   a # of Poles: USB3.2
   b Pole 1 Frequency: 1.55GHz
   c Pole 2 Frequency: 5.0GHz
   d AC Gain: 1.413
   e DC Gain: 10^(DC/20) (See “10G Eye Measurement Test” on page 95 for the optimum value of DC)
12 Setup Clock Recovery:
   2nd order PLL, data rate of 10Gbps, loop bandwidth of 7.5MHz, damping factor of 0.707
13 Setup EZJIT Complete:
   a Set CTLE as source
   b Enable Jitter Mode on EZJIT+
   c BER Level: 1E-6
   d Measurement: TIE (Phase)
   e Edges: Both
   f RJ Bandwidth: Narrow
   g RJ Method: Spectral Only
   h Pattern Length: Arbitrary
   i ISI Filter Lead: -2
   j ISI Filter Lag: 18

Expected / Observable Results

The measurement results for Total Jitter, Deterministic Jitter, Eye Width and Extrapolated Eye Height must be within the conformance limit as specified in the USB 3.2 specification.

10G Far End Template Test and 10G Far End Differential Output Voltage Test

Test Condition

Test Method
SDA

Test Procedure

1 Set up the stimulus for 2-cycle LFPS ping.
2 Default the scope.
3 Setup Function 1 as subtraction of Channel 1 and Channel 3.
4 Set horizontal scale to 2ns, position at 0.
5 Ping the DUT until CP9 is attained.
6 Setup the Acquisition
   - *a* Select Sampling Mode as “Real Time”
   - *b* Set interpolation to OFF
   - *c* Sample rate to 80GSa/s
   - *d* 16M points
7 Setup InfiniiSim. See Appendix A, “InfiniiSim Setup for 10G” for settings.
8 Set Sweep as AUTO.
9 Setup horizontal scale to 20us, position at 0.
10 Stop the acquisition and save the waveform.
11 Setup CTLE:
   - *a* # of Poles: USB3.2
   - *b* Pole 1 Frequency: 1.5GHz
   - *c* Pole 2 Frequency: 5.0GHz
   - *d* AC Gain:1.413
   - *e* DC Gain: 10^(DC/20) (See “10G Eye Measurement Test” on page 95 for the optimum value of DC)
12 Setup Clock Recovery:
   2nd order PLL, data rate of 10Gbps, loop bandwidth of 7.5MHz, damping factor of 0.707
13 Enable Mask Test:
   - *a* Load Mask
   - *b* Set Source as CTLE
   - *c* Set Color Grade to ON
   - *d* Set Infinite Persistent to ON
   - *e* Set Mask Scaling:
   - Horizontal Scaling: -50ps
   - Delta: 100ps
   - *f* Set Mask Vertical Scaling:
   - 1 Level: 600mV
   - 0 Level: -600mV
   - *g* Enable “Bind 1 & 0 Levels”
   - *h* Enable “Real-Time Eye”

14 For DFE setup, click the DFE tab:
   a Set CTLE as the source
   b # of DFE taps: 1
   c Gain: 1
   d Upper Target & Lower Target = ±25mV
   e In the Auto Set section, set Max Tap Value = 1.0
   f Set Min Tap value = 0.0
   g Set Tap 1 value = 1
   h Select to check Enable DFE
   i Fill in the Delay to adjust the position of the waveform
   j Note the following acronyms:
      i T = Unit-less Tap value
      ii U = Upper target
      iii L = Lower target
      iv A = Amplitude
      v O = Offset
      vi A = (U-L)/2
      vii O = (U+L)/2
      viii U & L = ±50mV; Tap = 1 is equal to U & L = ±1; Tap = 0.5

Bit (0-1)	V
1	V = O + A * (T1 * 1)
0	V = O + A * (T1 * -1)

15 Run Mask Test.
16 Measure Eye Height and Eye Width.

Expected / Observable Results

The signal must pass the Mask Test and the Differential Output Voltage must be within the conformance limits as specified in the USB 3.2 specification.

10G Transmitter Eye Short Channel Tests

The 10G Transmitter Eye Short Channel Tests include:

- 10G Short Channel Template Test
- 10G Short Channel Differential Output Voltage
- 10G Short Channel Extrapolated Eye Height Test
- 10G Short Channel Minimum Eye Width Test

This section provides the Methods of Implementation (MOIs) for 10G Transmitter Eye Short Channel tests using a Keysight 90000A Series Infiniium oscilloscope, USB 3.0 test fixture, and USB3.2 Test Compliance Application.

Connection Diagram See Appendix A, “Test Connection”.

Test Reference from the Specification Table 6-16 and Table 6-20 of the USB 3.2 Specification, revision 1.0.

Table 6-20. Normative Transmitter Eye Mask at Test Point TP4

Signal Characteristic	5GT/s		10GT/s		Units	Note
	Minimum	Maximum	Minimum	Maximum		
Eye Height	100	1200	70	1200	mV	2, 3, 4
Dj		0.43		0.530	UI	1, 2, 3
Rj		0.23		0.141	UI	1, 5, 6
Tj		0.66		0.671	UI	1, 2, 3

Notes:

1. Measured over 10^6 consecutive UI and extrapolated to 10^{-12} BER.
2. Measured after receiver equalization function.
3. Measured at end of reference channel and cables at TP4 in Figure 6-20.
4. The eye height is to be measured at the minimum opening over the range from the center of the eye ± 0.05 UI.
5. The Rj specification is calculated as 14.069 times the RMS random jitter for 10^{-12} BER.
6. Measured at the output of the compliance breakout board without embedding the compliance cable and load board.

Figure 73 Table 6-20 of USB 3.2 Specification Version 1.0

NOTE According to the USB 3.2 Specification, Version 1.0 CTS, the Eye Width and the Extrapolated Eye Height measurement requires computing the Data Eye using CP9 using Rj as input from the CP10 waveform and compare it against requirements for a 70mV Eye Height and a 48.0ps Eye Width both at 10E-6 BER.

6.8.2.2.2 Reference DFE

In addition to the 1st order CTLE, a one-tap reference DFE is used in transmitter compliance testing. The DFE behavior is described by equation (15) and Figure 6-29. The limits on d_1 are 0 to 50mV.

(15) $$y_k = x_k - d_1 \operatorname{sgn}(y_{k-1})$$

where y_k is the DFE differential output voltage

y^*_k is the decision function output voltage, $|y^*_k| = 1$

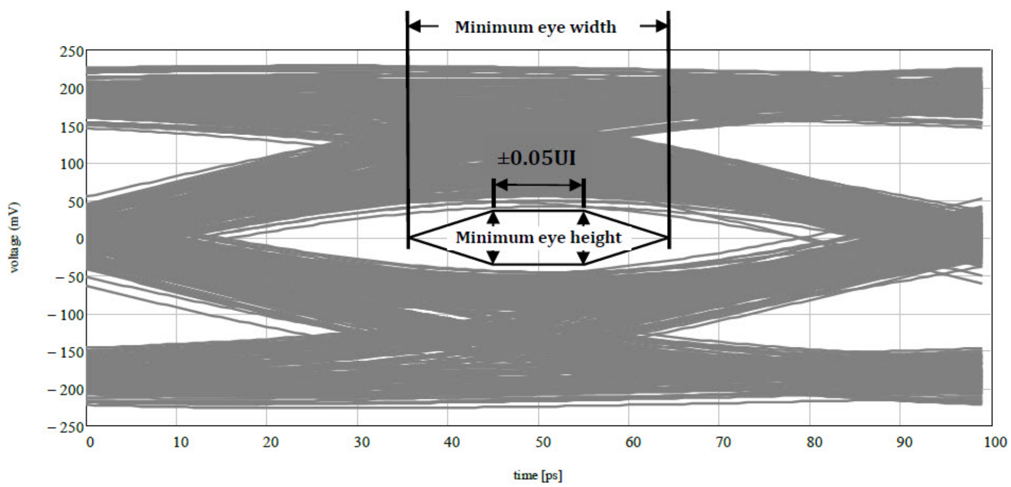
x_k is the DFE differential input voltage

d_1 is the DFE feedback coefficient

k is the sample index in UI

Figure 74 Equation for Reference DFE

Figure 6-17. Eye Masks



Gen 2 eye mask

Figure 75 Gen 2 Eye Mask for 10G Transmitter Short Channel tests

10G Short Channel Template Test, 10G Short Channel Differential Output Voltage, 10G Short Channel Extrapolated Eye Height and 10G Short Channel Minimum Eye Width

Test Conditions

Test Method
USB-IF SigTest

Test Procedure

1 Set up the stimulus for 2-cycle LFPS ping.
2 Default the scope.
3 Setup Function 1 as subtraction of Channel 1 and Channel 3.
4 Set horizontal scale to 2ns, position at 0.
5 Ping the DUT until CP9 is attained.
6 Setup the Acquisition
  a Select Sampling Mode as “Real Time”
  b Set interpolation to OFF
  c Sample rate to 80GSa/s
  d 16M points
  e Bandwidth to 25GHz
7 Set Sweep as AUTO
8 Setup horizontal scale to 20us, position at 0.
9 Stop the acquisition and save the waveform.
10 Launch SigTest tool.
11 Load the waveform file. Select the options for Technology and Template File as shown in Figure 76.
  a Technology set to ‘USB_3_10GB’
  b Template File set to ‘USB_3_10Gb_CP9_Tx_Short’
  c Set Random Jitter

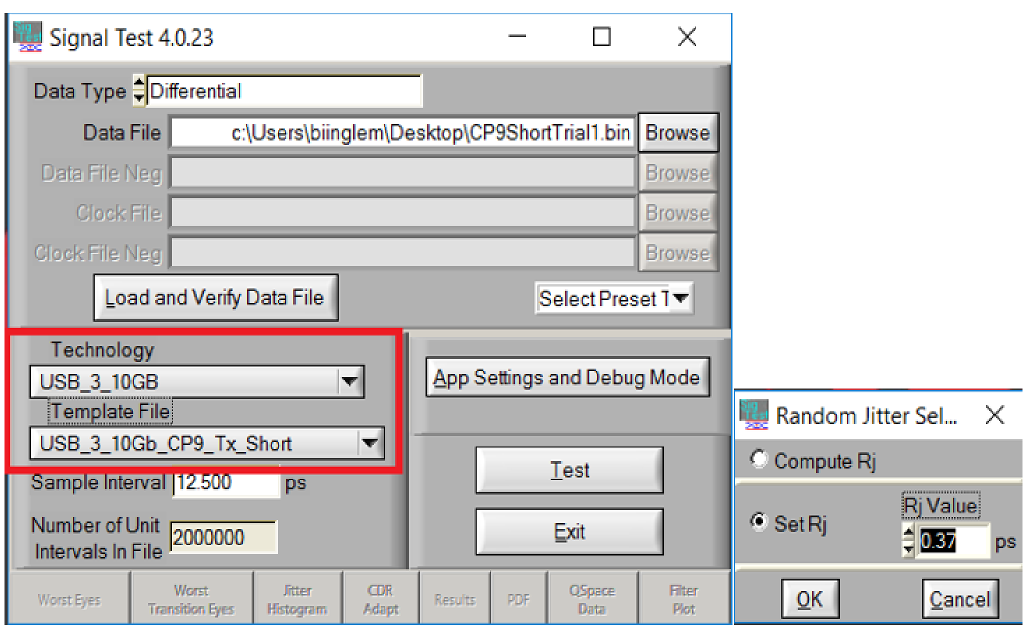


Figure 76 SigTest tool settings for measuring Eye Width and Extrapolated Eye Height

12 Record the measurement result for Eye Width and Extrapolated Eye Height.

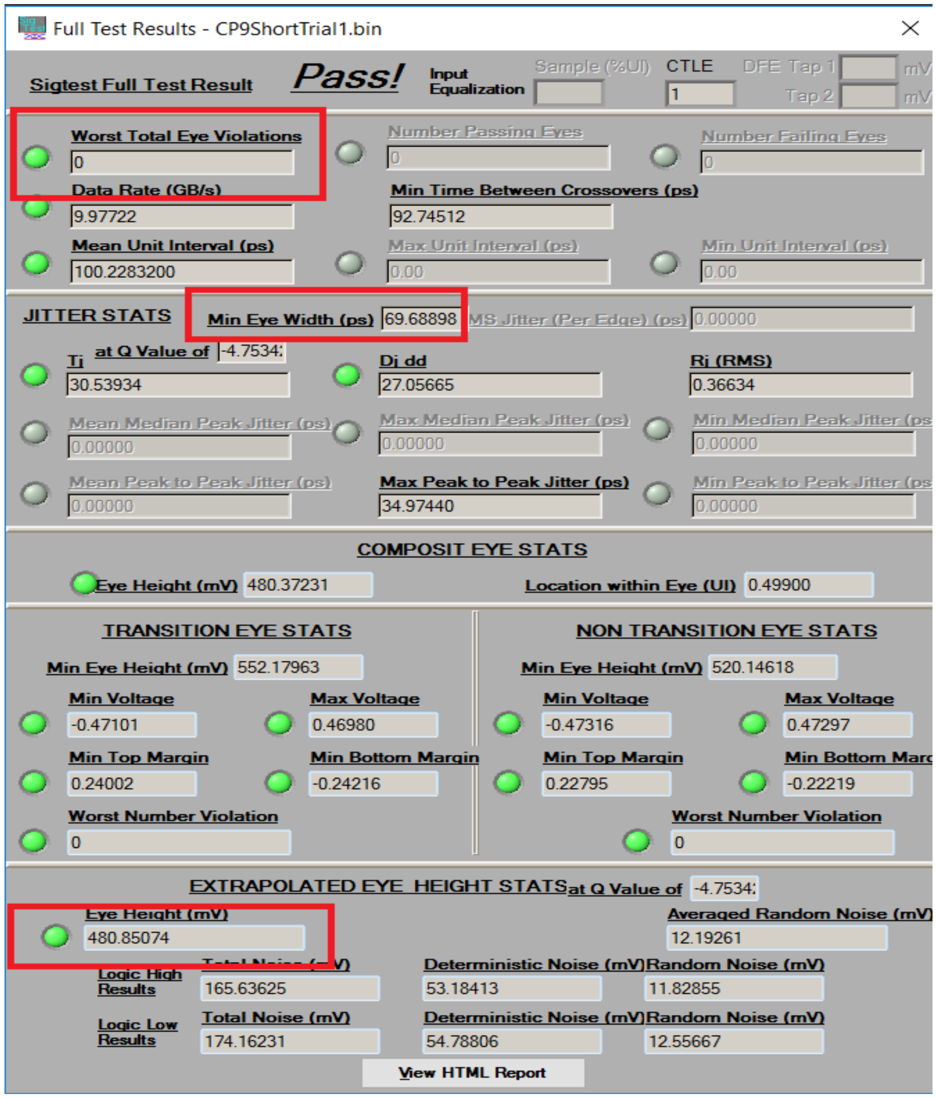


Figure 77 SigTest tool report for Short Channel Eye Width and Extrapolated Eye Height measurement

Expected / Observable Results

The measurement results for Short Channel Eye Width and Extrapolated Eye Height must be within the conformance limit as specified in the USB 3.2 specification.

10G Transmitter Eye Near End (TP0) Tests

The 10G Transmitter Eye Near End (TP0) Tests include:

- 10G Near End Random Jitter
- 10G Near End Maximum Deterministic Jitter Test
- 10G Near End Total Jitter at BER- 6 Test
- 10G Near End Template Test
- 10G Near End Differential Output Voltage

This section provides the Methods of Implementation (MOIs) for 10G Transmitter Eye Near End (TP0) tests using a Keysight 90000A Series Infiniium oscilloscope, USB 3.0 test fixture, and USB3.2 Test Compliance Application.

Connection Diagram

See Appendix A, “Test Connection”.

Test Reference from the Specification

Table 6-16 of the USB 3.2 Specification, revision 1.0.

Table 6-16. Informative Jitter Budgeting at the Silicon Pads[7]

Jitter Contribution (ps)	Gen 1 (5 GT/s)			Gen 2 (10 GT/s)		
	Rj[1,2]	Dj[3]	Tj[4] at 10^{-12}	Rj[1,2]	Dj[3]	Tj[4] at 10^{-12}
Tx[6]	2.42	41	75	1.00	17	31.1
Media[5]	2.13	45	75	0.00	36	36.0
Rx	2.42	57	91	1.00	27.1	41.2
Total	4.03	143	200	1.41	80.1	100

Notes:

1. Rj is the sigma value assuming a Gaussian distribution.
2. Rj Total is computed as the Root Sum Square of the individual Rj components.
3. Dj budget is using the Dual Dirac method.
4. Tj at a 10^{-12} BER is calculated as 14.068 * Rj + Dj.
5. The media budget includes the cancellation of ISI from the appropriate Rx equalization function.
6. Tx is measured after application of the JTF.
7. In this table, Tx jitter is defined at TP1, Rx jitter is defined at TP4, and media jitter is defined from TP1 to TP4.

Figure 78 Table 6-16 of USB 3.2 Specification Version 1.0

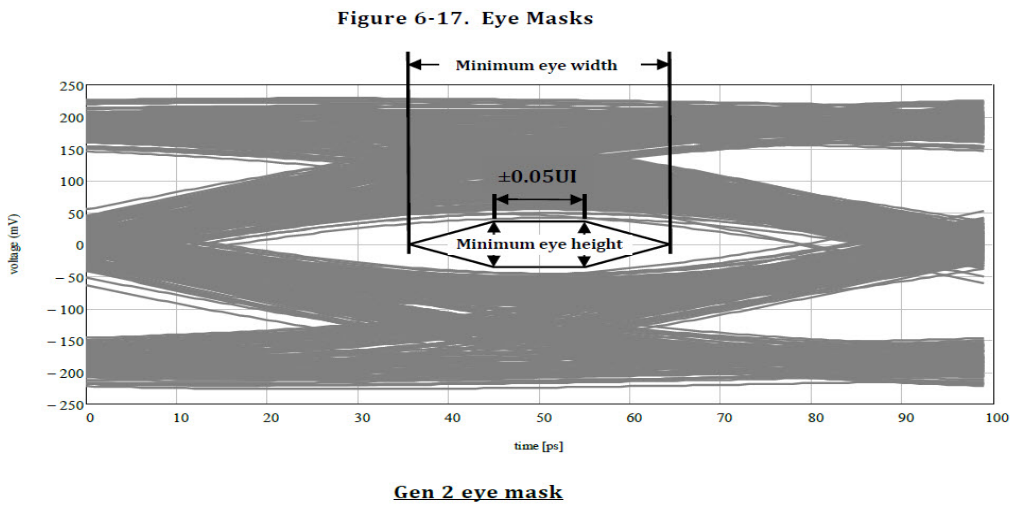


Figure 79 Gen 2 Eye Mask for 10G Transmitter Eye Near End (TP0) tests

10G Near End Random Jitter Test

Test Overview The purpose of this test is to verify that the Near End Random Jitter of the transmitter complies with the specification.

Test Condition

Test Method
SDA

Test Procedure

1 Set up the stimulus for 2-cycle LFPS ping.
2 Default the scope.
3 Setup Function 1 as subtraction of Channel 1 and Channel 3.
4 Set horizontal scale to 2ns, position at 0.
5 Ping the DUT until CP10 is attained.
6 Setup the Acquisition
   a Select Sampling Mode as “Real Time”
   b Set interpolation to OFF
   c Sample rate to 80GSa/s
   d 16M points
   e Bandwidth to 25GHz
7 Set Sweep as AUTO
8 Setup horizontal scale to 20us, position at 0.
9 Stop the acquisition and save the waveform.
10 Setup Clock Recovery:
   2nd order PLL, data rate of 10Gbps, loop bandwidth of 7.5MHz, damping factor of 0.707
11 Setup EZJIT Complete:
   a Set FUNC1 as source
   b Enable Jitter Mode on EZJIT+
   c BER Level: 1E-6
   d Measurement: TIE (Phase)
   e Edges: Both
   f RJ Bandwidth: Narrow
   g RJ Method: Spectral Only
   h Pattern Length: Periodic, Auto
12 Obtain Near End RJ reading.

Expected / Observable Results The measurement results for Near End Random Jitter must be within the conformance limit as specified in the USB 3.2 specification.

10G Near End Maximum Deterministic Jitter and 10G Near End Total Jitter At BER-6 Test

Test Condition

Test Method
SDA

Test Procedure

1 Set up the stimulus for 2-cycle LFPS ping.
2 Default the scope.
3 Setup Function 1 as subtraction of Channel 1 and Channel 3.

4 Set horizontal scale to 2ns, position at 0.
5 Ping the DUT until CP9 is attained.
6 Setup the Acquisition
   a Select Sampling Mode as “Real Time”
   b Set interpolation to OFF
   c Sample rate to 80GSa/s
   d 16M points
7 Set Sweep as AUTO.
8 Setup horizontal scale to 20us, position at 0.
9 Stop the acquisition and save the waveform.
10 Setup Clock Recovery:
   2nd order PLL, data rate of 10Gbps, loop bandwidth of 7.5MHz, damping factor of 0.707
11 Setup EZJIT Complete:
   a Set FUNC1 as source
   b Enable Jitter Mode on EZJIT+
   c BER Level: 1E-6
   d Measurement: TIE (Phase)
   e Edges: Both
   f RJ Bandwidth: Narrow
   g RJ Method: Spectral Only
   h Pattern Length: Arbitrary
   i ISI Filter Lead: -2
   j ISI Filter Lag: 18

Expected / Observable Results

The measurement results for Total Jitter and Deterministic Jitter must be within the conformance limit as specified in the USB 3.2 specification.

10G Near End Template Test and 10G Near End Differential Output Voltage Test

Test Condition

Test Method
SDA

Test Procedure

1 Set up the stimulus for 2-cycle LFPS ping.
2 Default the scope.
3 Setup Function 1 as subtraction of Channel 1 and Channel 3.
4 Set horizontal scale to 2ns, position at 0.
5 Ping the DUT until CP9 is attained.
6 Setup the Acquisition
   a Select Sampling Mode as "Real Time"
   b Set interpolation to OFF
   c Sample rate to 80GSa/s
   d 16M points
7 Set Sweep as AUTO.
8 Setup horizontal scale to 20us, position at 0.
9 Stop the acquisition and save the waveform.
10 Setup Clock Recovery:
   2nd order PLL, data rate of 10Gbps, loop bandwidth of 7.5MHz, damping factor of 0.707
11 Enable Mask Test:
   a Load Mask
   b Set Source as FUNC1
   c Set Color Grade to ON
   d Set Infinite Persistent to ON
   e Set Mask Scaling:
   - Horizontal Scaling: -50ps
   - Delta: 100ps
   f Set Mask Vertical Scaling:
   - 1 Level: 600mV
   - 0 Level: -600mV
   g Enable "Bind 1 & 0 Levels"
   h Enable "Real-Time Eye"
12 Run Mask Test.
13 Measure Eye Height and Eye Width.

Expected / Observable Results

The signal must pass the Mask Test and the Differential Output Voltage must be within the conformance limits as specified in the USB 3.2 specification.

A Appendix

Test Connection

When performing compliance tests, the USB3.2 Test Compliance Application prompts you for proper connections. The connections may appear similar to the diagram showed in Figure 80. Refer to the Connect tab in USB3.2 Test Compliance Application for more details.

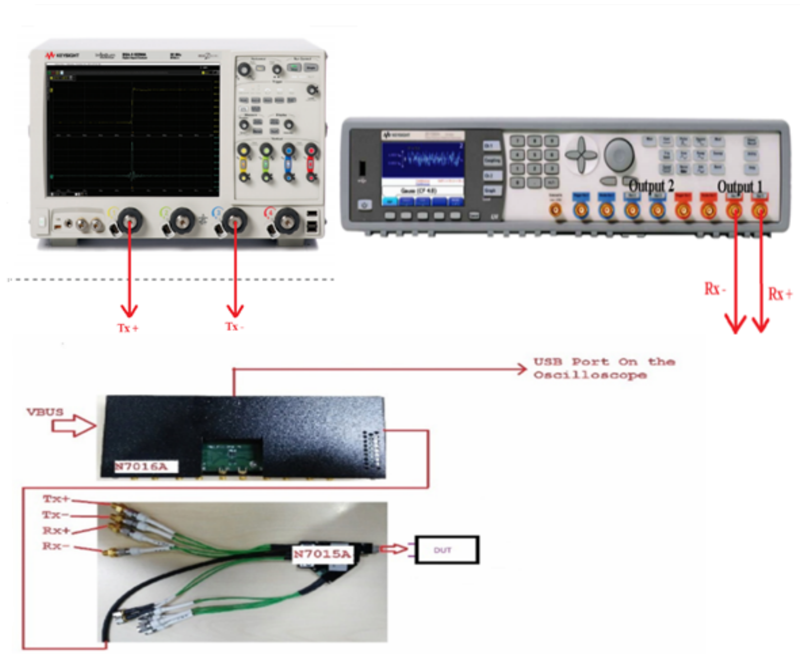


Figure 80 Connection Diagram for various USB 3.2 Compliance Tests

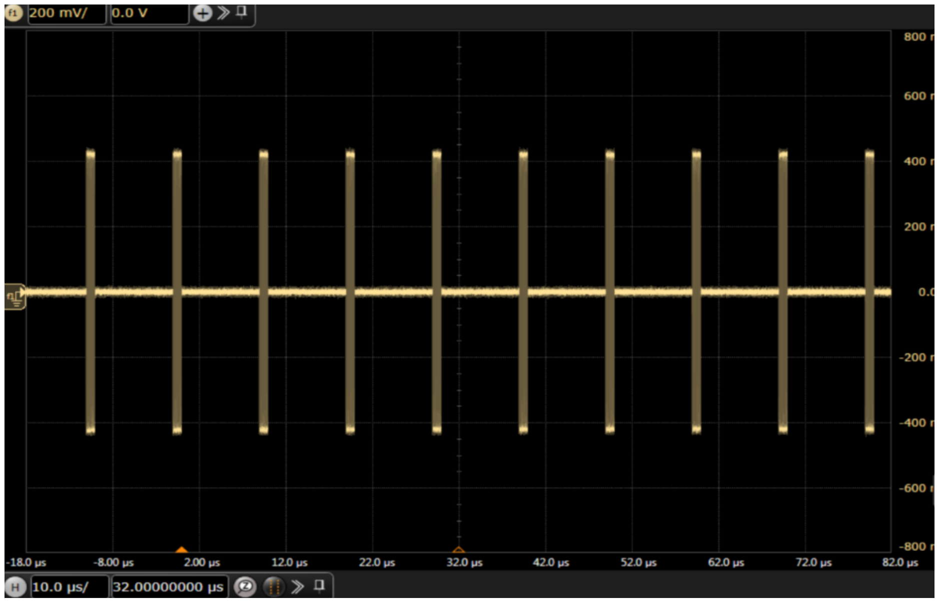
Required fixture for connections

Keysight recommends using the N7015A/N7016A Type-C Test Kit for connections. For more information about this fixture kit, refer to the Keysight N7015A/16A Type-C Test Kit User Guide.

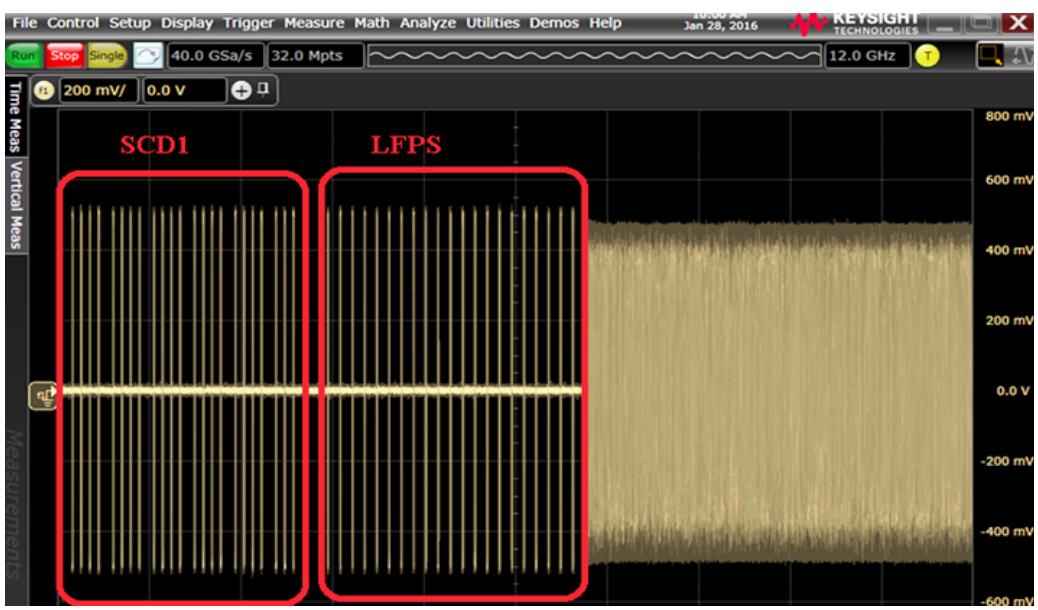
Compliance Pattern used in USB3 Tx Tests

Following images display the compliance patterns acquired or attained during USB3 Tx Tests:

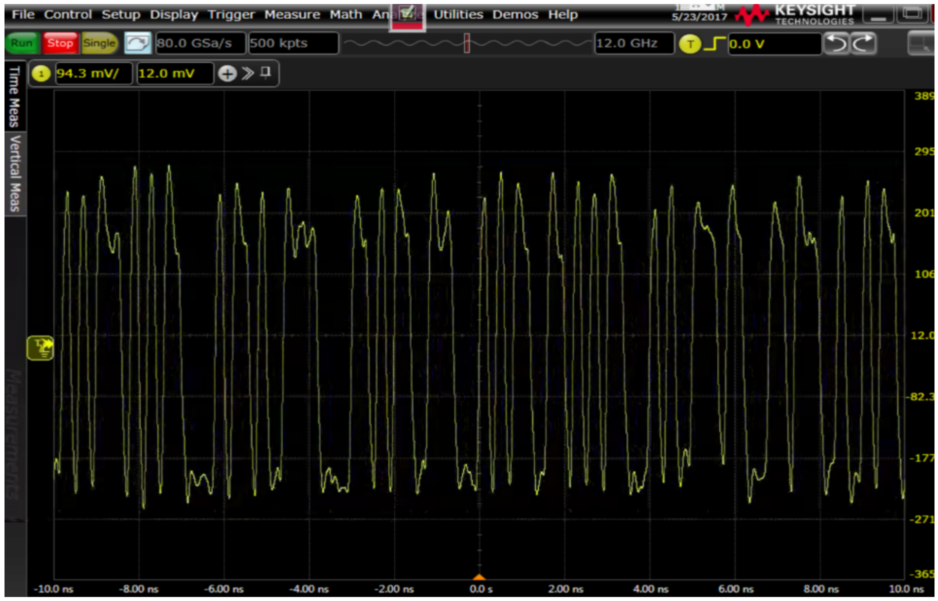
LFPS Pattern in 5G Tests



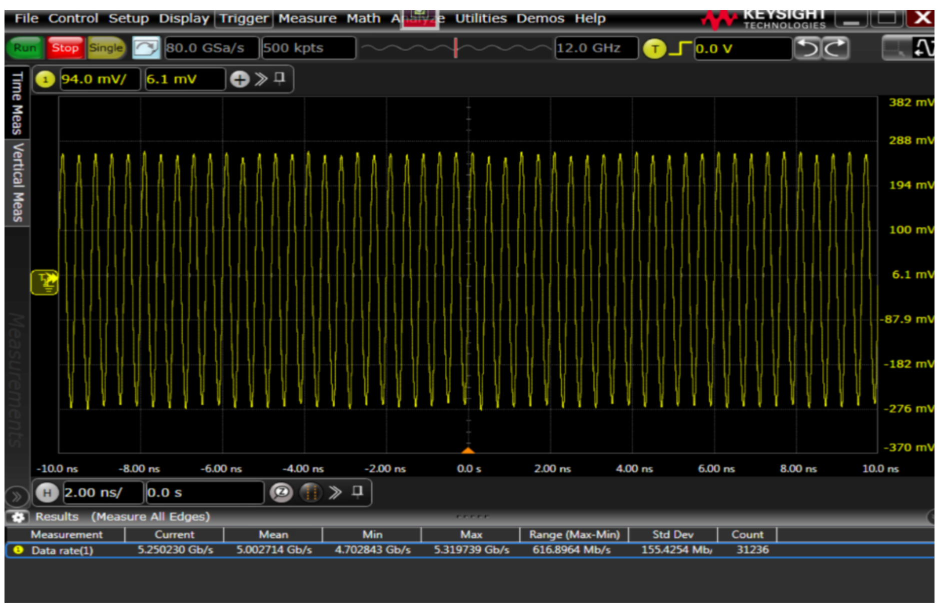
LFPS Pattern in 10G Tests



CP0 Pattern

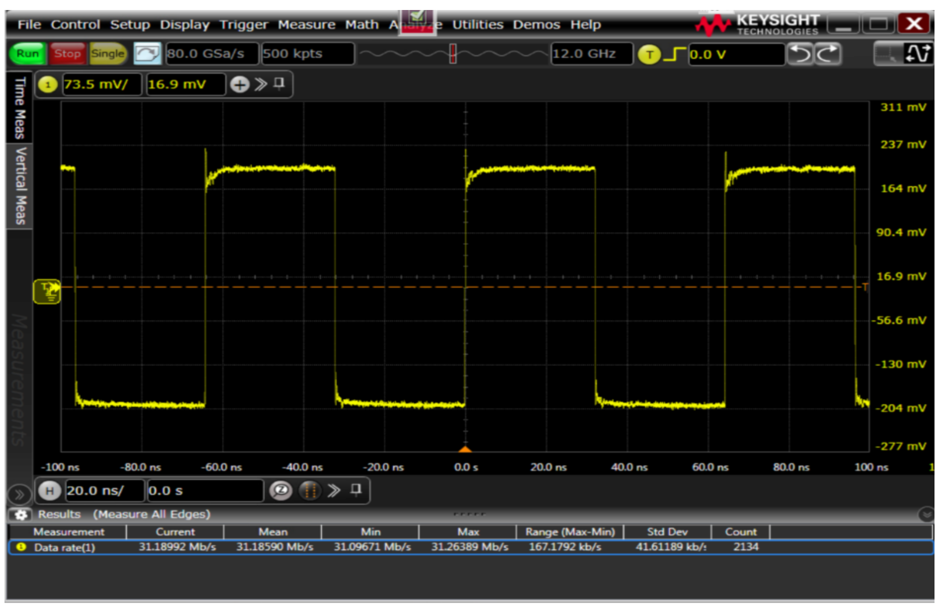


CP1 Pattern



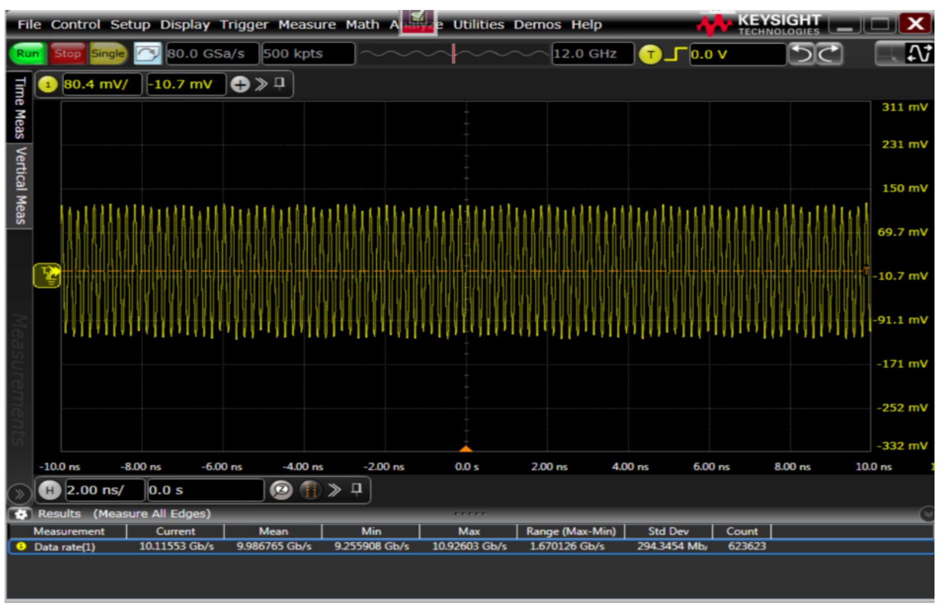
CP7 Pattern

CP8 Pattern



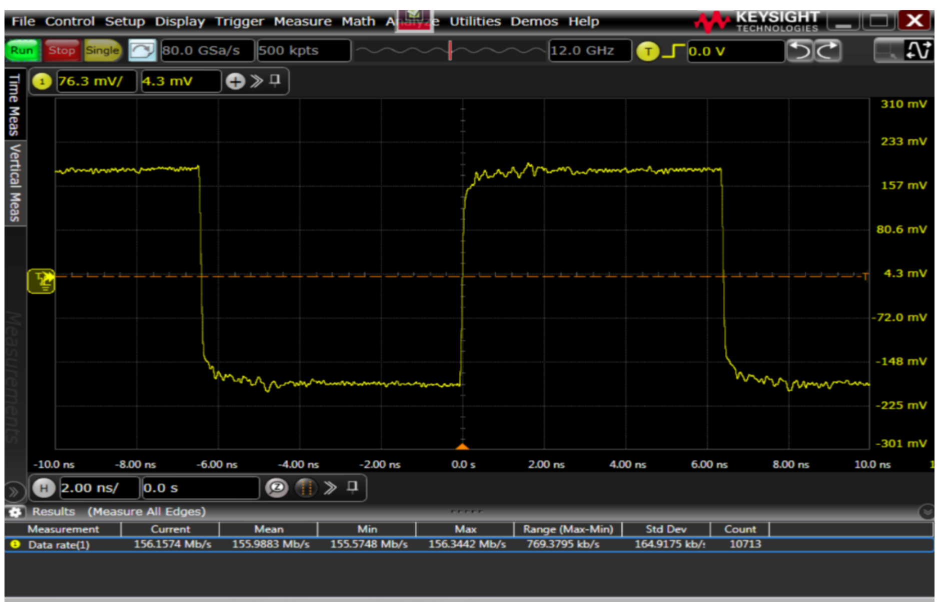
CP9 Pattern

CP10 Pattern



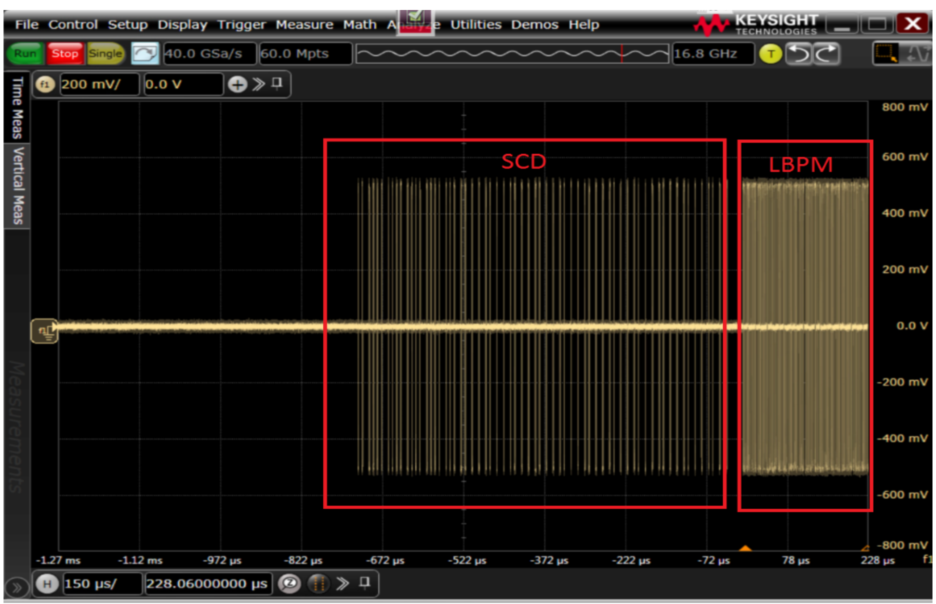
CP13 Pattern

CP14 Pattern



CP15 Pattern

SCD and LBPM Pattern



Compliance Pattern Sequence

Refer to the Table 6-13 of the USB 3.2 Specification, Revision 1.0.

Table 6-13. Compliance Pattern Sequences

Compliance Pattern	Value	Description
CP0	D0.0 scrambled	A pseudo-random data pattern that is exactly the same as logical idle (refer to Chapter 7) but does not include SKP sequences.
CP1	D10.2	Nyquist frequency
CP2	D24.3	Nyquist/2
CP3	K28.5	COM pattern
CP4	LFPS	The low frequency periodic signaling pattern
CP5	K28.7	With de-emphasis
CP6	K28.7	Without de-emphasis
CP7	50-250 1's and 0's	With de-emphasis. Repeating 50-250 1's and then 50-250 0's.
CP8	50-250 1's and 0's	~~With~~ ~~w~~Without de-emphasis. Repeating 50-250 1's and then 50-250 0's.
CP9		Pseudo-random data pattern (see section 6.4.4.1)
CP10	AAh	Nyquist pattern at 10Gb/s. This is not 128b132b encoded.
CP11	CCh	Nyquist/2 at 10Gb/s, This is not 128b132b encoded.
CP12	LFSR15	Uncoded LFSR15 for PHY level testing and fault isolation. This is not 128b132b encoded. The polynomial is x^15+x^14+1.
CP13	64 1's and 0's	With pre-shoot defined in section 6.7.5.2 (no de-emphasis). Repeating 64 1's and then 64 0's at 10Gb/s. This is not 128b132b encoded.
CP14	64 1's and 0's	With de-emphasis defined in section 6.7.5.2 (no pre-shoot). Repeating 64 1's and then 64 0's at 10Gb/s. This is not 128b132b encoded.
CP15	64 1's and 0's	With pre-shoot and de-emphasis defined in section 6.7.5.2. Repeating 64 1's and then 64 0's at 10Gb/s. This is not 128b132b encoded.
CP16	64 1's and 0's	No de-emphasis or pre-shoot. Repeating 64 1's and then 64 0's at 10Gb/s. This is not 128b132b encoded.

Note: Unless otherwise noted, scrambling is disabled for compliance patterns.

Mask Template

The mask template can be located within the folders specified below:

C:\Program Files\Keysight\Infiniium\Apps\USB3Test\app\template

1. USB3 Gen 1 Far End Mask Template
   USB3_0_Template_FarEnd.dat
2. USB3 Gen 1 Near End Mask Template
   USB3_0_Template_NearEnd.dat
3. USB3 Gen 2 Far End Mask Template
   USB3_SSP_Template_FarEnd.dat
4. USB3 Gen 2 Near End Mask Template
   USB3_SSP_Template_NearEnd.dat

InfiniiSim Setup for 5G

Transfer function files can be located within the folders specified below:

C:\Users\Public\Documents\Infiniium\Apps\USB3Test\TransferFunctions

1 De-embed keysight fixture (N7015A)

   a Channel Setting: C to C

   N7015A_Deembed__13p5dbLossAt2p5GHz_Embed.tf4

   b Channel Setting: Captive Device

   N7015A_Deembed__6p5dbLossAt2p5GHz_Embed.tf4

2 De-embed Keysight fixture (U7242A)

   Device Mode

   a Channel Setting: Std A to Std B

   U7242A_Deembed__USB3_TX_Device_Channel.tf4

   b Channel Setting: Std A to Micro B

   U7242A_Deembed__USB3_MicroB_Channel.tf4

   c Channel Setting: Tethered

   U7242A_Deembed__USB3_Tethered_Channel.tf4

   Host Mode

   a Channel Setting: Std A to Std B

   U7242A_Deembed__USB3_TX_Host_Channel.tf4

   b Channel Setting: Micro AB

   U7242A_Deembed__USB3_MicroAB_Channel.tf4

3 De-embed USBIF fixture

   a Std A to Std B

   USB3_TX_Device_Channel.tf4

   b Std A to Micro B

   USB3_MicroB_Channel.tf4

   c Tethered

   USB3_Tethered_Channel.tf4

   d Micro AB

   USB3_MicroAB_Channel.tf4

   e C to C

   SSGen1_TxComp12p7dB_Embedding.tf4

   f Captive Device

   SSGen1_TxComp6p5dB_Embedding.tf4

InfiniiSim Setup for 10G

Transfer function files can be located within the folders specified below:

C:\Users\Public\Documents\Infiniium\Apps\USB3Test\TransferFunctions

1 De-embed keysight fixture (N7015A)

   a Channel Setting: C to C

   N7015A_Deembed__TypC_TypC_14p1dbAt5GHz_Embed.tf4

   b Channel Setting: Captive Device

   Device Mode

   N7015A_Deembed__Mock_Device_Cascaded_Model_8p5dB_rspl.tf4

   Host Mode

   N7015A_Deembed__Mock_Host_Cascaded_Model_8p5dB_rspl.tf4

2 De-embed USBIF fixture

   a Std A to Std B

   SSGen2_TxComp12p2dB_Embedding.tf4

   b Std A to Micro B

   SSGen2_TxComp12p2dB_Embedding.tf4

   c Std A to C

   SSGen2_TxComp12p2dB_Embedding.tf4

   d C to Std B

   SSGen2_TxComp12p2dB_Embedding.tf4

   e C to Micro B

   SSGen2_TxComp12p2dB_Embedding.tf4

   f C to C

   SSGen2_TxComp12p2dB_Embedding.tf4

   g Captive Device

   Device Mode

   Mock_Device_Cascaded_Model_8p5dB_rspl.tf4

   Host Mode

   Mock_Host_Cascaded_Model_8p5dB_rspl.tf4

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KEYSIGHT TECHNOLOGIES

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