SuperSpeed USB Design Guidelines

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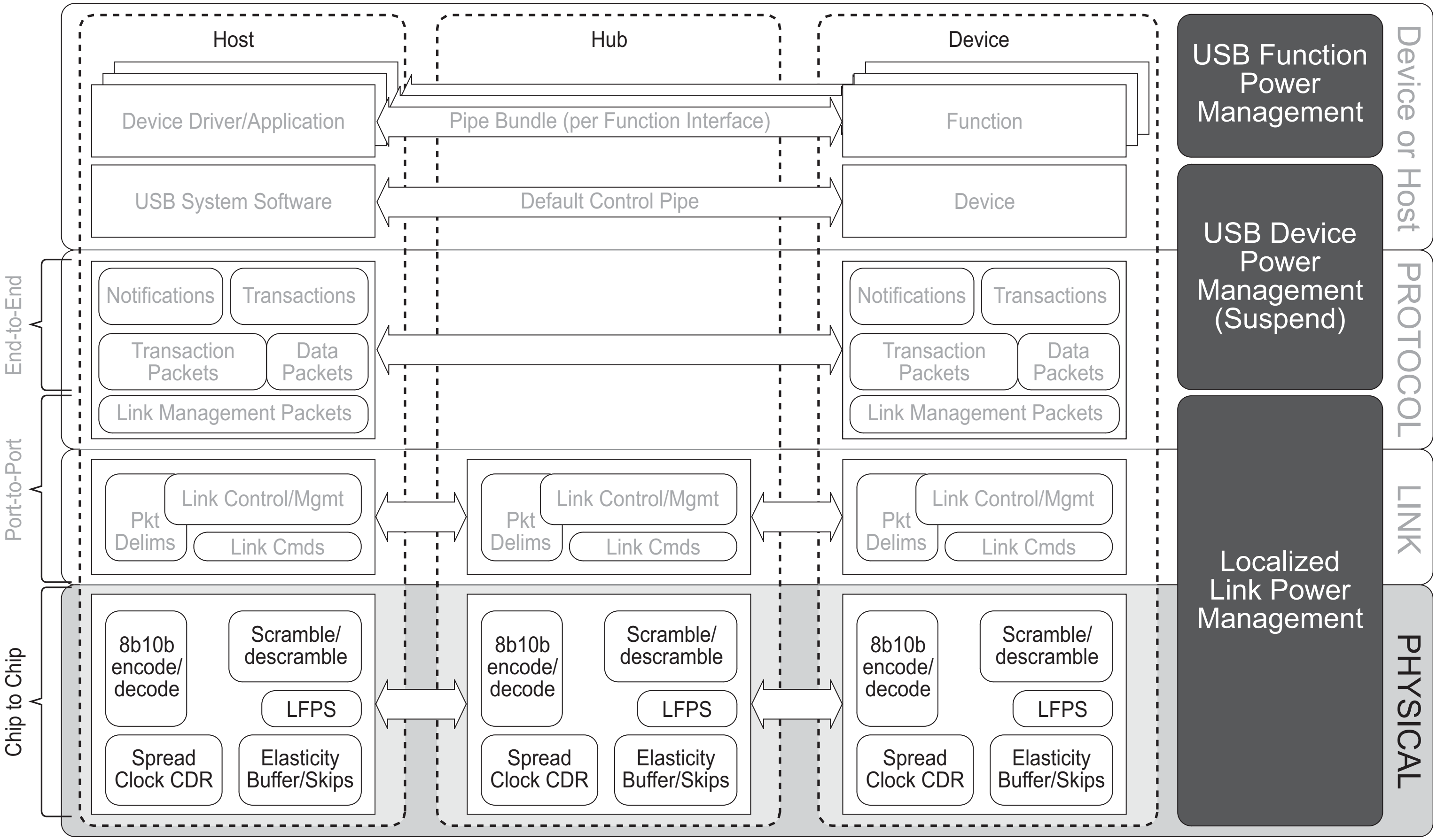
Where Are We?



Host

Hub

Device

Device Driver/Application

Pipe Bundle (per Function Interface)

Function

USB System Software

Default Control Pipe

Device

Notifications

Transactions

Transaction Packets

Data Packets

Link Management Packets

Notifications

Transactions

Transaction Packets

Data Packets

Link Management Packets

Pkt Delims

Link Control/Mgmt

Link Cmds

Pkt Delims

Link Control/Mgmt

Link Cmds

Pkt Delims

Link Control/Mgmt

Link Cmds

8b10b encode/ decode

Scramble/ descramble

LFPS

Spread Clock CDR

Elasticity Buffer/Skips

8b10b encode/ decode

Scramble/ descramble

LFPS

Spread Clock CDR

Elasticity Buffer/Skips

8b10b encode/ decode

Scramble/ descramble

LFPS

Spread Clock CDR

Elasticity Buffer/Skips

End-to-End

Port-to-Port

Chip to Chip

USB Function Power Management

USB Device Power Management (Suspend)

Localized Link Power Management

Device or Host

PROTOCOL

LINK

PHYSICAL

Key Messages

- Design of USB 3.0 hosts and devices requires:
  - Adaptive Rx Equalization (CTLE)
  - Crosstalk minimization through careful routing
  - Control of losses
    - Minimize package and board lengths
    - Minimize via usage & layer transitions
- EMI/ESD mitigation has small routing impact:
  - Used solutions that maintain differential route integrity.
  - Be careful to ensure your “no stuff” options are not worse than stuffed configurations.

Agenda

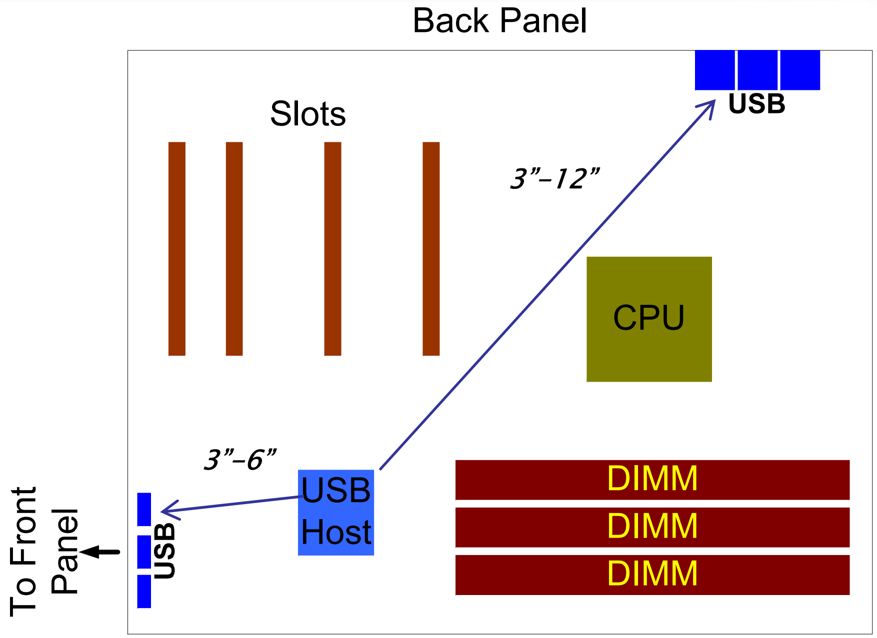
- **System Overview**
  - **Design Challenges**
  - **Physical Layer Overview**
  - **Channel Description**
- Host Design
- Device Design
- Silicon Considerations
- EMI/EMC Design
- Summary

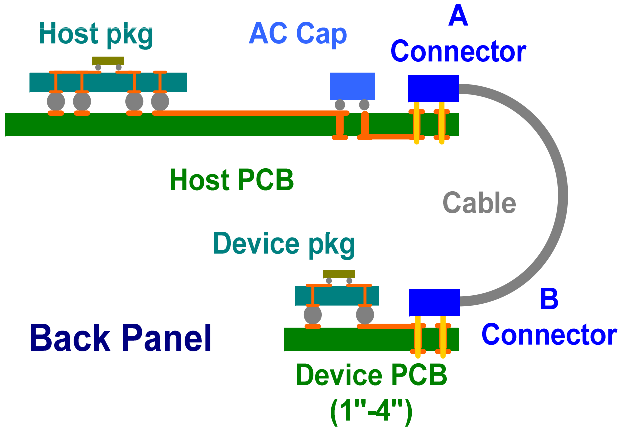
Design Challenges

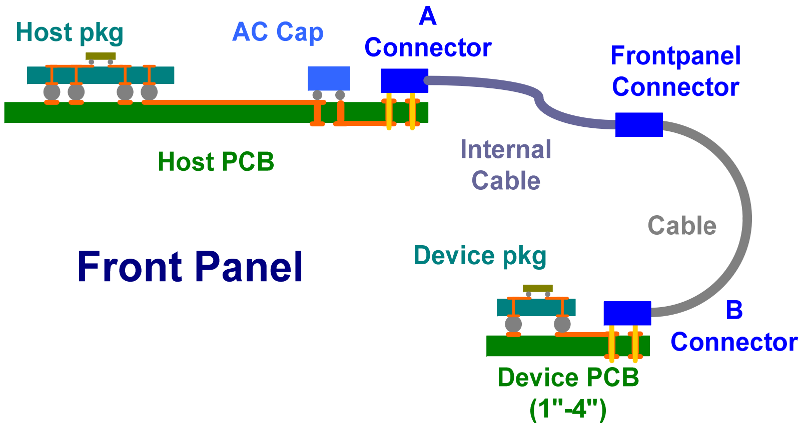
- 5 Gb/s data rate at 10^{-12} BER
- Low cost: 4 layer PCB, extension of USB cable technology
- Same design & usage flexibility as USB 2.0
  - Front panel & back panel connectors, 3 m cable
- Regulatory and Environmental Guidelines
  - EMI/EMC Mitigation: Impact at 5 Gb/s
  - Halogen Free Dielectrics: More crosstalk

Focus: 5 Gb/s SuperSpeed design guidelines

PHY Overview







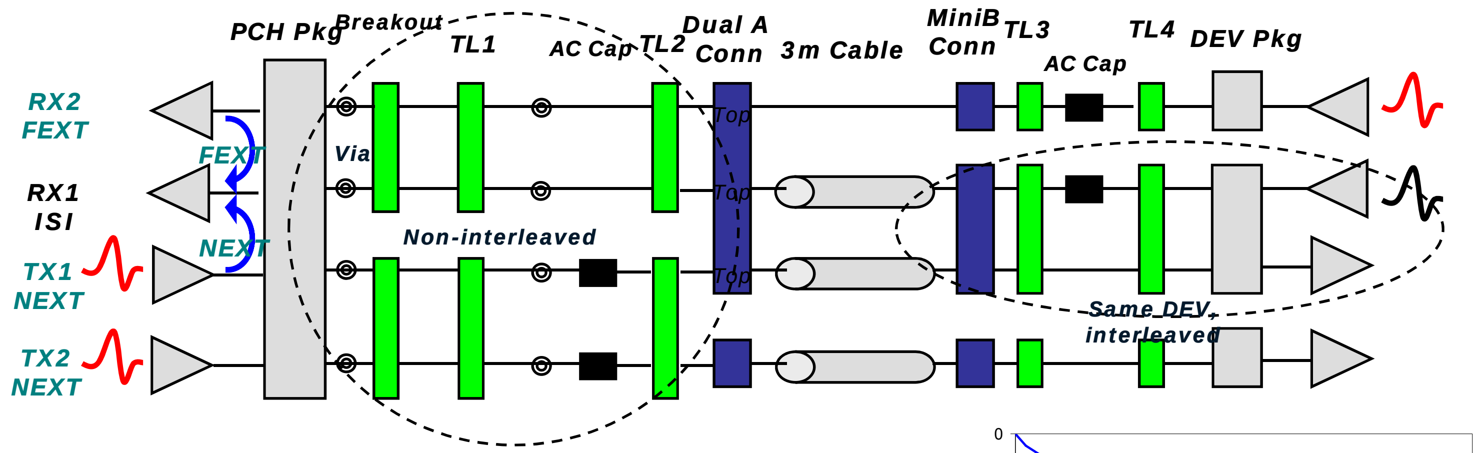
Channel Characteristics

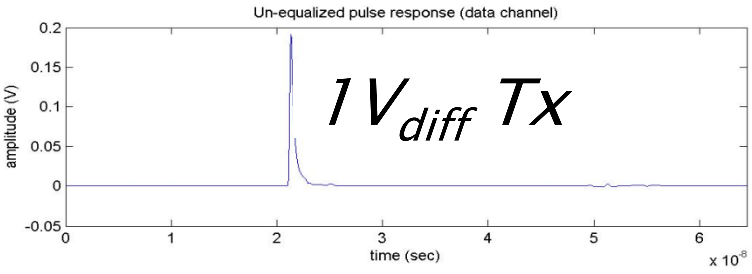
- 2”-12” host PCB length
- 10” to 16” Internal cable (FP)
- 0m to 3m External cable
- 1”- 4” device PCB length

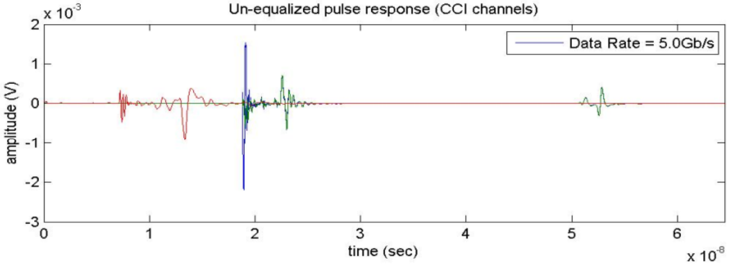
Same channel as 480Mb/s USB 2.0

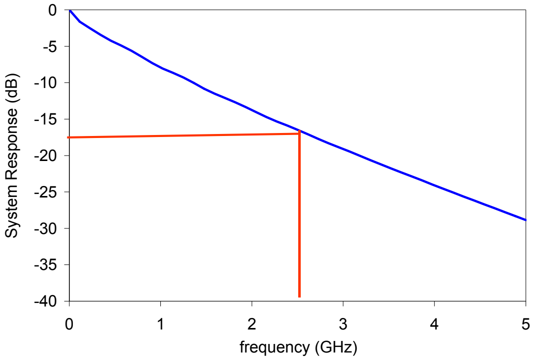
Channel Description

Crosstalk Sources and Attenuation









Key Performance Limiters

- Insertion loss: -6dB to -20dB
- Cable loss: -7.5dB (Spec max)
- Crosstalk: Both NEXT & FEXT

Agenda

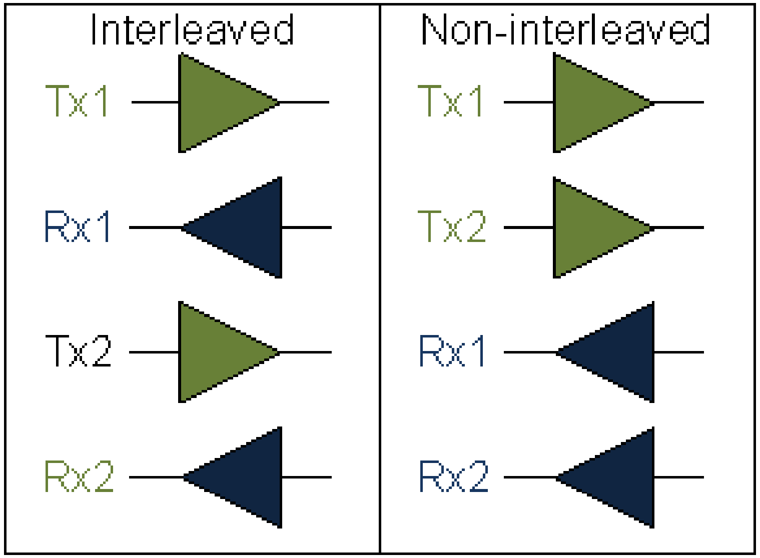
- System Overview
- **Host Design**
  - **Channel Configurations**
  - **Crosstalk Control**
  - **PCB Technology**
  - **Example Design Guidelines**
  - **Link Simulation**
- Device Design
- Silicon Considerations
- EMI/EMC Design
- Summary

Channel Configurations

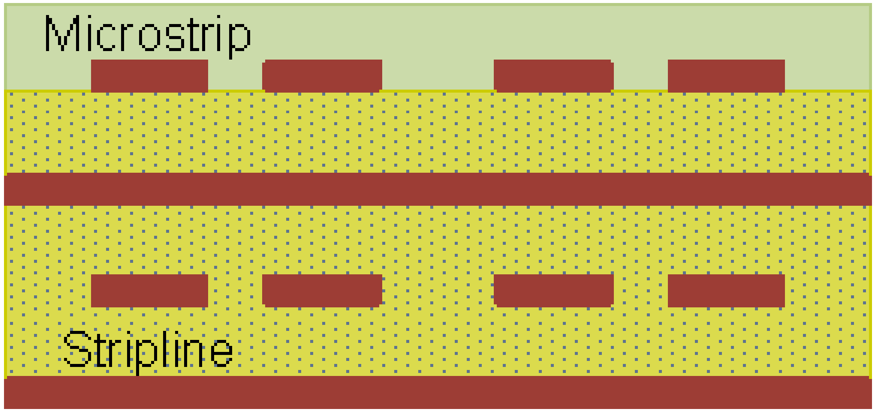
- Desktop Back Panel: Long routes, maximum loss
  - Front Panel: Can be reflective on short channels
- Mobile (Type 3 and Type 4 PCB)
  - Back Panel: Long routes, maximum loss
  - Daughter Card: Cabled or board-to-board
  - Docking: Only Active docks supported
  - ExpressCard II
- Handhelds: Low cost technology, wide impedance ranges, reflections

Smallest margins

Crosstalk



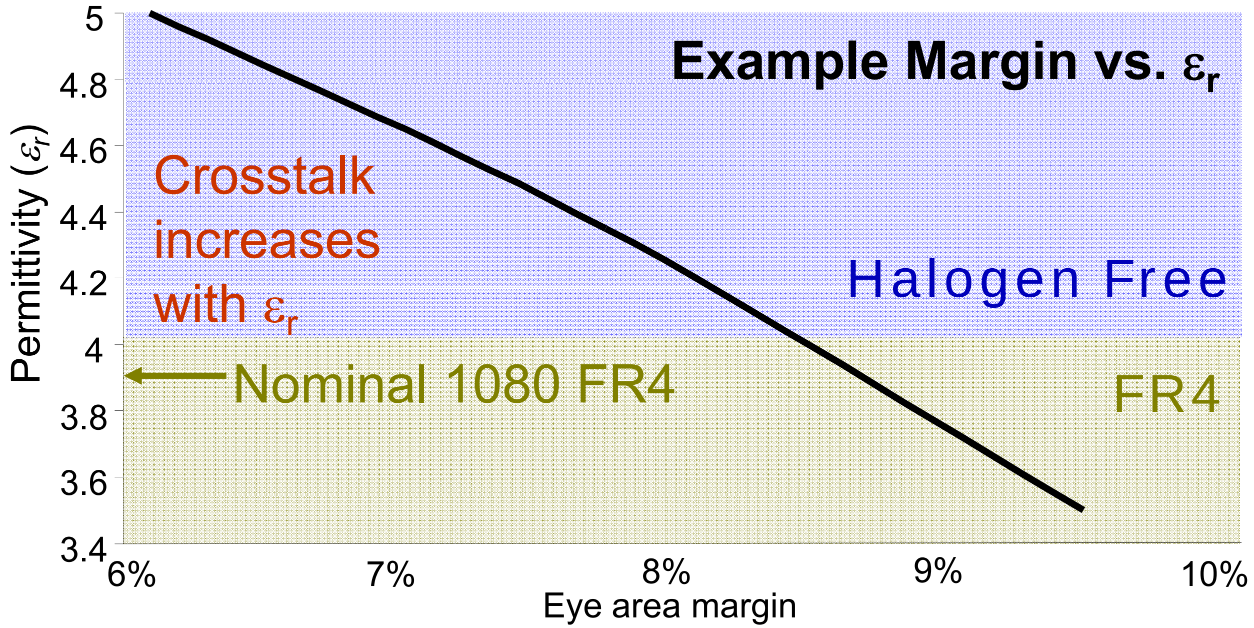
Use semi/non-interleaved routing to minimize near end crosstalk (NEXT).



Use striplines to reduce far end crosstalk (FEXT) of non-interleaved routing.

PCB Design: Halogen Free Dielectric

The industry is moving to Halogen free (HF) dielectric materials...



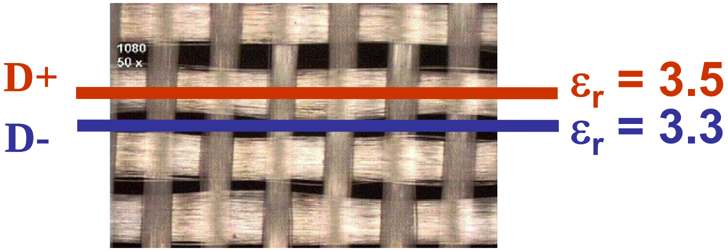
Plan for a margin reduction of 5-10% when switching to HF from FR4.

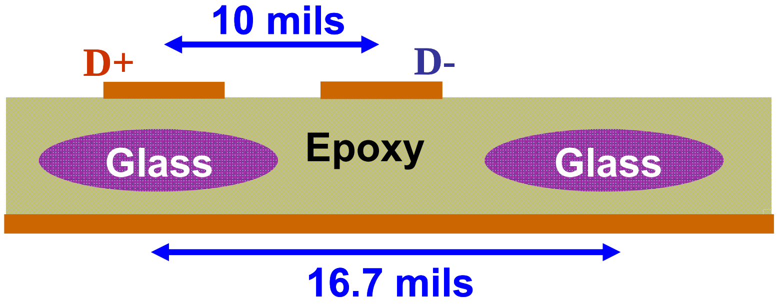
PCB Design: Fiber Weave

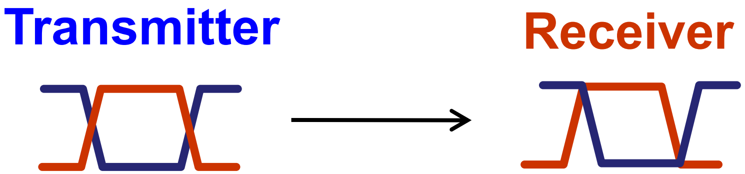
- Local variation in dielectric constant causes differential skew.
- Varying the routing direction helps to cancel the skew.
- Reommendation: Keep *RSS*≤3” (8cm) to minimize the impact of fiber weave.

$$RSS = \sqrt{\sum_i Horizontal^2 + \sum_j Vertical^2}$$

FR4 Glass Cloth w/ Differential Signals

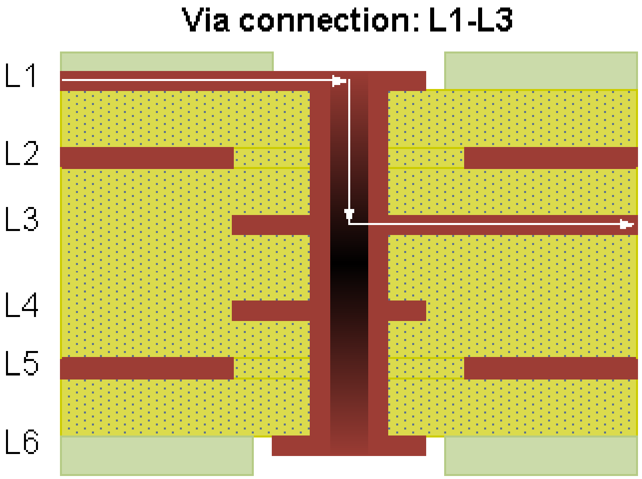






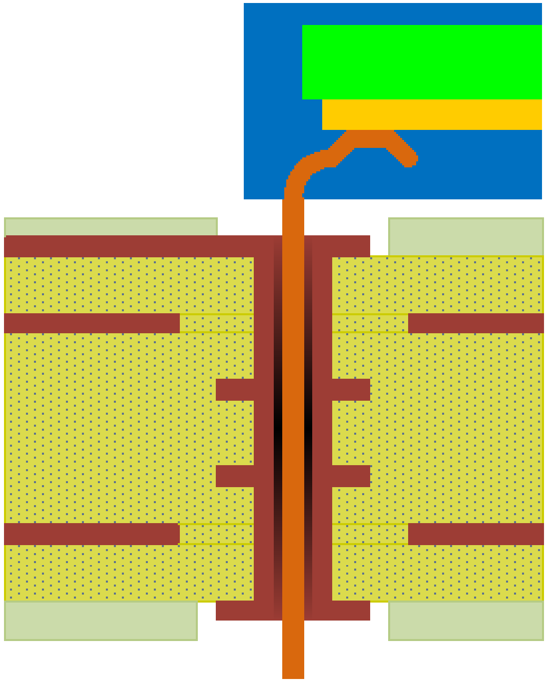
PCB Design: Reflections

Vias



Stub-induced reflections cost up to 1” of routing per via

Connector Entry

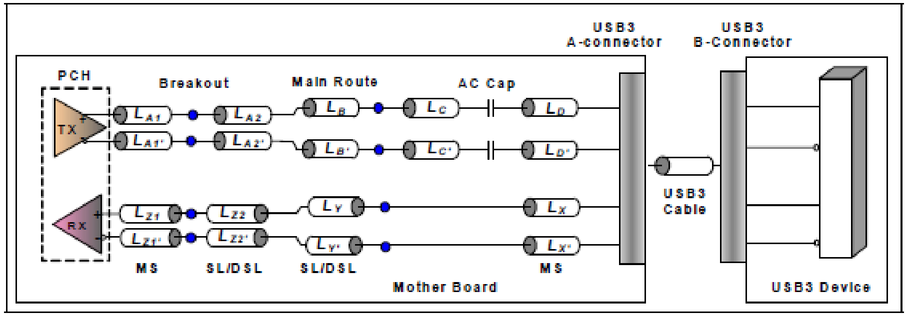


Bottom entry recommended

- Otherwise trade-off: top entry vs. extra via for bottom entry

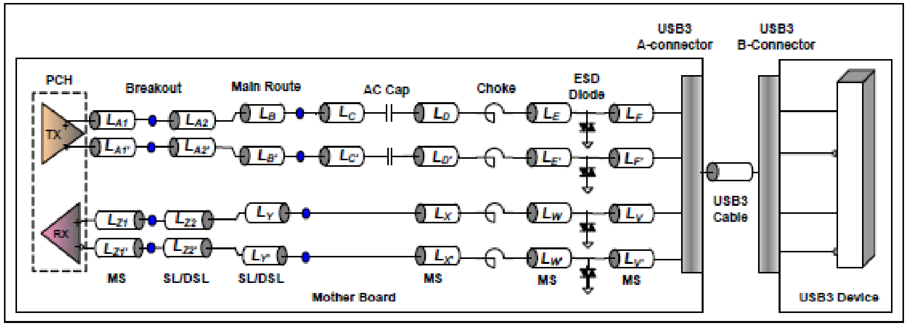
Host Design Example: Mobile Type 3 PCB Guidelines

USB 3.0 External Topology without Choke and ESD Diode



LA1 (PCH Breakout)	MS	LA1+LA2 Max = 600 mils (15.2 mm)
LA2 (PCH Breakout)	SL/DSL	
LB (Main route)	SL/DSL	Max – 8400 mils (213.4 mm)
LC (To AC cap)	MS	Max – 100 mils (2.5 mm)
LD (Io connector)	MS	Max = 900 mils (22.9 mm)
Total Trace Length		LA1+LA2+LB+LC+LD Max = 10000 mils (254.0 mm)

USB 3.0 External Topology with Choke and ESD Diode



LA1 (PCH Breakout)	MS	LA1+LA2 Max = 600 mils (15.2 mm)
LA2 (PCH Breakout)	SL/DSL	
LB (Main route)	SL/DSL	Max = 7400 mils (188.0 mm)
LC (To AC cap)	MS	LC+LD+LE Max = 400 mils (10.2 mm)
LD (To Choke)	MS	
LE (To ESD diode)	MS	
LF (To Connector)	MS	Max = 600 mils (15.2 mm)
Total Trace Length		LA1+LA2+LB+LC+LD+LE+LF **Max = 9000 mils (228.6 mm)**

Host PCB

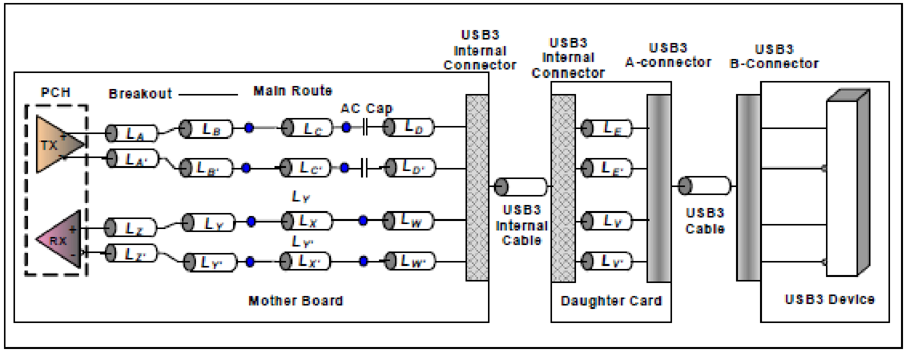
- 8 layer 85Ω stack-up
- 2 vias
- Interleaved or non-interleaved Tx/Rx routing

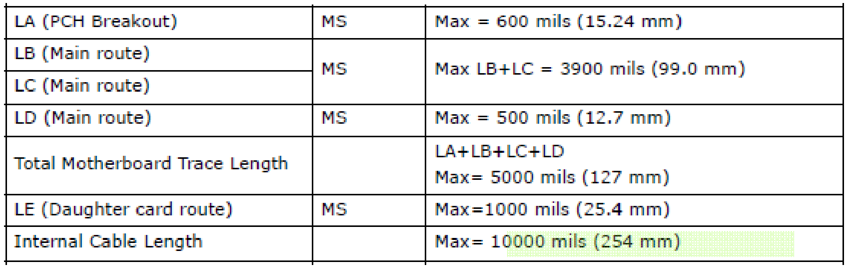
Device PCB

- 2” 85Ω µstrip
- No vias
- Interleaved routing

Host Design Example:
4 Layer Desktop Board

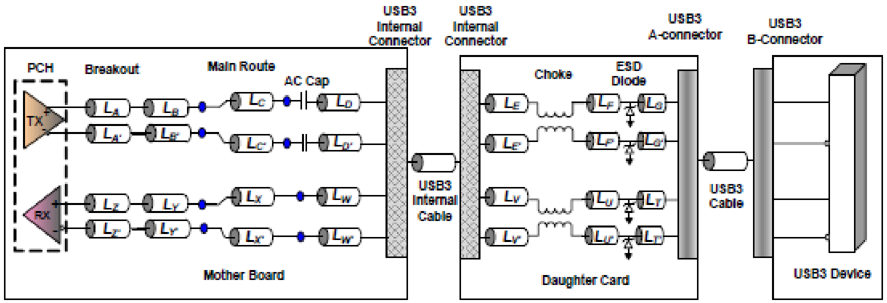
USB 3.0 Frontpanel Topology without Choke and ESD diode

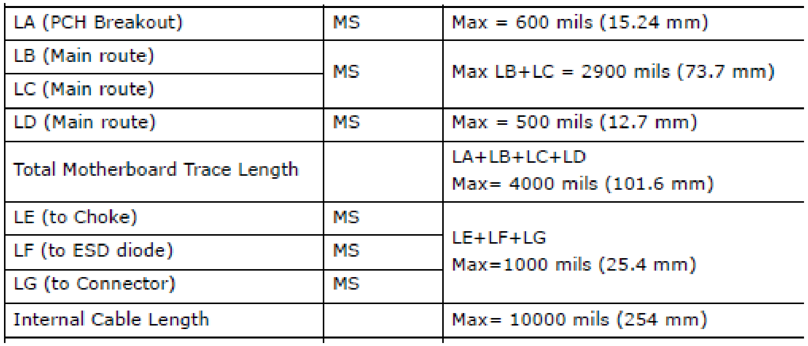




LA (PCH Breakout)	MS	Max = 600 mils (15.24 mm)
LB (Main route)	MS	Max LB+LC = 3900 mils (99.0 mm)
LC (Main route)		
LD (Main route)	MS	Max = 500 mils (12.7 mm)
Total Motherboard Trace Length		LA+LB+LC+LD Max= 5000 mils (127 mm)
LE (Daughter card route)	MS	Max=1000 mils (25.4 mm)
Internal Cable Length		Max= 10000 mils (254 mm)

USB 3.0 Frontpanel Topology with Choke and ESD diode





LA (PCH Breakout)	MS	Max = 600 mils (15.24 mm)
LB (Main route)	MS	Max LB+LC = 2900 mils (73.7 mm)
LC (Main route)		
LD (Main route)	MS	Max = 500 mils (12.7 mm)
Total Motherboard Trace Length		LA+LB+LC+LD Max= 4000 mils (101.6 mm)
LE (to Choke)	MS	LE+LF+LG Max=1000 mils (25.4 mm)
LF (to ESD diode)	MS	
LG (to Connector)	MS	
Internal Cable Length		Max= 10000 mils (254 mm)

Host PCB

- 4 layer 85Ω Z_{diff} stack-up
- 2 vias
- Interleaved or non-interleaved Tx/Rx routing

Device PCB

- 2” 85Ω Z_{diff} µstrip
- No vias
- Interleaved routing

Link Simulation

- Full system (Pad-to-pad)
  - Include crosstalk, variations in package, PCB, and cable.
  - Don’t forget the non-cabled case (flash drive).
- Tx Compliance
  - Drive from host/device into the compliance channel S-parameter & reference CTLE.
  - Compliance channel models are available on the USB-IF website.

Simulate both of these to ensure proper operation.

Agenda

- System Overview
- Host Design
- **Device Design**
- Silicon Considerations
- EMI/EMC
- Summary

Device PCB & Package Design

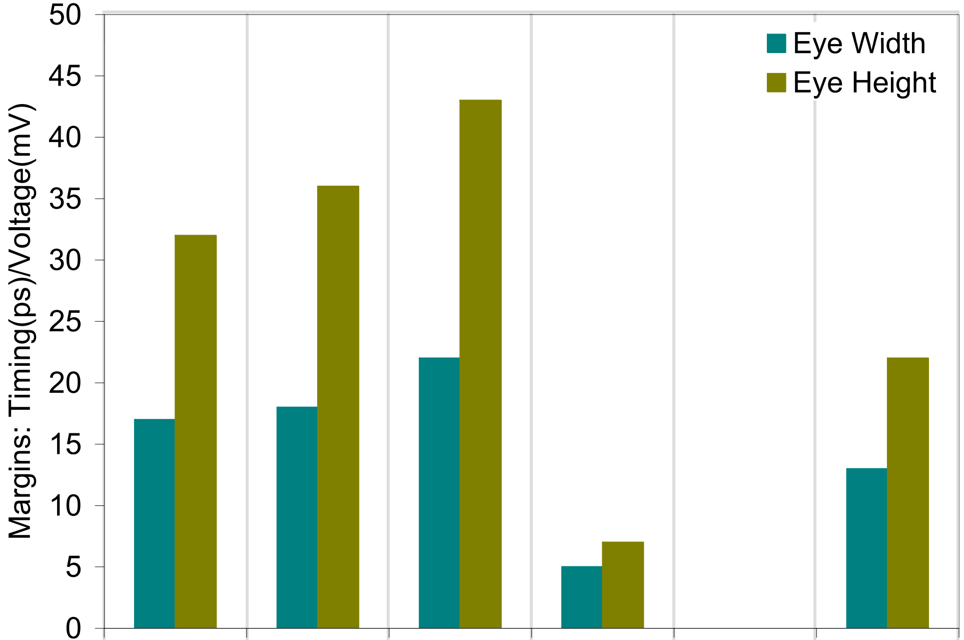
Package

- Minimize trace length.
- Route on different layers or maximize inter-pair spacing.

PCB

- Keep trace length ≤ 2”.
- Route on different layers or 0.040+” between pairs on same layer.

Example Margins



Dev Pkg Interleave	No	No	No	No	Yes	No
Dev PCB Space	0.020”	0.026”	0.040+”	0.020”	0.020”	0.040+”
Host PCB	10.6” trace w/ 2 vias			12.6” w/ 3 vias		

Agenda

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- **Silicon Considerations**
- EMI/EMC Design
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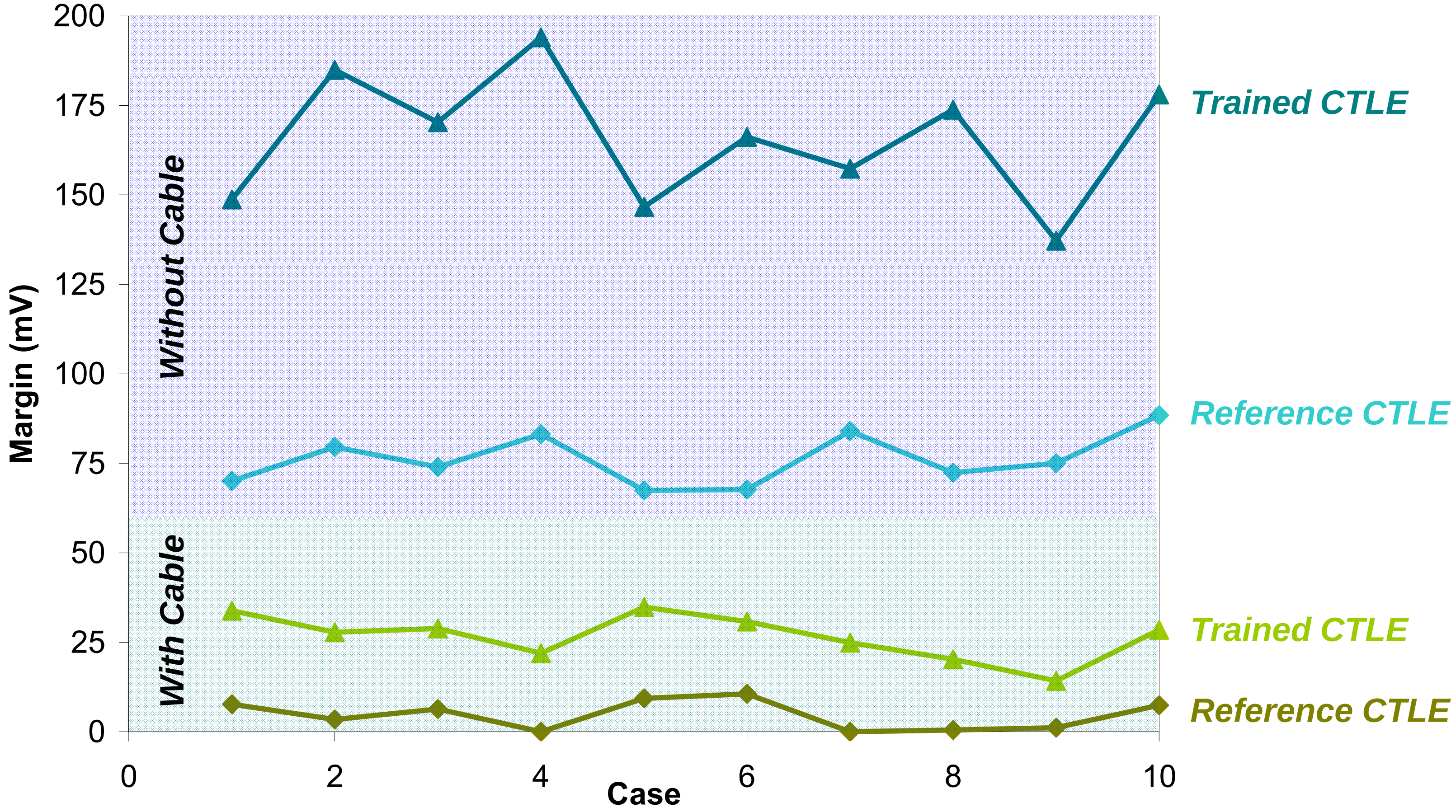
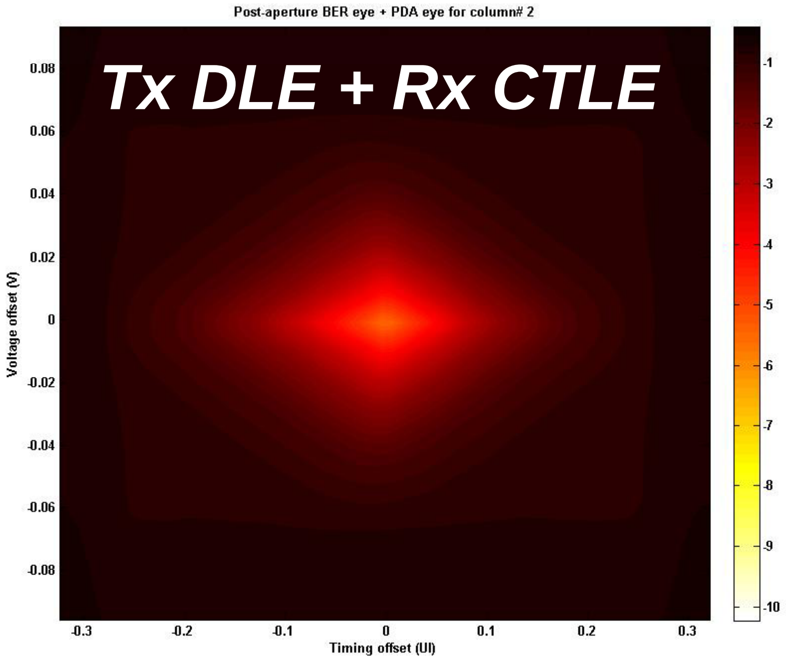
CTLE Training



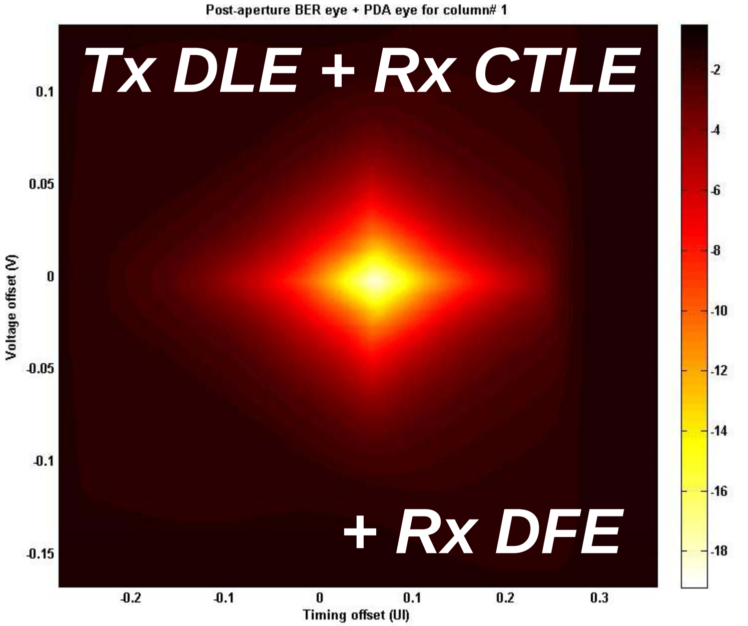
Design your receiver to accommodate a wide range of loss (6dB-20dB) by properly training your equalizer.

Decision Feedback Equalization



While the spec does not require DFE…

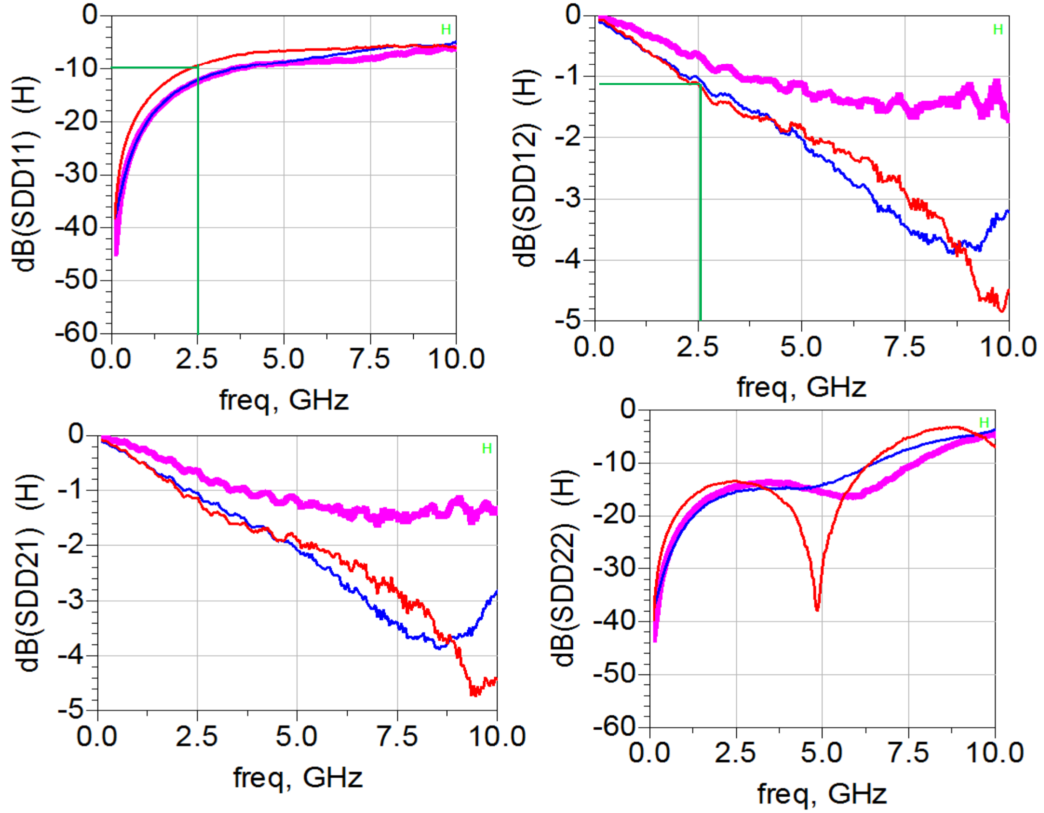
…it improves margin by up to~50mV & 20ps @ 10^{-12} BER.



Agenda

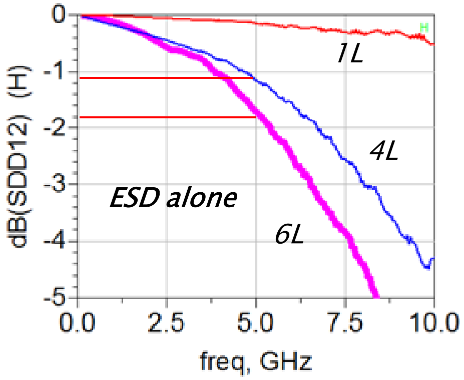
- System Overview
- Host Design
- Device Design
- Silicon Considerations
- **EMI/EMC Design**
  - **Measured Loss Budgets**
  - **Component PCB Void and 0Ω Resistor Impacts**
  - **Component Placement & Routing**
- Summary

EMC Design:
Impact on PCB Length



- 🟥 *4L ESD + CMC "A"*
- 🟦 *1L ESD+ CMC "B" w/Voids*
- 🟪 *1L ESD+ CMC "A"*

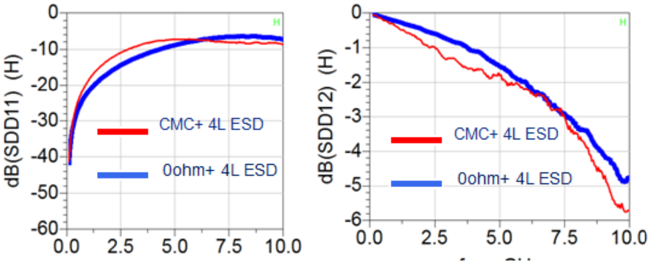
6L ESD is too lossy at harmonics;
∴ greater than 1" route impact



Loss from common mode choke (CMC) + ESD Diode reduces max route length by ~1".

EMC Design Considerations

- Incorporate 100% voids under the CMC and ESD diode signal pads to reduce losses.
- Use 0402 “0” Ω resistors for CMC “no stuff” options.
    - Larger components can be more lossy than the CMC itself and exceed design budgets.



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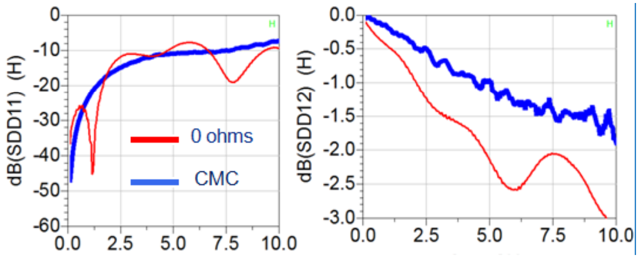

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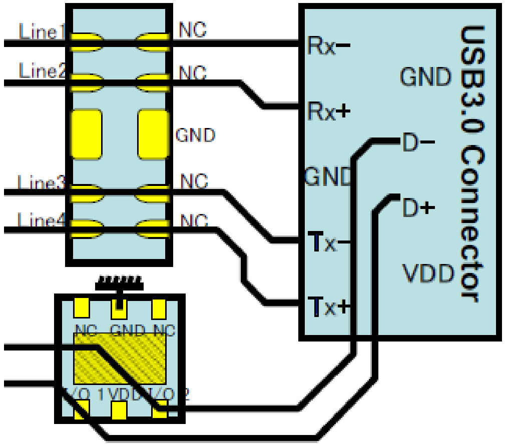
EMC Design: Placement & Routing

- Place EMC components at the USB Connector
  - Back Panel: on Host PCB
  - Front Panel: on the Front Panel Card
  - Recommend Secondary side mounting to avoid connector via stubs
- 4 Lane ESD Diode is the best option
  - Cleanest differential routing - no bends
  - Acceptable network loss when combined with wire wound CMC
  - Better ESD suppression than 1L Ceramics



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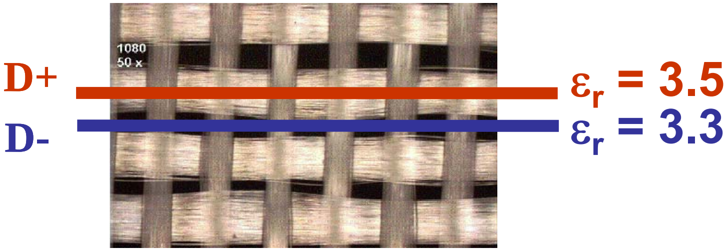
- Design of USB 3.0 hosts and devices requires:
  - Adaptive Rx Equalization (CTLE)
  - Routing to minimize crosstalk minimization
  - Control of losses
    - Minimize package and board lengths
    - Minimize via usage & layer transitions
- EMI/ESD mitigation has small routing impact:
  - Used solutions that maintain differential route integrity.
  - Be careful to ensure your “no stuff” options are not worse than stuffed configurations.

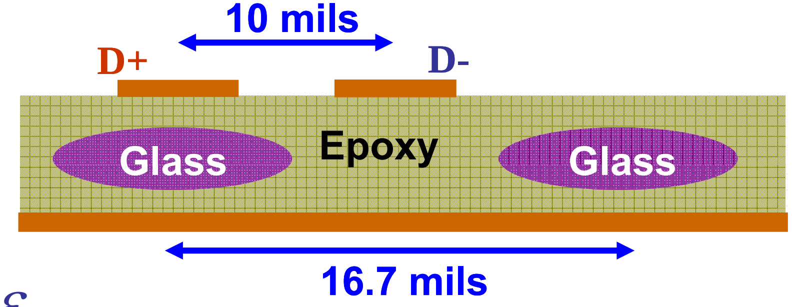
THANK YOU

Common Mode Conversion in PCBs

- **Phenomenon:** Differential pairs see variation in effective dielectric constant due to local non-uniformity. [3]
- **Cause:** ε_r differences between glass (~ 6) & epoxy (~ 3).
  - A line routed over a glass bundle travels more slowly due to the higher ε_r (& vice versa).
  - Converts differential signals to common mode thru electrical length mismatch caused by the ε_r difference.

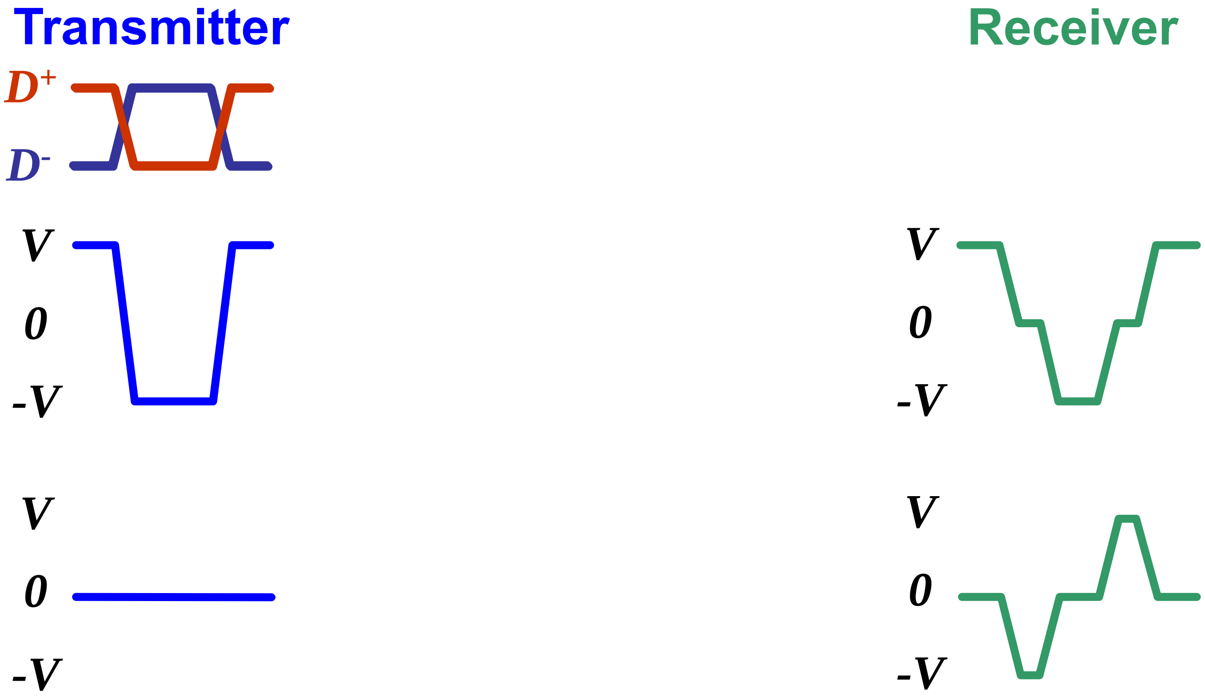
FR4 Glass Cloth w/ Differential Signals





This is sometimes called the “fiber weave” effect

Common Mode Conversion Mechanism



$$V_{diff} = D^{+} - D^{-}$$

$$V_{comm} = \frac{D^{+} + D^{-}}{2}$$

Differential phase skew degrades voltage & timing margins

Fiber Weave Routing Rules

- Horizontal & vertical routed lengths combine via root-sum-of-squares (RSS)
- SuperSpeed USB Recommendation: Keep $length_{RSS} \leq 3''$ (8cm)

$$Length_{RSS} = \sqrt{\sum_i Length_{Horizontal}^2 + \sum_j Length_{Vertical}^2}$$