



WICED Smart Tag Hardware User Manual

BCM920737TAG-04

WICED™ Development System

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920737TAG04-HWUM101-RDS

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Revision History

Revision	Date	Change Description
920737TAG04-HWUM101-R	08/27/15	Updated: <ul style="list-style-type: none">• “Board Layout” on page 9• “Configurable Resistor Descriptions” on page 13
920737TAG04-HWUM100-R	06/23/15	Initial release

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About This Document

The Broadcom Wireless Internet Connectivity for Embedded Devices (WICED; pronounced "wicked") Smart™ SDK is shipped with the BCM920737TAG-04 evaluation board. This document provides board layout, schematics, and instructions on how to use this board.

This document is for software developers who are using the WICED Smart Development System to create applications for Broadcom Bluetooth Smart devices.

Acronyms and Abbreviations

In most cases, acronyms and abbreviations are defined on first use. For a comprehensive list of acronyms and other terms used in Broadcom documents, go to:

<http://www.broadcom.com/press/glossary.php>.

Document Conventions

The following conventions may be used in this document:

Convention	Description
Bold	User input and actions: for example, type exit , click OK, press Alt+C
Monospace	Code: #include <iostream> HTML: <td rowspan = 3> Command line commands and parameters: w1 [-1] <command>
< >	Placeholders for <i>required</i> elements: enter your <username> or w1 <command>
[]	Indicates <i>optional</i> command-line parameters: w1 [-1] Indicates bit and byte ranges (inclusive): [0:3] or [7:0]

References

The references in this section may be used in conjunction with this document.



Note: Broadcom provides customer access to technical documentation and software through its Customer Support Portal (CSP) and Downloads and Support site (see [Technical Support](#)).

For Broadcom documents, replace the “xx” in the document number with the largest number available in the repository to ensure that you have the most current version of the document.

Document (or Item) Name	Number	Source
Broadcom Items		
[1] <i>WICED Smart™ Quick Start Guide</i>	WICED-Smart-QSG2xx-R	WICED Website

Technical Support

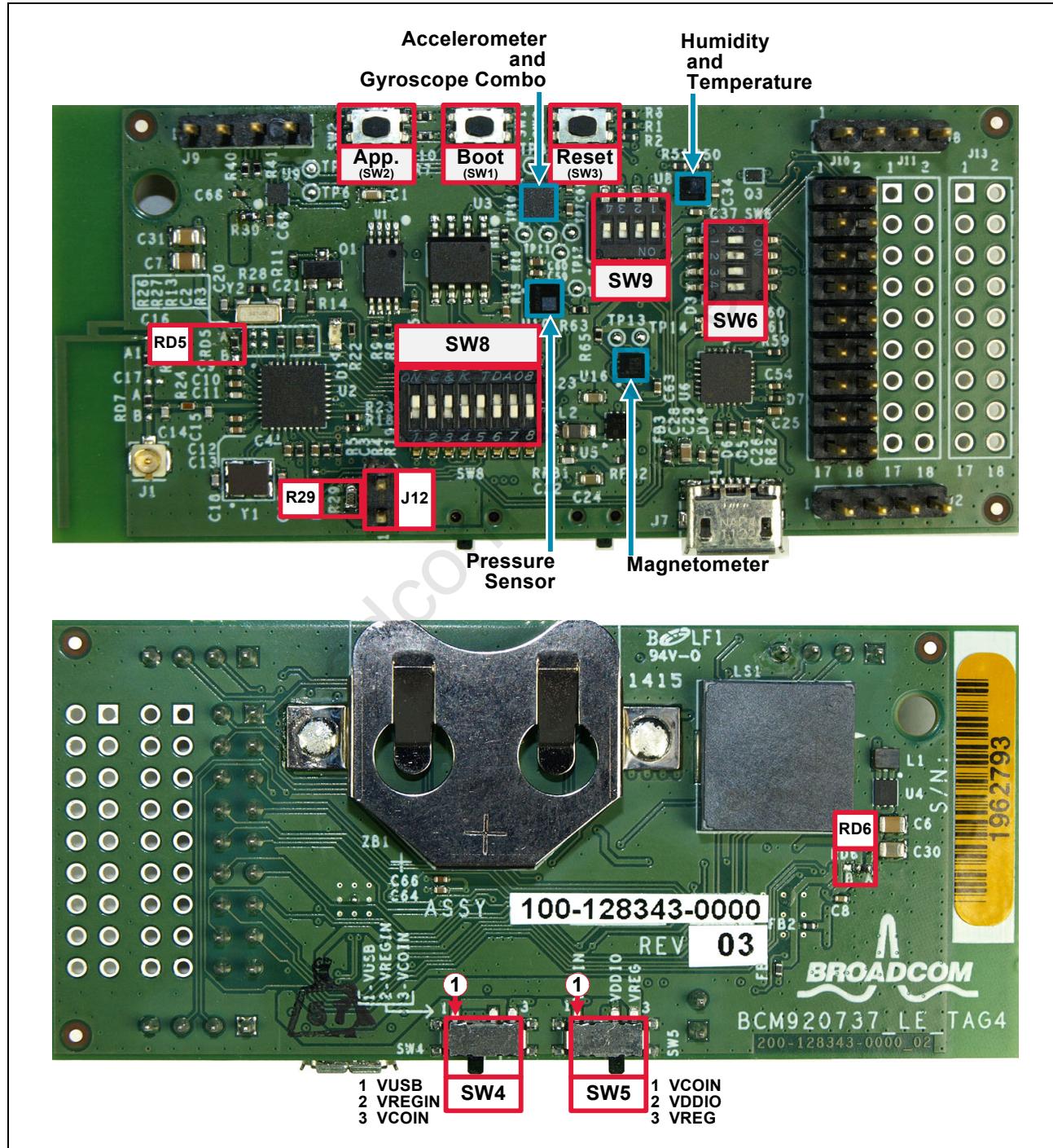
Broadcom provides customer access to a wide range of information, including technical documentation, schematic diagrams, product bill of materials, PCB layout information, and software updates through its customer support portal. For a CSP account, contact your Broadcom Sales or Engineering support representative.

General WICED support is available to registered users in the Broadcom Support Community forum:
<http://community.broadcom.com/welcome>

Product Description

The BCM27036 and BCM20737 are Bluetooth Low Energy (BLE)-compliant, stand-alone baseband processors with integrated 2.4 GHz transceivers. The Broadcom WICED Smart Tag4 (Figure 1) is an evaluation board that makes various pins on the BCM2073X available for debug, evaluation, and troubleshooting.

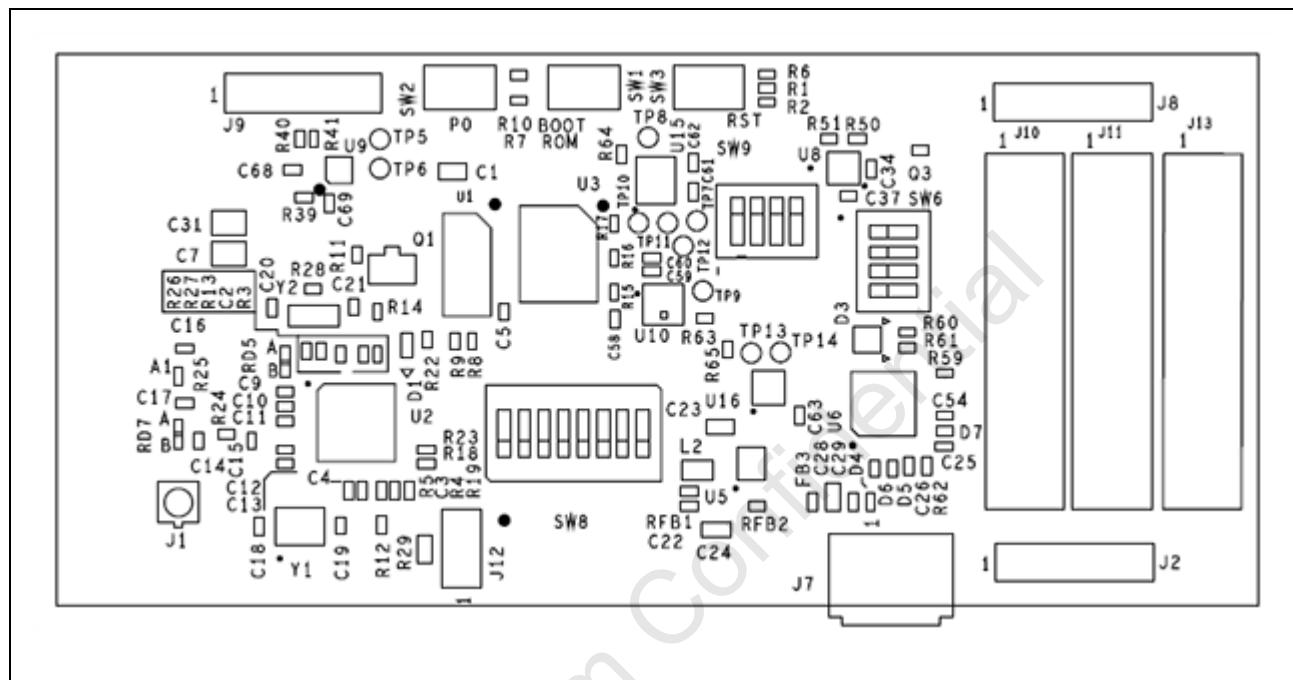
Figure 1: WICED Smart Tag4 Key Components



Board Layout

The Smart Tag evaluation board assembly top view is shown in [Figure 2](#). The resistors for memory selection are highlighted in red.

Figure 2: Board Assembly (Top View)



By default, the board is set to use the internal LPO for sleep, but it can be set to use external LPO by installing R102 and R103, highlighted in [Figure 2](#), above. Resistor values are listed in [Table 1](#), below.

Table 1: Resistor Settings for External 32 KHz Crystal

Resistor	<i>Internal LPO</i>	<i>External LPO</i>
R26	DNI	0 Ohm
R27	DNI	0 Ohm

By default, the board is set to use EEPROM but can be set for serial flash by adjusting the resistors highlighted in [Figure 2](#) to the desired setting (shown in [Table 2](#)).

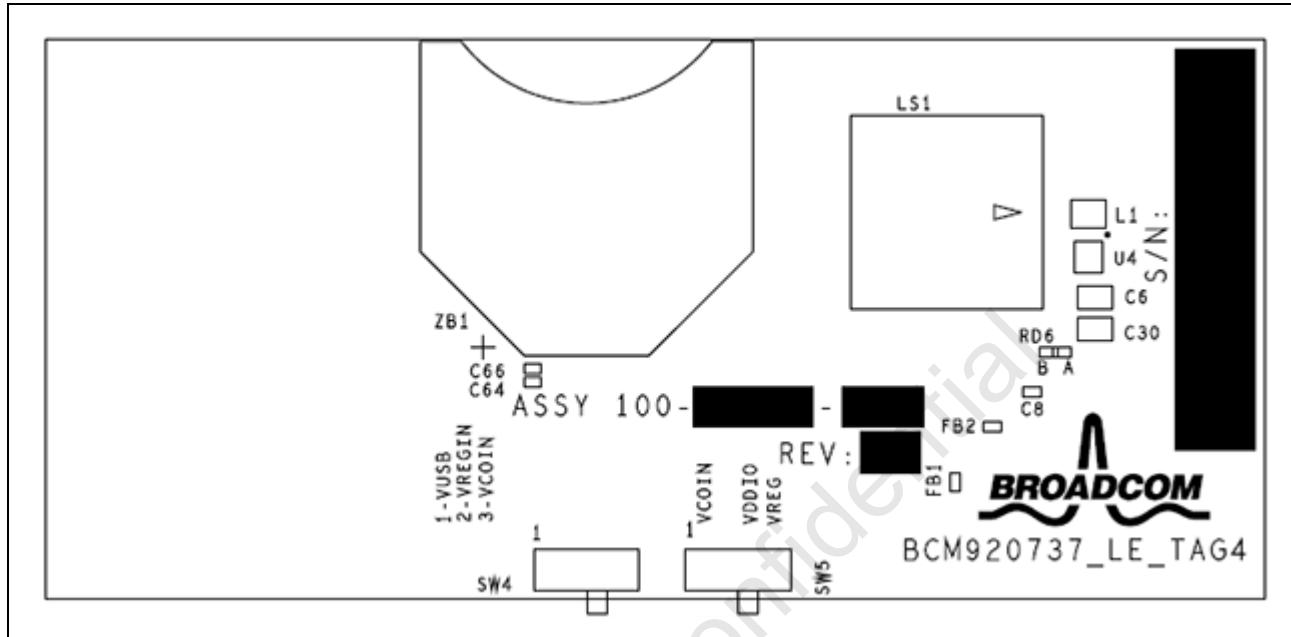
Table 2: SW8 DIP Settings (Memory Type)

Memory Type	ON	OFF
EEPROM	1, 3, and 5	2, 4, 6, 7, and 8
SFLASH ^a	2, 4, 6, 7, and 8	1, 3, and 5

- a. For the SFLASH to be active R39 must be removed to disable the I²C bus. This is in addition to the switch settings.

The Smart Tag evaluation board assembly bottom view is shown in [Figure 3](#).

Figure 3: Board Assembly (Bottom View)



Power-Up Options

VDDIO can be sourced from three options:

- Coin cell unregulated
- Coin cell regulated
- USB regulated

These options are set using **SW2** and **SW3** (see [Figure 2 on page 9](#)), as listed in [Table 3](#). The default regulator output is 1.8V.

Table 3: Switch Settings for Power

Switch	Coin Cell Unregulated	Coin Cell Regulated	USB Regulated
SW4	VUSB	VCOIN	VUSB
SW5	VCOIN	VREG	VREG

To adjust the regulator output, feedback components can be adjusted as shown in [Table 4](#).

Table 4: Voltage Regulator Output

VOUT	Component Values
3.3V	RFB1 = 470 kΩ, RFB2 = 150 kΩ, C22 = 100 pF
3.0V	RFB1 = 330 kΩ, RFB2 = 120 kΩ, C22 = 150 pF
1.8V	RFB1 = 300 kΩ, RFB2 = 240 kΩ, C22 = 150 pF
2.0V	RFB1 = 360 kΩ, RFB2 = 240 kΩ, C22 = 150 pF

UART Boot-Up

The following procedure describes how to power up the tag board with the UART interface enabled.

1. **SW4** and **SW5** should be placed in the desired power configuration, as shown in [Table 3](#).
2. **SW6** should be in HCI mode by placing DIP switches **2** and **4** in the **ON** position (these positions are considered standard until you wish to enter app mode).
3. Plug in the USB cable to connector **J7**. The Smart Tag will display in the Windows Device Manager as *two* COM ports named **Silicon Labs Dual CP210x USB to UART Bridge: Enhanced COM Port (COM##)**, where **##** is the number of the assigned com port.



Note: If the device driver does not load correctly, the FTS2232H driver must be downloaded from the FTDI website (see <http://www.ftdichip.com/Drivers/VCP.htm>).

The evaluation board can now accept HCI commands or download firmware through the UART interface.

Boot from ROM

The following procedure describes how to boot the Smart Tag board from ROM. This is available if the NVRAM is corrupted and the device is unable to boot correctly.

1. **SW4** should be in the **VUSB** position and **SW5** should be in the **VREG** position.
2. **SW6** should be in HCI mode by placing DIP switches **2 and 4** in the **ON** position.
3. Press and hold the BOOT ROM button (**SW1**) and power up the device by plugging in the USB cable to connector **J7**. The BOOT ROM button (**SW1**) can be released after the device is identified in the Windows Device Manager.
or
Press and hold the BOOT ROM button (**SW1**), press and release RESET (**SW3**), release the BOOT ROM button (**SW1**).

The evaluation board can now accept HCI commands or download firmware through the UART interface.

Application Firmware Software Boot-Up

The procedure below describes how to power up the Smart Tag board to run application firmware.

1. **SW4** should be in the **VUSB** position and **SW5** should be in the **VREG** position.
2. Set **SW8** DIP switches **1, 3, and 5** to the **ON** position (EEPROM). **All other** SW8 DIPs should be in the **OFF** position.
3. Set **SW6** DIP switches **2 and 4** to the **ON** position and switches **1 and 3 OFF** position.

The Smart Tag is now ready to be run the application firmware stored in EEPROM or serial flash, depending on the jumper configuration.

Hardware Settings

Configurable Resistor Descriptions

Hardware configuration for the Smart Tag board is defined in [Table 5](#).

Table 5: Configurable Resistor Descriptions

Component	Configuration	Description	Comments
RD5	A-C	External LDO DC/DC Converter	RD5 and RD6 must both be in either A-C or B-C, no mismatch
	B-C	Internal DC/DC converter	
RD6	A-C	External LDO DC/DC converter	
	B-C	Internal DC/DC converter	
RD7	A-C	PCB monopole antenna	–
	B-C	External antenna connector (J1)	
R26	Short	External crystal (0.03277 MHz)	R26 and R27 must both be in either open or closed, no mismatch
	Open	Internal crystal (24.000 MHz)	
R27	Short	External crystal (0.03277 MHz)	–
	Open	Internal crystal (24.000 MHz)	
R29	Short	Power analyzer terminal bypassed	–
	Open	Initiate power analyzing terminal (J12)	
R39	Short	I ² C expander disconnect/SFLASH enabled	–
	Open	I ² C expander active/SFLASH disabled	
FB3	Short	USB-to-UART (FTDI) active	–
	Open	FTDI disconnect	

Connector/Switch Descriptions

Connector/switch descriptions are defined in [Table 6](#).

Table 6: Connector/Switch Descriptions

Component	Description
SW1	EEPROM/SF bypass button (BOOT ROM)
SW2	GPIO0 button
SW3	Hardware reset button
SW4	Regulator input from coin cell/USB switch
SW5	VDDIO from coin cell/regulator output switch
SW6	HCI mode/application mode/JLINK mode switch
SW8	EEPROM/SF setting
SW9	Individual sensor switches
J1	External antenna connector
J2	JLINK debug
J7	USB connector
J8	UART header
J9	I ² C header
J10	GPIO headers
J12	Power analyzing terminal

Schematics

Figure 4: Baseband and PMU Schematics

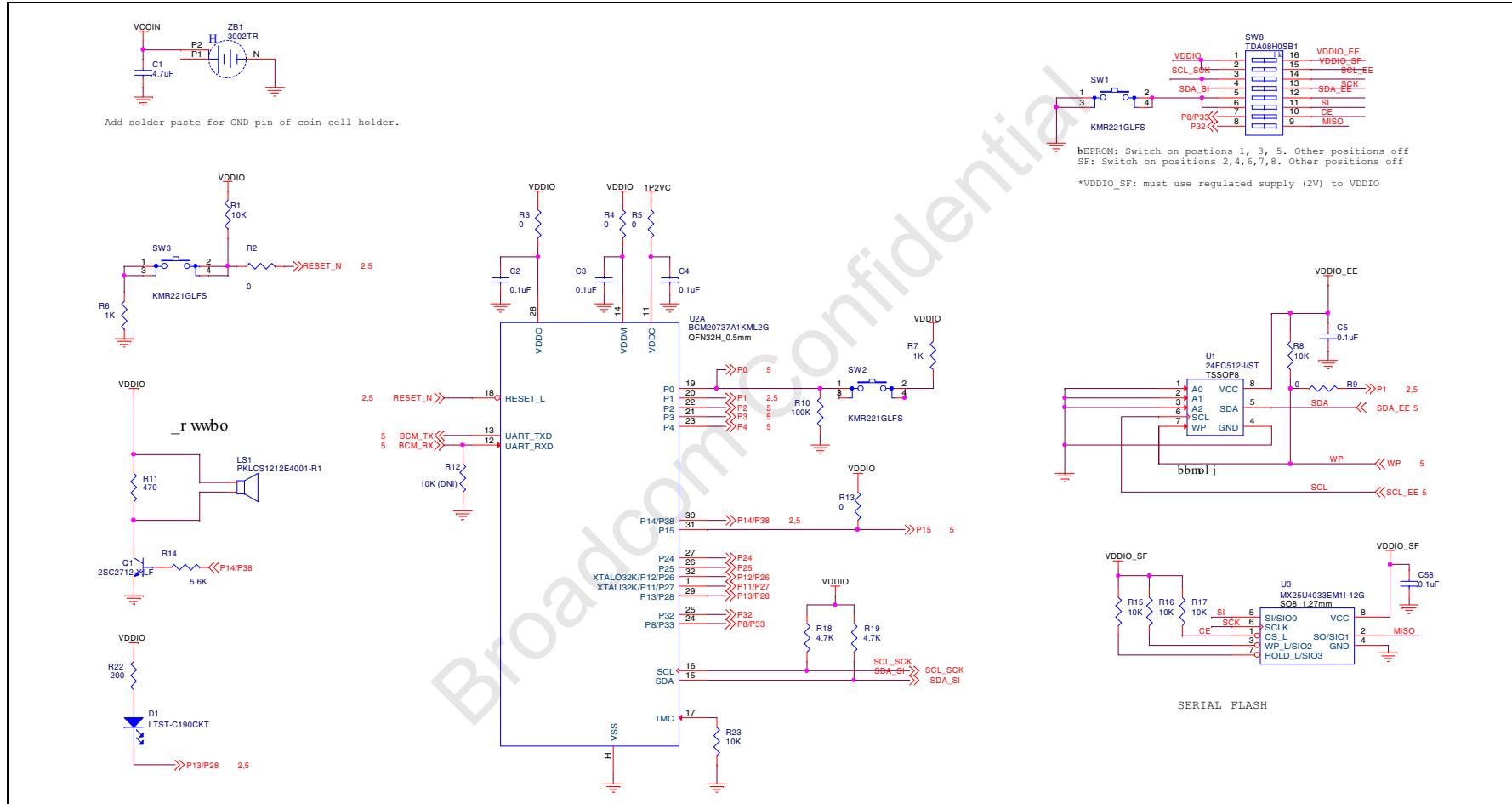


Figure 5: RF Schematics

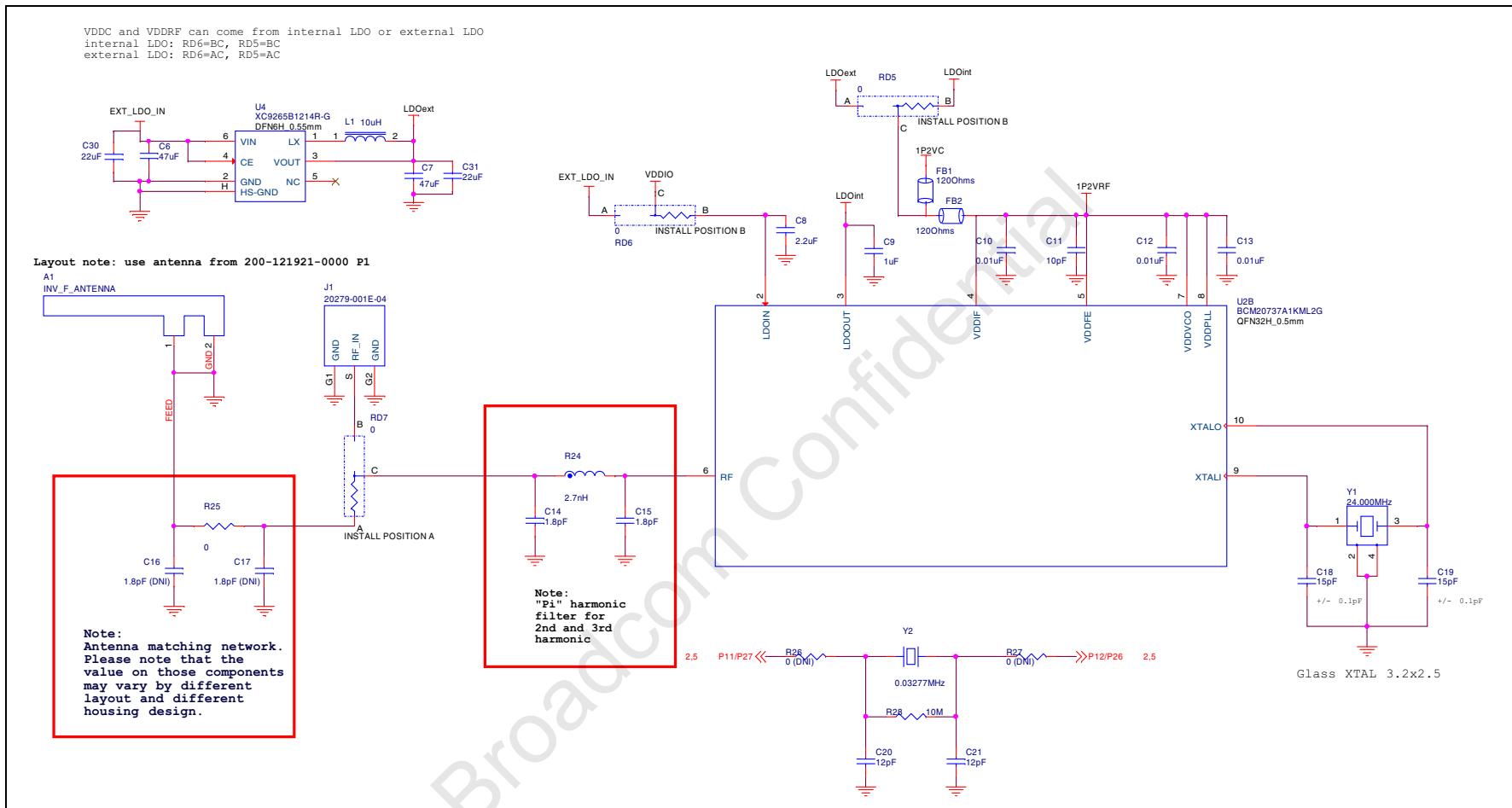


Figure 6: GPIO, Headers, and Power Schematics

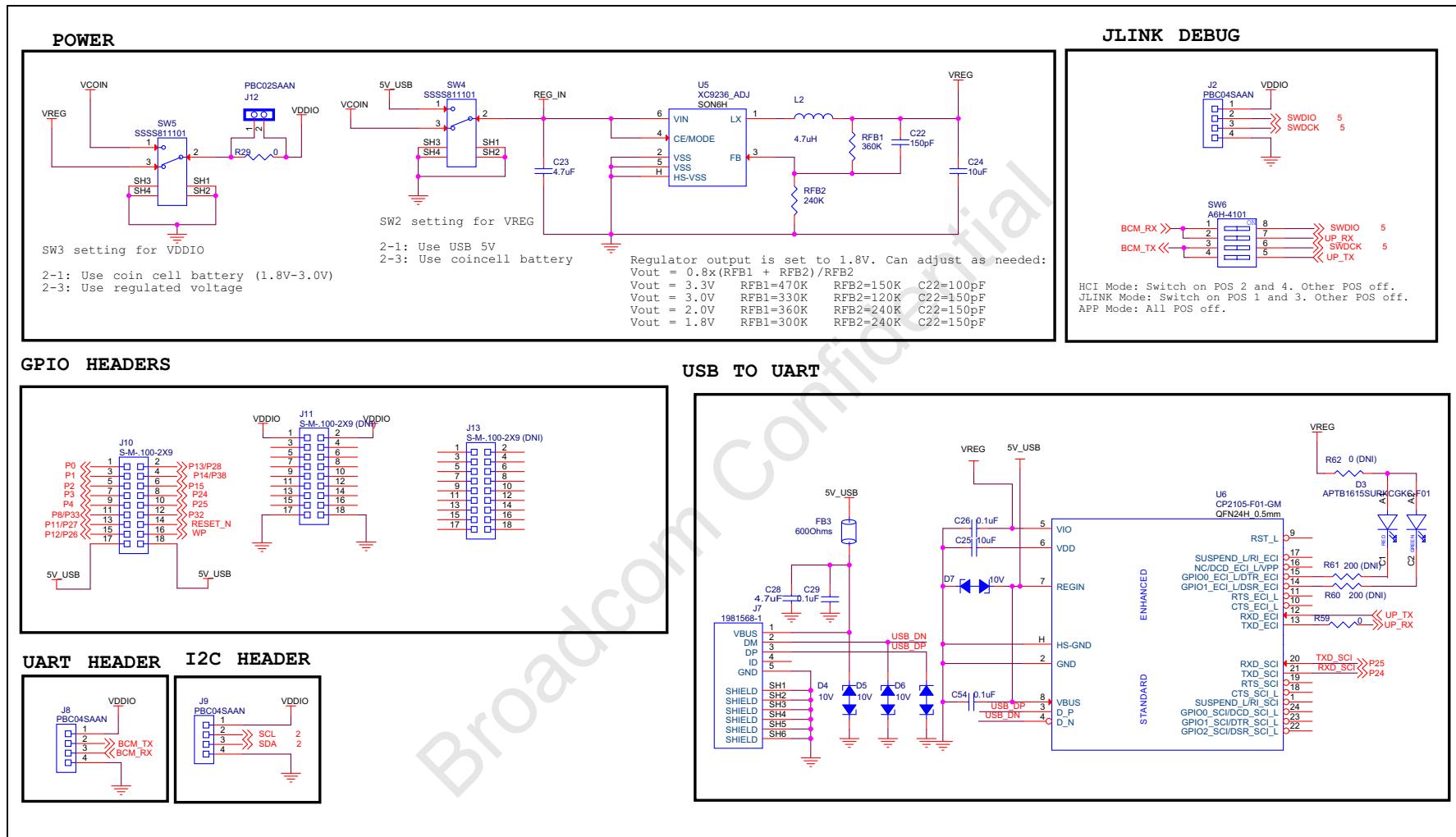
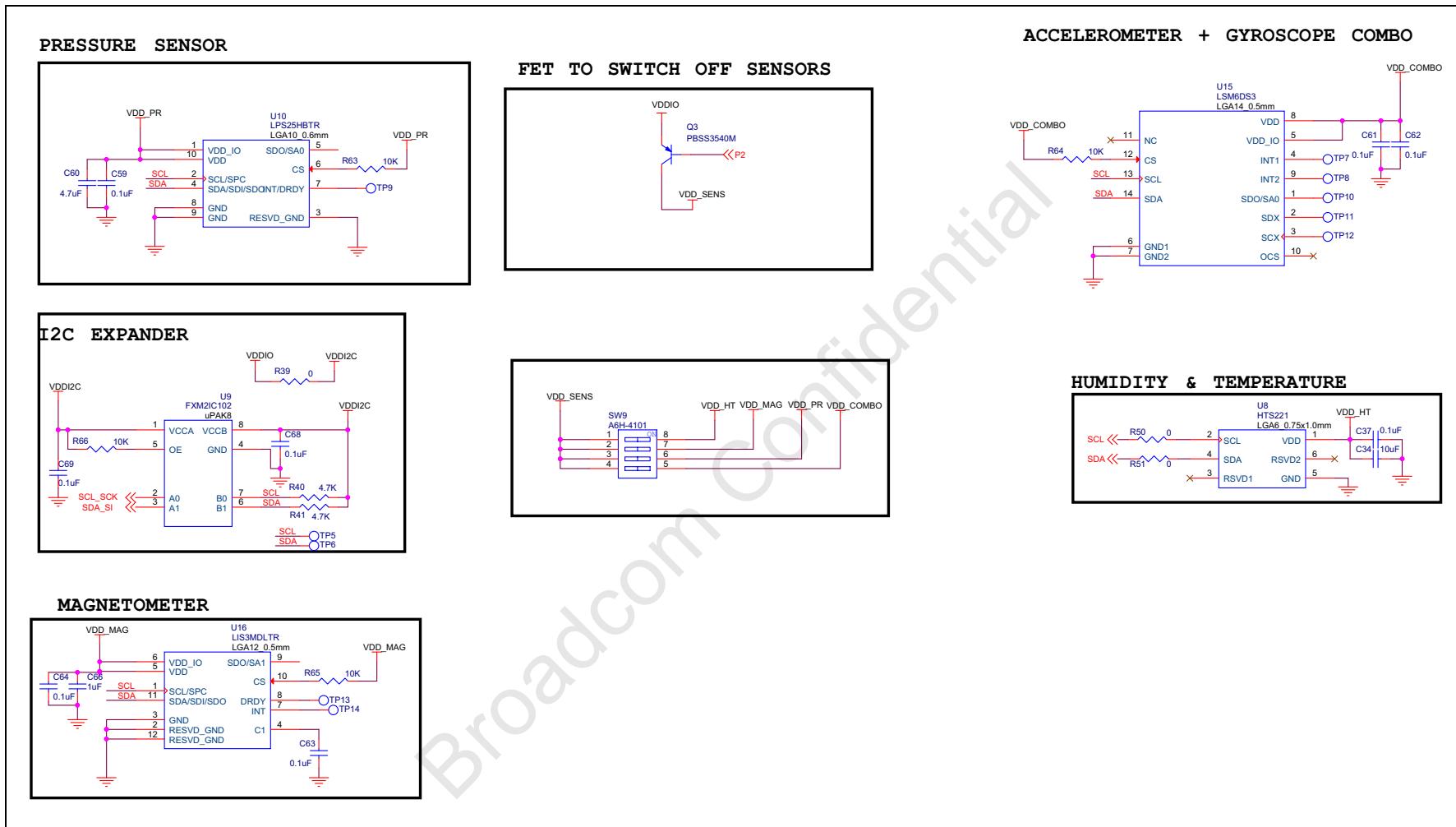


Figure 7: Switches and Sensors





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