Taylor & Francis
Taylor & Francis Group

International Journal of Electronics

ISSN: (Print) (Online) Journal homepage: https://www.tandfonline.com/loi/tetn20

A low-cost test strategy based on transient response method for embedded reconfigurable filters

Emanuel A. Dri , Gabriela M. Peretti & Eduardo A. Romero

To cite this article: Emanuel A. Dri , Gabriela M. Peretti & Eduardo A. Romero (2020): A low-cost test strategy based on transient response method for embedded reconfigurable filters, International Journal of Electronics, DOI: 10.1080/00207217.2020.1793412

To link to this article: https://doi.org/10.1080/00207217.2020.1793412

Publisher: Taylor & Francis & Informa UK Limited, trading as Taylor & Francis Group

Journal: *International Journal of Electronics*

DOI: 10.1080/00207217.2020.1793412

A low-cost test strategy based on transient response method for embedded reconfigurable filters

Emanuel A. Dri[a], Gabriela M. Peretti[a,b*] and Eduardo A. Romero[a,b]

[a*]*Grupo de Estudio en Calidad en Mecatrónica, Universidad Tecnológica Nacional – Facultad Regional Villa María, Villa María – Córdoba, Argentina;*

[b]*Grupo de Desarrollo Electrónico e Instrumental, Universidad Nacional de Córdoba – Facultad de Matemática, Astronomía y Física, Córdoba City – Córdoba, Argentina*

* Corresponding author: Gabriela Peretti

- Address: Av. Universidad 450, Villa María – Córdoba – Argentina
- Post code: X5900HLR
- e-mail: gperetti@frvm.utn.edu.ar

Disclosure statement: No potential conflict of interest was reported by the authors

Funding: This work was supported by Universidad Tecnológica Nacional under grant number UTI3812TC

Word Count: 5403

A low-cost test strategy based on transient response method for embedded reconfigurable filters

Abstract: This work introduces a low-cost test strategy for second-order lowpass filters implemented in analog reconfigurable circuits of PSoC1 devices. By adopting a functional approach, the specifications of the filters are determined through the analysis of their transient response features. The strategy relies on the device dynamic reconfiguration ability to minimize test hardware overhead. Additionally, it is capable of testing filters configured in all the programmable resources of the device. Test stimuli are produced in a signal generator implemented inside the chip. A test script running on a computer connected to an oscilloscope (or data acquisition board), processes the response of the filters and calculates their functional features. Experimental results in several chips show excellent stability and low errors against nominal values, proving the viability of the strategy. The proposal is compatible with field maintenance due to its low instrumental overhead. Additionally, it can be used as a low-cost production test, for debugging circuits during the development process, or as end-of-line testing.

Keywords: Analog and mixed-signal reconfigurable circuit, transient response analysis method, embedded mixed-signal circuit testing, functional test, analog filter test

1. Introduction

Configurable mixed-signal microcontrollers (μC) can offer low-cost and practical solutions for a wide range of applications. Their analog configurable circuits (ACCs) increase the flexibility and allows the user to implement analog processing functions on the same chip. This contributes to miniaturization, reduces costs, increases reliability, and improves time to market. Mixed-signal μC can also operate as analog coprocessors, achieving considerable reductions of the required digital resources (Twigg & Hasler, 2009), (Schlottmann et al., 2012).

However, the users must deal with the testing of systems implemented with these μCs either during the production phase (for quality assurance) or in-field for determining circuit degradations (Golonek & Machniewski, 2018). The testing problem scales when it is necessary to address the circuits embedded in the ACCs, becoming challenging due to multiple factors. The lack of detailed information about the actual implementation of the internal circuits, the reduced controllability and observability (due to difficult access to these sections), the complexity of the signals to be treated, and adverse noise conditions are only some of them.

The test of ACCs also presents the same problems found in their fixed-function counterparts: the lack of an adequate fault model and the difficulty to discriminate between fault-free and faulty circuits, due to the complex relationship between input and output signals (Ting & Chen, 2018), (Hatzopoulos, 2017). This limits the availability of systematic procedures for mixed-signal testing (Gomez-Pau et al., 2015; Vock et al., 2012). In this sense, it is accepted that solutions can only be given for specific circuits or at most for circuit classes (Bushnell & Agrawal, 2002; Gomez-Pau et al., 2015). The application of a given methodology to a circuit usually requires the formulation of a specific scheme, the demonstration of its feasibility and efficiency.

Because analog filtering is widely used (Ting & Chen, 2018), numerous devices offer this function, that can be implemented using different techniques. Passive filters exhibit low noise, high linearity, and lack of power dissipation, but require hard to integrate inductors. Active-RC and Gm-C implementations overcome this drawback, allowing the implementation of relatively high-frequency filters. On the other hand, Switched-Capacitor (SC) technique allows obtaining filters that are more stable but require operation below their sampling frequencies, limiting the possibility of accomplishing high-frequency characteristics. Also, SC filters have disadvantages related to non-idealities in switches and operational amplifiers (Ananda Mohan, 2012).

The formulation of test strategies for filters, when are configured in ACCs embedded in μCs is relevant, especially those able to be implemented by the final user. In this way, it will be possible to check the specifications of the filters either during the fabrication of products based on these circuits or for detecting malfunctioning in-field.

1.1Previous work

Although the analog and mixed-signal circuits testing is a very active research field, a relatively small number of papers focus on the test of ACCs. The initial impulse in this field has been given by the work of (Balen et al., 2006), contemporary with the advent of commercial FPAAs. Afterwards, the advances in the technologies of ACCs have not been accompanied by the formulation of suitable test strategies. During almost the last two decades both, scientific and industrial communities proposed and produced different ACCs, some of them embedded in complex platforms (Hasler, 2019; Schlottmann et al., 2012; Suda et al., 2016). However, the relevant test proposals suitable to be implemented by the final user of the configurable devices (not by the vendor) are few (Andrade et al., 2005; Balen et al., 2007; Laprovitta et al., 2014; Lovay et al., 2015).

The present paper proposes the use of the Transient Analysis Method (TRAM) for testing SC lowpass filters embedded in the analog sections of the Cypress Psoc1 processor. TRAM is a specific test technique for second-order filters or a cascade of them (Calvano et al., 1999) that has been proved to be useful only for a few configurable devices.

Balen et al. (2006,2007) have made use of TRAM to test the ACCs of Field Programmable Analog Array (FPAAs). They address two commercial FPAAs (Anadigm© and Lattice©), targeting the detection of faults in their structures, without obtaining the parameters of the transfer function of the filters under test. Additionally, they do not consider the statistical variations of the test parameters, that can seriously compromise the fault detection ability of the proposed scheme.

Lovay et al. (2015) employed TRAM for getting the specifications of second-order filters in an FPAA from Lattice® in the context of an evolutionary hardware strategy. The authors resort to a simulation model of the filter under test, without considering experimental measurements nor statistical variations, presenting the same problems of the previously referenced paper.

Golonek & Machniewski (2018) employ a transient analysis similar to TRAM, but that it is not proved in filters configured in ACCs. They formulate a mathematical model before the test implementation for making a quick verification of the circuit specifications.

1.2 Paper contributions

This paper presents a novel scheme for applying TRAM to second-order lowpass filters embedded in the ACCs of the PSOC1 processor. The solution is comprehensive, i.e., all the possible filters in the analog array can be tested. The proposal employs in a new way, concepts of TRAM, software-based test, and signal processing techniques. The later allows overcoming the well-known noise problems related to the analog sections of this processor. Also, the scheme takes advantage of the processor on-fly reconfigurability characteristics for reaching zero circuit overhead for testing. The use of internal resources for generating test signals reduces the requirement of external test equipment. The remaining of the test equipment is affordable by small companies and even for technicians. Our characterization campaign is entirely experimental, including on-chip and inter-chip variations, more exhaustive than previously reported research in the area. The results establish a reasonable basis of confidence in the test scheme, allowing the test engineers in the industry to adopt it in a very straightforward way.

2. System Description

2.1 PSoC1 Architecture

Fig. 1 depicts the top-level view of the PSoC 1 architecture. The device has resources usual of μCs, like an 8 bits CPU, Flash and SRAM memories, and communications interfaces, among others. Additionally, PSoC1 also offers analog and digital configurable blocks and user-configurable interconnection routes that make this platform highly flexible. The ACCs of the device are of two types: continuous-time (CT) and SC blocks, organized in columns (Cypress Semiconductor, 2017b). Analog blocks can implement programmable gain amplifiers (PGAs), programmable filters, comparators, analog to digital converters (ADCs) and digital to analog converters (DACs) among other functionalities.

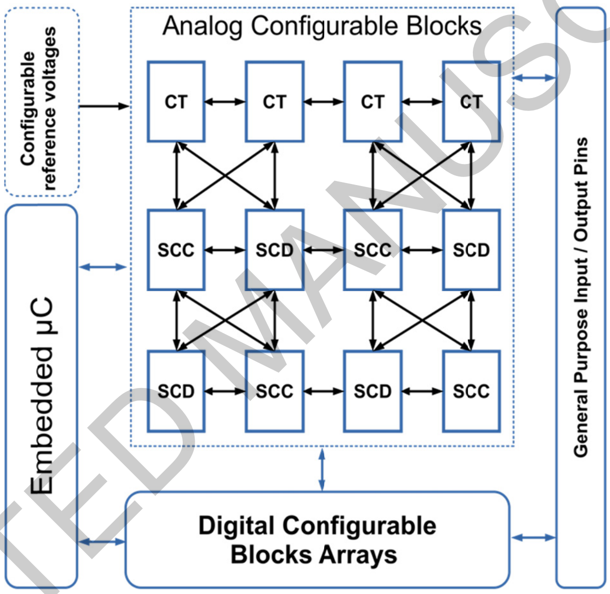

Figure 1. PSoC1 architectural description

2.2 Filters under test

A schematic diagram of the filter under test is shown in Fig. 2. This filter is configured by the proper interconnection of two configurable cells, one of type SCC and the other one of type SCD (Fig. 1). In Fig. 2, φ1 and φ2 are the two non-overlapping clock-phases of frequency fs (sample frequency). The values of the capacitors are obtained by programming capacitors arrays that have a base-capacity of 80fF. C1 to C4 can adopt a value ranging from 0 to 31 times the base-capacity, while CA and CB can adopt 16 or 32 times this value.

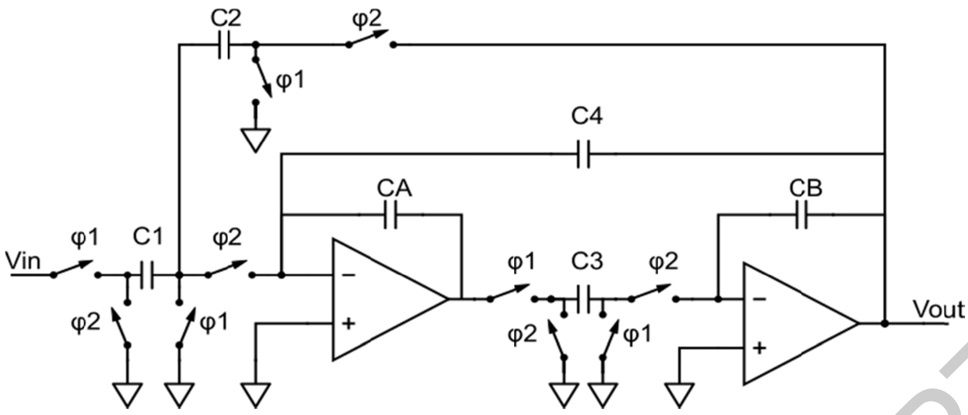

Figure 2. Schematic diagram of the filter under test

The ACCs of PSoC1 allows configuring the filter of Fig. 2 in different locations of the analog array. From the test point of view, the filter position is relevant because it restricts the connectivity with other blocks, complicating the formulation of the test scheme.

In a four-column device like the one adopted here, the location of the filter can be horizontal or vertical. Additionally, some filters can be configured as type A or B according to the resources used for implementing the structure shown in Fig. 2. In the following, we assign to the filters a name with the structure "FNOT", where F denotes the word filter, N is the number, O is the orientation (Horizontal or Vertical), and T is the filter type (A, B, A|B means that could be A or B). For instance, F1HA|B denotes the filter number 1, in the horizontal position, which can be type A or B. Table 1 summarizes all the filters that can be configured in a four-column PSoC1 device (implementing the structure of Fig. 2).

Table 1. Resources of the filters that can be configured in PSoC1

Filter	Input SC block	Output SC block
F0HA|B	ASC10	ASD11
F1HA|B	ASC21	ASD20
F2HA|B	ASC12	ASD13
F3HA|B	ASC23	ASD22
F0VA	ASC10	ASD20
F1VA|B	ASC21	ASD11
F2VA	ASC12	ASD22
F3VA|B	ASC23	ASD13

The transfer function of the filter in the discrete-time domain (Cypress Semiconductor, 2018) is:

$$H(z)=\frac{zC_1C_3}{z^2C_BC_A\text{-}2zC_BC_A+zC_2C_3+zC_4C_3\text{-}C_4C_3+C_BC_A} \quad (1)$$

The application of the bilinear transform to (1) leads to a continuous-time domain equivalent (2). The comparison of (2) with the general lowpass filter expression (3) allows determining the main filter specifications as a function of the capacitor values, as long as fs has a high value (Cypress Semiconductor, 2018). In (3), the specifications are the bandpass gain (K), pole frequency (ωp), and quality factor (Qp). Other features, like the bandpass ripple (Mr) and the -3dB cutoff frequency (Fc) can be obtained from (3) by simulation.

$$H(s)=\frac{-\frac{C1}{C2}\cdot\frac{\left(1-\left(\frac{s}{2fs}\right)^2\right)fs^2}{\frac{C_AC_B}{C_2C_3}-\frac{1}{4}-\frac{1}{2}\frac{C_4}{C_2}}}{s^2+\frac{C_4}{C_2}\cdot\frac{sfs}{\frac{C_AC_B}{C_2C_3}-\frac{1}{4}-\frac{1}{2}\frac{C_4}{C_2}}+\frac{fs^2}{\frac{C_AC_B}{C_2C_3}-\frac{1}{4}-\frac{1}{2}\frac{C_4}{C_2}}} \quad 2)$$

$$H(s)=\frac{K.{\omega_p}^2}{s^2+\frac{\omega_p}{Q_p}s+{\omega_p}^2} \quad 3)$$

3. Test proposal

3.1 General considerations on TRAM

TRAM requires a proper excitation of the filter under test to produce an underdamped response. For this purpose, a step, ramp, or parabola is used, depending on the type of the filter (lowpass, bandpass, or highpass, respectively). Then, parameters of the transient response are measured, usually the peak time (Tp) and the overshoot (OS). It is assumed that a fault in the filter will deviate the transient response parameters out of their fault-free tolerances, and the faulty behavior will be observed.

Fig. 3 illustrates a typical underdamped response, pointing out the main test attributes, Tp, and OS. The figure also shows the voltages Vpeak (peak value), Vfinal (steady-state), and Vini (initial value), which will be used for determining OS and K, later in this work.

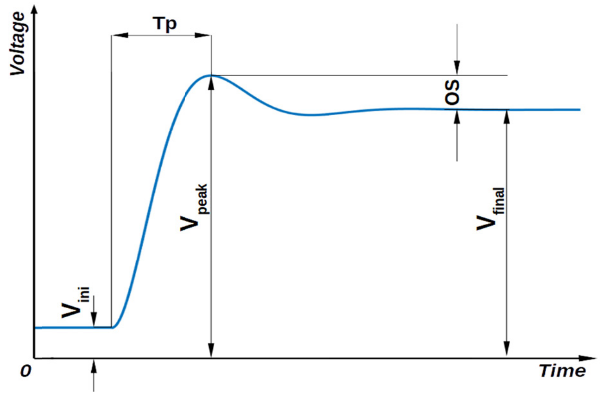

Figure 3. Second-order filter step response, and test parameters Tp, OS, Vini, Vfinal, and Vpeak.

TRAM is considered as a functional test because it is possible to determine ωp, Qp, and K from the transient response parameters using expressions (4) to (6) (Ogata, 2010). In (4), Vstep is the amplitude of the input step (stimulus used when the filter is low pass).

$$K = \frac{V_{final} - V_{ini}}{V_{step}} \tag{4}$$

$$Q_p = \frac{1}{2}\sqrt{\left(\frac{\pi}{\ln(OS)}\right)^2 + 1} \tag{5}$$

$$\omega_p = \frac{\pi}{Tp\sqrt{1 - \frac{1}{4.Q_p{}^2}}} \tag{6}$$

3.2 General Test Scheme

Fig. 4 shows a general scheme of the test proposal. We use the internal resources of PSoC1 for the test stimuli generation. An oscilloscope captures the CUTs responses, and a laptop computer connected to it via a VISA interface, collects and processes the test data.

The scheme uses the configurable internal connection network for delivering the test signals to the filters under test and bringing their responses to a pin. However, due to constraints in the device connectivity, some cases require additional blocks to perform this task.

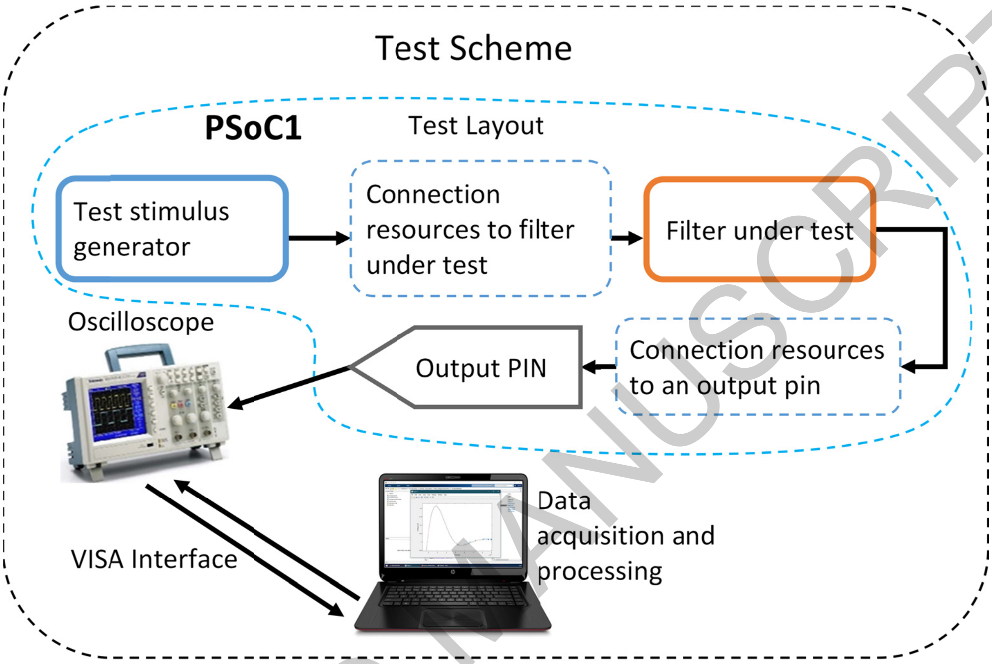

Figure 4. General test scheme

The test strategy relies on the device dynamic reconfiguration ability, which allows time multiplexing of the resources inside PSoC1 (Cypress Semiconductor, 2017a) while avoids including extra hardware for the test. Dynamic reconfiguration requires the definition of different hardware configurations (layouts), one of them holding the test configuration. Usually, user applications run in one or more layers. In test mode, the corresponding layout maintains the filter under test in its position and includes the resources for the test (test stimulus generator and connection blocks, Fig. 4). An application programming interface (API) in the firmware switches between normal and test layouts.

As an example, Fig. 5 illustrates a hardware configuration applied to test the filter F1HA. The user layout has the normal-mode hardware configuration. Here, it has an amplifier and conditioning system for an external signal, which uses an instrumentation amplifier (Ins Amp) and the F1HA filter. The analog signal is converted to digital with ΣΔADC and then is transmitted by the UART. The test layout unplaces all blocks except F1HA and adds the test mode resources, in this case, the stimulus generator PGA0 and an auxiliary amplifier (Amp Aux1).

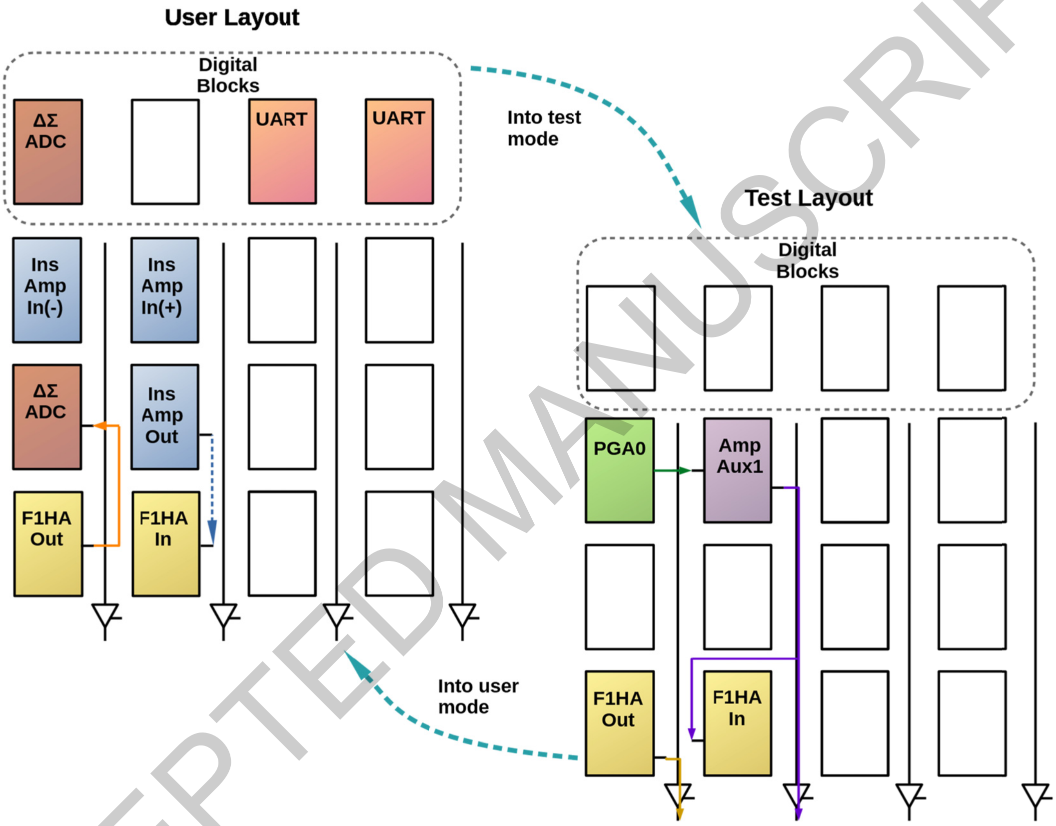

Figure 5. Normal to test mode switching example

3.3 Test stimulus generation

A PGA placed on a CT block (Fig. 6) generates the test stimulus. For doing this task, a software routine writes a register (Reference selection) associated with the PGA for switching its input between a reference voltage RefLo (1.2V for a 5V supply), and AGND (nominally 2.5V). This action produces a step signal that can be amplified or attenuated by the PGA, according to the configuration of the programmable resistor network formed by Ra and Rb. Unity gain is also possible, as shown in the figure. It should be noted that only PGAs in the analog columns 0 and 3 can be used as test stimuli generators due to constraints in the connectivity resources.

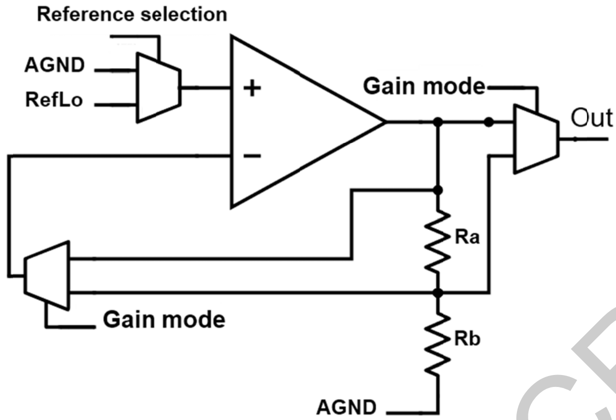

Figure 6. Simplified scheme of a PGA configured as a step signal generator

3.4 Resources used by the test

The location of a given filter in the analog array conditions the resources required for its test. Our proposal to overcome connectivity restrictions is shown schematically in Fig. 7 for horizontal filters and in Fig. 8 for vertical filters. Although this test scheme is not unique, it has been chosen after a characterization campaign of different alternatives. The proposal here is the one that offers the best performance.

In the figures, dash line boxes represent the filters, and the arrows represent signal paths. Buf0 to Buf3 are buffers that connect analog blocks to output pins. PGA0 and PGA3 are blocks that generate step stimuli (Fig. 6). AmpAux1 and AmpAux2 are auxiliary unity-gain PGAs, and AmpSC is an amplifier configured in an SC block.

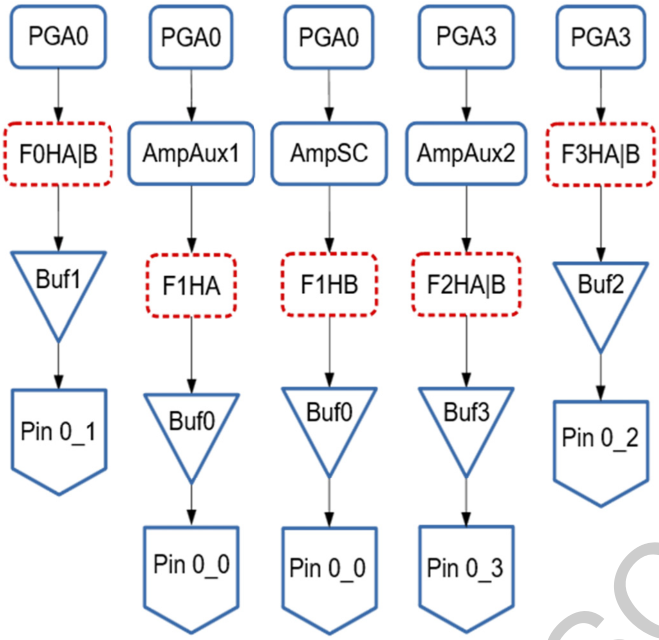

Figure 7. Resources used to test horizontal filters.

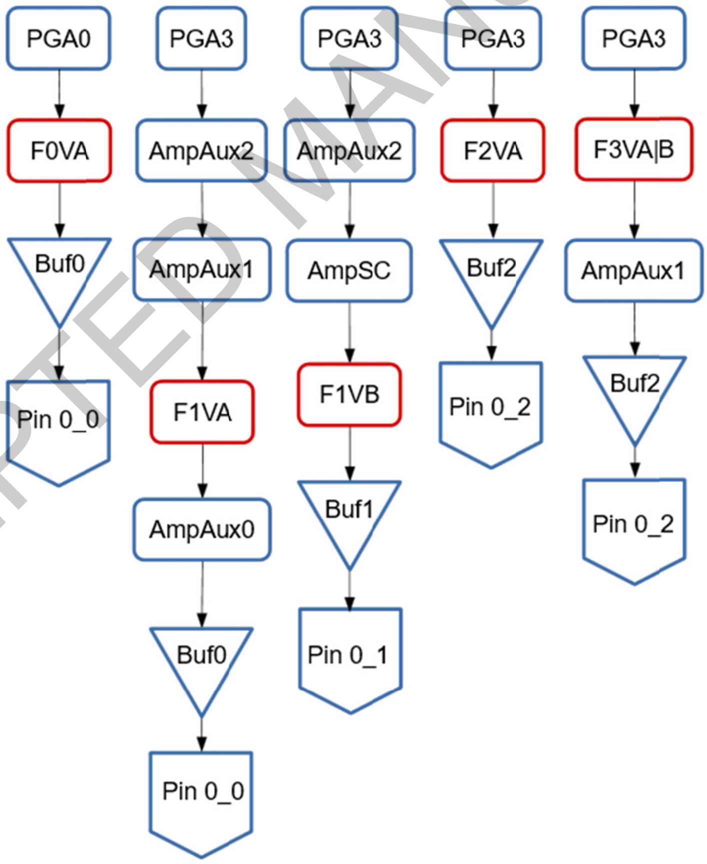

Figure 8. Resources used to test vertical filters

For example, Fig. 9 relates the information of Fig. 7 with the location and resources needed in the analog array. In particular, it is shown the proposal to excite and to observe the output of the FIHA and F3HA|B filters. For F1HA, the stimulus generation is configured in PGA0. The output of PGA0 is conducted to an auxiliary PGA embedded in the second column (AmpAux1), whose output is connected to F1HA. The output of F1HA is connected to a pin using Buf0. Alternatively, the F3HA|B test uses PGA3 as the stimulus generator and Buf2 as a connection to an output pin.

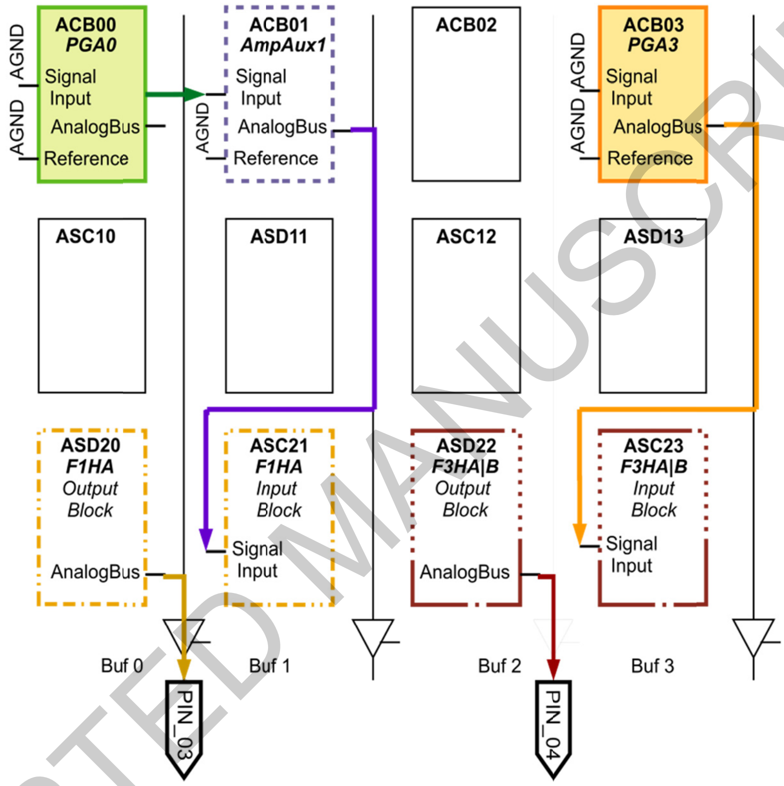

Figure 9. Connection scheme for testing horizontal filters in row 2

3.5 Response processing

The responses generated by the filters under test present a significant amount of noise and a DC level that considerably varies from chip to chip and with the environmental conditions. For the sake of illustration, Fig. 10 shows an experimental measure of the F1VB filter, where it is observed the test stimulus, which consists of a negative step and the filter response.

The proper determination of the test parameters requires to perform signal processing. This process is first performed by the oscilloscope, which averages 128 samples of the filter test response for reducing the noise. However, the signal is sampled in amplitude and time and presents residual noise. These characteristics complicate getting accurate parameters for the test.

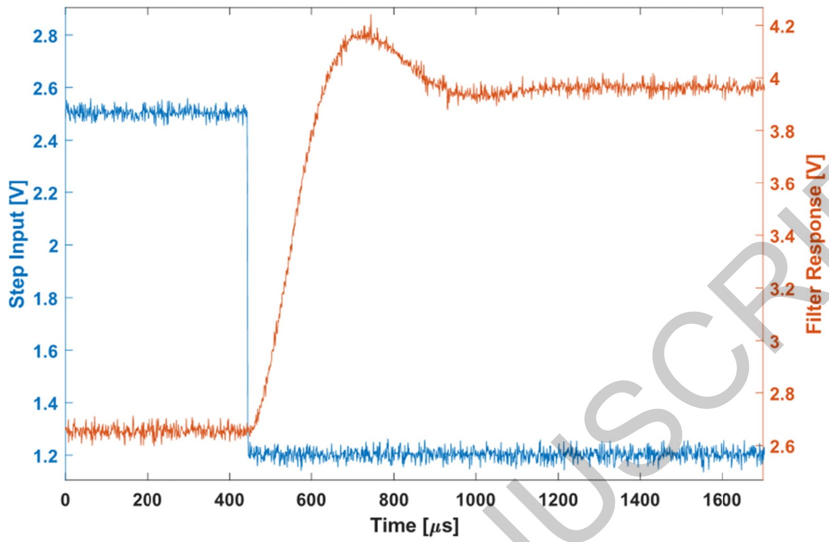

Figure 10. Experimental measurement of filter FIVB without averaging

To overcome this inconvenience, we smooth the waveforms and use the resulting curves to determine the parameters K, OS% (the overshoot percentage), and Tp. For this purpose, we employ the MatLab © Curve Fitting application for obtaining smooth spline adjustment curves. To illustrate this process, Fig. 11 shows the superimposition of a filter response as captured by the oscilloscope in average mode and its smoothed curve. The amplification of the boxed portion of the signal shows that, if the maximum of the unprocessed signal is used to obtain the peak time, an erroneous value would be obtained. Taking the maximum of the adjusted curve overcomes this problem.

Additionally, we use the MatLab© DSP System Toolbox tool to find the peak time values as well as the voltages needed to calculate OS% by using (7).

$$OS\% = \frac{V_{peak} - V_{final}}{V_{final} - V_{ini}} \times 100\% \quad (7)$$

In (7), Vpeak is the overshoot voltage, which is computed as the maximum of the adjusted curve. Vini and Vfinal are the initial and final voltages of the responses of the filters (Fig. 3).

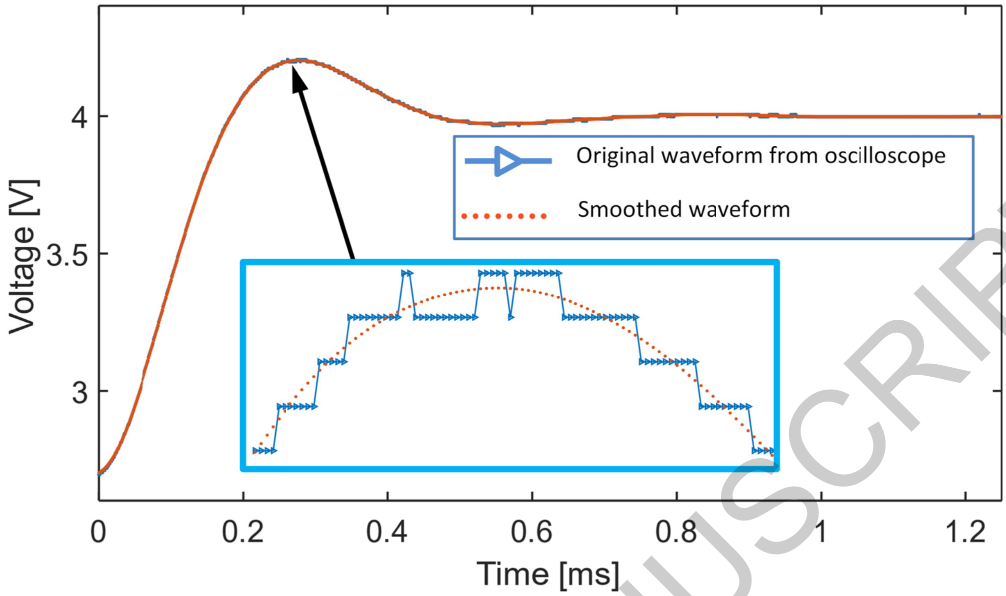

Figure 11. Waveform obtained from the oscilloscope (average mode) and its smoothed curve

The use of expressions (4) to (6) allows establishing ωp and Qp from each set of values of Tp, OS%, and K. Then, the filter transfer function is reconstructed to determine by simulation in Matlab the other two parameters of interest, Fc and Mr. Then, it is possible to verify if the filter specifications are within the tolerance established by the final user.

4. Experimental results

The effectiveness of the test proposal was evaluated through a characterization campaign by adopting an entirely experimental approach. For this purpose, a lowpass filter with the specifications depicted in Table 2 was selected as a case study. The specifications were obtained by simulating in MatLab the discrete-time domain transfer function (1), using the capacitor values given by the IDE at the design stage.

The laboratory experiments involved the application of the test procedure described in Section 3. A filter from Table 1 was embedded in the CY8C-29466-PXI PSoC1 device. The test procedure was repeated 100 times for establishing the repeatability of the measurements. All the filters of Table 1 were tested to establish the variability regarding the location of the filters. Then, the experiment was repeated in seven chips more to explore how the inter-chip variations affect the test outcome.

Table 2. Specifications of the filter under test

Feature	Value
Edge frequency (0 dB cross) (Hz)	1990.0
-3dB frequency (Hz)	2552.5
Bandpass ripple (V/V)	1.14
DC Gain (V/V)	1.0
ω_p (rad/s)	12685
Qp	0.98
Sampling frequency [KHz]	200

4.1 TRAM performance

Tables 3 to 6 show statistics obtained for the three basic specifications K, ωp, and Qp, and for the derived ones, Fc and Mr. The tables show the mean, the range (maximum and minimum) and the standard deviation (as a percentage of the mean) of the test measurements. In every table, the specification with the highest dispersion is underscored with dashed lines.

Table 3 shows a characterization for horizontal filters, while Table 4 shows the same for vertical filters. In both tables, each column corresponds to 100 measurements performed in Chip0. The dispersions are very low, being in the worst case the std/mean value of 0.38% for horizontal filters and 0.27% for vertical filters.

If the specifications in Table 2 are considered the expected output of the filters, it is found that the means of the measurements are close to them. For both filter implementations, the error of the mean for Qp and Mr is close to 0%, while the error for K is 3% maximum. For ωp, the maximum difference is 1.98% (horizontal) and 2.16% (vertical), while for Fc is 1.78% (horizontal) and 1.99% (vertical).

Table 3. Statistics of measurements by location of horizontal filters, Chip0

Filter Position	F0HA	F0HB	F1HA	F1HB	F2HA	F2HB	F3HA	F3HB

	Filter Position	F0HA	F0HB	F1HA	F1HB	F2HA	F2HB	F3HA	F3HB
K [V/V]	Mean	0.972	0.975	0.975	0.988	0.984	0.988	0.987	0.985
	Max	0.973	0.976	0.975	0.989	0.985	0.989	0.989	0.986
	Min	0.971	0.974	0.974	0.987	0.982	0.985	0.984	0.982
	Std/Mean	0.039%	0.063%	0.026%	0.029%	0.099%	0.109%	0.147%	0.096%
Qp	Mean	0.982	0.984	0.983	0.980	0.984	0.982	0.983	0.983
	Max	0.985	0.985	0.984	0.981	0.986	0.985	0.985	0.984
	Min	0.979	0.982	0.982	0.979	0.983	0.980	0.981	0.982
	Std/Mean	0.140%	0.051%	0.051%	0.057%	0.046%	0.133%	0.122%	0.037%
ωp	Mean	12846	12936	12928	12934	12900	12795	12796	12873
	Max	12951	12962	12961	13008	12957	12912	12909	12922
	Min	12779	12861	12906	12870	12815	12734	12724	12773
	Std/Mean	0.346%	0.203%	0.169%	0.191%	0.165%	0.254%	0.271%	0.219%
Fc [Hz]	Mean	2577	2598	2595	2592	2591	2567	2568	2584
	Max	2602	2602	2602	2607	2603	2594	2594	2593
	Min	2563	2583	2591	2579	2574	2555	2555	2565
	Std/Mean	0.377%	0.201%	0.174%	0.194%	0.163%	0.293%	0.305%	0.215%
Mr	Mean	1.141	1.142	1.142	1.139	1.143	1.141	1.142	1.142
	Max	1.143	1.143	1.143	1.140	1.144	1.143	1.144	1.143
	Min	1.139	1.141	1.141	1.138	1.142	1.139	1.140	1.141
	Std/Mean	0.091%	0.034%	0.033%	0.037%	0.030%	0.087%	0.080%	0.024%

Table 4. Statistics of measurements by location of vertical filters, chip 0

	Filter Position	F0VA	F1VA	F1VB	F2VA	F3VA	F3VB
K [V/V]	Mean	0.973	0.976	0.977	0.982	0.988	0.986
	Max	0.974	0.979	0.979	0.984	0.989	0.987
	Min	0.972	0.974	0.975	0.979	0.985	0.983
	Std/Mean	0.034%	0.134%	0.064%	0.128%	0.067%	0.074%
Qp	Mean	0.984	0.981	0.983	0.984	0.983	0.984
	Max	0.985	0.982	0.984	0.985	0.985	0.985
	Min	0.983	0.980	0.980	0.983	0.982	0.983
	Std/Mean	0.034%	0.052%	0.072%	0.047%	0.072%	0.047%
ωp [rad/s]	Mean	12955	12862	12959	12895	12838	12951
	Max	13003	12973	13015	12953	12911	13000
	Min	12822	12787	12908	12816	12783	12871
	Std/Mean	0.266%	0.215%	0.231%	0.193%	0.195%	0.138%

	Filter Position	F0VA	F1VA	F1VB	F2VA	F3VA	F3VB
Fc [Hz]	Mean	2602	2579	2601	2590	2578	2601
	Max	2611	2600	2610	2602	2592	2611
	Min	2574	2563	2591	2574	2565	2584
	Std/Mean	0.270%	0.212%	0.219%	0.198%	0.198%	0.138%
Mr [V/V]	Mean	1.142	1.140	1.141	1.143	1.142	1.142
	Max	1.143	1.141	1.142	1.143	1.143	1.143
	Min	1.142	1.139	1.140	1.142	1.141	1.142
	Std/Mean	0.022%	0.034%	0.047%	0.030%	0.047%	0.030%

The evaluation of the test parameters in other chips was performed through a complete set of measurements in eight chips (Chip0 to Chip7). The results of the experiments are shown in Tables 5 and 6 for the horizontal and vertical implementations, respectively. In these tables, each column considers data from 800 measurements (100 measurements for every filter implementation in a chip). The tables show an increment in the dispersions of the specifications, being the worst case for the relation std/mean of 0.66% for both filter implementations. We attribute this effect to the inter-chip variation of filters and the circuits added for the test.

However, the mean value for all measurements remains almost constant for the measurements on a single chip. The error between the means for one chip and eight chips, relative to the mean in one chip, is in the worst-case of -1.03% for the horizontal filters and 1.19% for the vertical ones.

On the other hand, Tables 3 to 6 show that it seems to be no correlation between the dispersion or the error in the mean and the number of elements included in the test signal path. For example, the F1HA filter, which has the largest number of elements added, does not have the most significant dispersion values or the greatest errors against the design specification. This is true for any of the parameters evaluated in one and eight chips. The same characteristic presents F1VB, the vertical filter with the largest number of elements added in its signal path. In this sense, we could affirm that the choice of additional resources for the test is adequate.

Table 5. Statistics of measurements by location of horizontal filters, eight devices

	Filter Position	F0HA	F0HB	F1HA	F1HB	F2HA	F2HB	F3HA	F3HB
K [V/V]	Mean	0.975	0.977	0.978	0.988	0.978	0.978	0.978	0.975
	Max	0.982	0.988	0.987	1.001	0.988	0.989	0.989	0.986
	Min	0.967	0.966	0.973	0.983	0.967	0.967	0.966	0.966
	Std/Mean	0.332	0.601	0.435	0.398	0.648	0.658	0.603	0.486
Qp	Mean	0.983	0.983	0.982	0.981	0.983	0.982	0.982	0.982
	Max	0.987	0.986	0.989	0.985	0.987	0.987	0.987	0.987
	Min	0.977	0.980	0.976	0.961	0.978	0.970	0.976	0.975
	Std/Mean	0.180	0.118	0.282	0.395	0.207	0.340	0.228	0.183
ω_p [rad/s]	Mean	12904	12937	12929	12966	12901	12904	12898	12923
	Max	13039	13049	13069	13058	13060	13069	13069	13052
	Min	12737	12733	12761	12870	12741	12734	12724	12773
	Std/Mean	0.487	0.419	0.525	0.298	0.504	0.632	0.476	0.366
Fc [Hz]	Mean	2590	2597	2594	2600	2589	2589	2588	2593
	Max	2616	2621	2620	2621	2623	2623	2616	2617
	Min	2560	2559	2562	2574	2560	2555	2555	2565
	Std/Mean	0.464	0.411	0.456	0.393	0.513	0.598	0.480	0.367
Mr [V/V]	Mean	1.142	1.142	1.141	1.140	1.142	1.141	1.141	1.141
	Max	1.145	1.144	1.146	1.143	1.145	1.145	1.145	1.144
	Min	1.137	1.139	1.136	1.126	1.138	1.132	1.137	1.136
	Std/Mean	0.117	0.077	0.183	0.255	0.135	0.221	0.148	0.119

Table 6. Statistics of measurements by location of vertical filters, eight devices

	Filter Position	F0VA	F1VA	F1VB	F2VA	F3VA	F3VB
K [V/V]	Mean	0.974	0.976	0.982	0.975	0.977	0.977
	Max	0.984	0.990	0.992	0.984	0.989	0.990
	Min	0.965	0.966	0.970	0.969	0.971	0.968
	Std/Mean	0.411%	0.641%	0.560%	0.443%	0.475%	0.552%
Qp	Mean	0.982	0.984	0.981	0.983	0.983	0.982
	Max	0.988	0.990	0.990	0.985	0.989	0.989
	Min	0.971	0.980	0.962	0.980	0.978	0.964
	Std/Mean	0.337%	0.305%	0.664%	0.121%	0.253%	0.433%
ωp [rad/s]	Mean	12968	12920	12813	12912	12974	13001
	Max	13096	13055	13015	13031	13107	13186
	Min	12799	12783	12650	12743	12783	12804
	Std/Mean	0.443%	0.512%	0.615%	0.403%	0.552%	0.564%
Fc [Hz]	Mean	2602	2595	2570	2592	2605	2609
	Max	2629	2628	2610	2617	2630	2633

	Filter Position	F0VA	F1VA	F1VB	F2VA	F3VA	F3VB
	Min	2569	2563	2543	2559	2565	2570
	Std/Mean	0.425%	0.568%	0.562%	0.399%	0.542%	0.522%
Mr [V/V]	**Mean**	1.141	1.143	1.141	1.142	1.142	1.141
	Max	1.145	1.147	1.147	1.143	1.147	1.146
	Min	1.133	1.139	1.126	1.139	1.138	1.128
	Std/Mean	0.219%	0.199%	0.429%	0.079%	0.165%	0.281%

4.2 Comparison of the test scheme with other techniques

The comparison of our scheme with previous work requires to consider other functional approaches applied to similar CUTs. However, the relatively low number of relevant papers makes it difficult to find out such a contribution.

We selected (Balen et al., 2007), which has conceptual similarities with our proposal. They indicated that the lowest functional parameter deviations in the filters under test that their scheme detect was 3%.

From Tables 3 and 4, we considered the functional parameter with the highest deviation (*fc* for F0HA). Based on the size of the sample, we established a limit of 1.41% (95% confidence level). Then, we can detect deviations in functional parameters higher than this value, which is lower than the one reported by Balen et.al. It is highlighted that this comparison considers one of the most critical performance metrics of the test strategies: their abilities for detecting deviations in the functional parameters. Due to the notably different characteristics of the CUTs, other ones would be questionable.

In addition to the previous comparison, we also resorted to experimentally obtain the frequency response of the filters under test for getting their functional parameters. This is a consistent comparison because it is performed on the same CUT for strategies that pursue the same goals.

Frequency response is the accepted method for measuring the transfer function of a filter. However, this is no easy to implement by the end-user because it usually requires the generation of a coherent multitone signal, and it could not be easy to set the frequencies of the tones, particularly for programmable filters. Also, the measurement of the attenuation band could require additional amplification, and for low-frequency filters, the settling time makes the test too long (Burns et al., 2012). The poor controllability and observability, which are characteristic of configurable analog circuits, add to these problems.

For establishing a comparative measurement, we performed an experimental determination of the frequency response of the filter specified in Table 2. For the laboratory measurements, we stimulated the filter under test with sinusoidal signals of variable frequency and acquired the response of the filter with an oscilloscope in averaging mode (128 samples). To mitigate the noise at the filter output, we adjusted a curve to each filter output using the MatLab © Curve Fitting application.

We decided not to use a multitone coherent signal for simplifying the signal generation, incurring in this way in longer test time. The experiment was performed in Chip0, configuring only the filters that allow the application of the input stimulus directly from a pin. In this way, we avoided using additional blocks that could generate additional noise or distort the input signal. For this reason, only seven implementations were evaluated: F0HA|B, F3HA|B, F0VA, F3VA|B. Table 7 shows the parameters measured, where each measurement is the mean of three evaluations of the frequency response.

Table 7. Frequency response parameters evaluation, Chip0.

Filter	K	Fc -3dB	Mr [V/V]	Qp	ωp [rad/s]
F0HA	1.002	2597	1.139	0.991	12774
F0HB	1.004	2598	1.141	0.991	12767

Filter	K	Fc -3dB	Mr [V/V]	Qp	ωp [rad/s]
F3HA	1.000	2597	1.137	0.991	12786
F3HB	1.004	2598	1.142	0.990	12774
F0VA	1.003	2597	1.140	0.990	12780
F3VA	1.004	2597	1.140	0.989	12780
F3VB	1.002	2597	1.138	0.990	12786

The error between the two measurements, related to the frequency response, is shown in Table 9. In TRAM, we use the average of the measurements of Chip0. The most significant differences are in the gain, while the other parameters have minimal differences, less than 1.32%. This indicates that the results present a good correlation, suggesting that the proposed strategy could be used as an alternative to the frequency response measurement.

Table 8. Relative errors between the frequency response and our proposal, chip0

Filter	**K**	**Fc -3dB**	**Mr [V/V]**	**Qp**	**ωp [rad/s]**
F0HA	3.033%	0.770%	0.180%	0.910%	0.569%
F0HB	3.206%	0.809%	0.041%	0.901%	0.619%
F3HA	2.823%	0.770%	0.292%	0.985%	0.470%
F3HB	2.943%	0.019%	0.004%	0.619%	1.269%
F0VA	2.774%	0.020%	0.178%	0.642%	1.219%
F3VA	2.889%	0.020%	0.192%	0.568%	1.219%
F3VB	2.868%	0.176%	0.344%	0.613%	1.320%

The difference between the frequency response and to the specifications of Table 2 is shown in Table 9. The table shows that both are very close, being the highest relative error of 1.783%.

Table 9. Relative errors of frequency response concerning the specifications, chip0

Filter	**K**	**Fc -3dB**	**Mr [V/V]**	**Qp**	**ωp [rad/s]**
F0HA	0.219%	1.744%	0.371%	0.696%	0.699%
F0HB	0.398%	1.783%	0.150%	0.687%	0.650%

F3HA	0.003%	1.744%	0.483%	0.773%	0.798%
F3HB	0.425%	1.783%	0.049%	0.615%	0.699%
F0VA	0.251%	1.744%	0.231%	0.639%	0.749%
F3VA	0.370%	1.744%	0.245%	0.564%	0.749%
F3VB	0.193%	1.744%	0.386%	0.626%	0.798%

The errors between our proposal and the frequency response method are small, and both methods present results that are close to the specifications. Then, the expected response pattern of the filter without failures could be obtained from a simulation of the frequency response of the filter with the capacitor values given by the IDE. This is very useful since it facilitates the implementation for the final user and overcomes the limitation of the frequency response method.

5. Perspectives

5.1 Extension to bandpass filters

Our work focuses on lowpass filters but does not consider the bandpass ones. It should be noted that highpass characteristics can not be implemented in the device (Cypress Semiconductor, 2018).

Some features of the general test strategy successfully experimented can support the extension of the strategy to bandpass filters. The first is the signal manipulation that demonstrated to be useful for reducing the high noise level in the test signals. The second is the procedure for determining the transient response parameters and the specifications. The third is the use of dynamic reconfiguration that allows low test overhead. The fourth is the signal paths and added blocks that showed good performance. Finally, the demonstration that economical equipment can be successfully used for implementing our strategy is vital. Given the relatively low frequencies responses of the filters able to be implemented in PSOC1, it is reasonable to expect that the extension to bandpass filters can make use of the features already presented in this work. However, new research must validate the extension.

5.2. Built-in Self-Test implementation

The implementation of the test scheme as a Built-In Self-Test (BIST) requires including an ADC in the same chip. To explore the feasibility of this possibility, we use an eight-bits ΔΣ ADC that is available in PSoC1. The results from the analog conversion are averaged 128 times and processed in the same manner used for the oscilloscope measurements presented in section 5.

Fig. 12 plots a comparison of a waveform acquired with the oscilloscope against one obtained using the internal converter of PSoC1. As can be seen, there are no significant differences among them. The waveform obtained from PSoC1 seems to be smoother than the one acquired at the oscilloscope, but this is due to the internal ADC has a much lower sample rate than the instrument and lose some information. A closer look into the waveforms, as shown in Fig. 12, reveals this effect. Additionally, these results can be improved by using better-quality resources like those available in complex systems where PSoC1 devices could perform as analog coprocessors. On the other hand, the diversity of resources present in PSoC1 would make it possible to measure the test parameters internally. However, this implementation is left for future work.

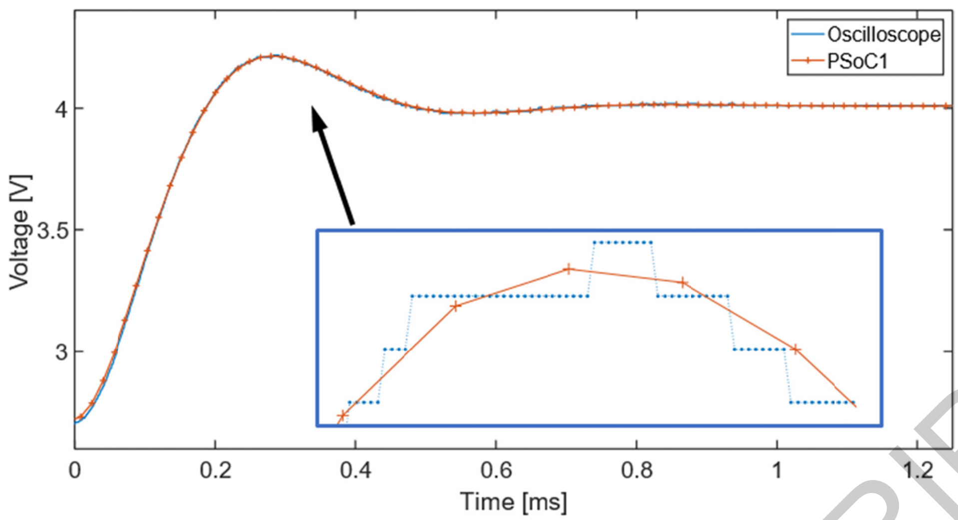

Figure 12 Comparison between measurements using an oscilloscope and a PSoC1 ADC

6. Conclusions

In this work, we addressed the test of lowpass switched capacitors filters embedded in the analog configurable array of a PSOC1 µC, adopting a functional approach that combines TRAM with concepts of the software-based test. The proposal is novel and comprehensive, covering all possible lowpass filters in the device. The combination of internal resources for test stimuli generation and external but inexpensive equipment allows obtaining a low-cost test scheme. Our characterization campaign, completely experimental, gives an excellent and reliable basis for the straightforward application of the strategy. The test signal processing approach proposed in the paper demonstrated to be very stable, overcoming the adverse noise conditions present in the system under test. Our work contributes by providing a viable solution for small companies, since the tools used commonly in the industry and can be implemented by design engineers, without resorting to specialists.

Our scheme requires an acquisition system and a laptop for signal processing. Despite the feasibility of implementing a BIST with the internal resources is explored slightly in the paper, exhaustive research has to be done for demonstrating its efficiency. Additionally, the test requires validation for bandpass filters. However, we consider that the ideas an data in the paper contribute to facilitating the extension to other filters and the formulation of BIST schemes.

7. References

Ananda Mohan, P. V. (2012). *VLSI Analog Filters: Active RC, OTA-C, and SC*. New York: Birkhäuser Boston.

Andrade, A., Vieira, G., Balen, T. R., Lubaszewski, M., Azaïs, F., & Renovell, M. (2005). Built-in self-test of global interconnects of field programmable analog arrays. *Microelectronics Journal*, *36*(12), 1112–1123. https://doi.org/10.1016/j.mejo.2005.06.001

Balen, T.R., Calvano, J. V., Lubaszewski, M. S., & Renovell, M. (2006). Functional Test of Field Programmable Analog Arrays. *24th IEEE VLSI Test Symposium*, 326–333. https://doi.org/10.1109/VTS.2006.37

Balen, Tiago R., Calvano, J. V., Lubaszewski, M. S., & Renovell, M. (2007). Built-in self-test of field programmable analog arrays based on transient response analysis. *Journal of Electronic Testing: Theory and Applications (JETTA)*, *23*(6), 497–512. https://doi.org/10.1007/s10836-007-5004-8

Burns, M., Roberts, G., & Taenzler, F. (2012). *An introduction to mixed-signal IC test and measurement 2nd Ed.* New York: Oxford University Press.

Bushnell, M., & Agrawal, V. (2002). *Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits*. https://doi.org/10.1007/b117406

Calvano, J. V. V., Alves, V. C., Lubaszewski, M., Castro Alves, V., & Lubaszewski, M. (1999). Fault detection in systems with 2nd order dynamics using transient analysis. *Proceedings - 12th Symposium on Integrated Circuits and Systems Design, SBCCI 1999*, 110–114. https://doi.org/10.1109/SBCCI.1999.803099

Cypress Semiconductor. (2017a). *AN2104 - PSoC® 1 - Dynamic Reconfiguration with PSoC Designer™* (Revision G). San Jose, CA.

Cypress Semiconductor. (2017b). *PSoC® Programmable System-on-Chip Technical Reference Manual* (Revision K). San Jose, CA.

Cypress Semiconductor. (2018). *AN2168 - PSoC® 1 - Understanding Switched Capacitor Filters Application Note* (Revision E). San Jose, CA.

Golonek, T., & Machniewski, J. (2018). Analog Circuit Specification Testing by Means of Walsh–Hadamard Transform and Multiple Regression Supported by Evolutionary Computations. In *Circuits, Systems, and Signal Processing* (Vol. 37). https://doi.org/10.1007/s00034-017-0708-1

Gomez-Pau, A., Balado, L., & Figueras, J. (2015). Analog circuits testing using digitally coded indirect measurements. *Proceedings - 2015 10th IEEE International Conference on Design and Technology of Integrated Systems in Nanoscale Era, DTIS 2015*. https://doi.org/10.1109/DTIS.2015.7127357

Hasler, J. (2019). Analog architecture complexity theory empowering ultra-low power configurable analog and mixed mode SoC systems. *Journal of Low Power Electronics and Applications*, *9*(1), 1–38. https://doi.org/10.3390/jlpea9010004

Hatzopoulos, A. A. (2017). Analog circuit testing. *Proceedings of the 2017 IEEE 22nd International Mixed-Signals Test Workshop, IMSTW 2017*, 1–6. https://doi.org/10.1109/IMS3TW.2017.7995206

Laprovitta, A., Peretti, G., & Romero, E. (2014). Applying the analog configurability test approach in a wireless sensor network application. *Journal of Electrical and Computer Engineering*, *2014*, 1–14. https://doi.org/10.1155/2014/309193

Lovay, M., Peretti, G., & Romero, E. (2015). Implementation of an adaptive filter using an evolvable hardware strategy. *IEEE Latin America Transactions*, *13*(4), 927–934. https://doi.org/10.1109/TLA.2015.7106339

Ogata, K. (2010). *Modern control engineering* (Fifth ed.). Upper Saddle River, NJ: Prentice-Hall.

Schlottmann, C. R., Shapero, S., Nease, S., & Hasler, P. (2012). A digitally enhanced dynamically reconfigurable analog platform for low-power signal processing. *IEEE Journal of Solid-State Circuits*, *47*(9), 2174–2184. https://doi.org/10.1109/JSSC.2012.2194847

Suda, N., Suh, J., Hakim, N., Cao, Y., & Bakkaloglu, B. (2016). A 65 nm Programmable ANalog Device Array (PANDA) for Analog Circuit Emulation. *IEEE Transactions on Circuits and Systems I: Regular Papers*, *63*(2), 181–190. https://doi.org/10.1109/TCSI.2015.2512718

Ting, H. W., & Chen, C. Y. (2018). A VLSI On-Chip Analog High-Order Low-Pass Filter Performance Evaluation Strategy. *IEEE Transactions on Instrumentation and Measurement*, *67*(3), 621–633. https://doi.org/10.1109/TIM.2017.2786599

Twigg, C., & Hasler, P. (2009). Configurable analog signal processing. *Digital Signal Processing: A Review Journal*, *19*(6), 904–922. https://doi.org/10.1016/j.dsp.2007.09.013

Vock, S. R., Escalona, O. J., Turner, C., & Owens, F. J. (2012). Challenges for semiconductor test engineering: A review paper. *Journal of Electronic Testing: Theory and Applications (JETTA)*, *28*(3), 365–374. https://doi.org/10.1007/s10836-011-5276-x

Figures captions

(1) Figure 1. PSoC1 architectural description

(2) Figure 2. Schematic diagram of the filters under test

(3) Figure 3. Second-order filter step response, and test parameters *Tp*, *OS*, V_{ini}, V_{final}, and V_{peak}.

(4) Figure 4. General test scheme

(5) Figure 5. Normal to test mode switching example

(6) Figure 6. Simplified scheme of a PGA configured as a step signal generator

(7) Figure 7. Resources used to test horizontal filters

(8) Figure 8. Resources used to test vertical filters

(9) Figure 9. Connection scheme for testing horizontal filters in row 2

(10) Figure 10. Figure 15. Experimental measurement of filter F1VB without averaging.

(11) Figure 11. Waveform obtained from the oscilloscope (average mode) and its smoothed curve

(12) Figure 12 Comparison between measurements using an oscilloscope and a PSoC1 ADC

Table 10. Resources of the filters that can be configured in PSoC1

Filter	Input SC block	Output SC block
F0HA|B	ASC10	ASD11
F1HA|B	ASC21	ASD20
F2HA|B	ASC12	ASD13
F3HA|B	ASC23	ASD22
F0VA	ASC10	ASD20
F1VA|B	ASC21	ASD11
F2VA	ASC12	ASD22
F3VA|B	ASC23	ASD13

Table 11. Specifications of the filter under test

Feature	Value
Edge frequency (0 dB cross) (Hz)	1990.0
-3dB frequency (Hz)	2552.5
Band-pass ripple (V/V)	1.14
DC Gain (V/V)	1.0
ω_p (rad/s)	12685
Qp	0.98
Sampling frequency [KHz]	200

Table 12. Statistics of measurements by location of horizontal filters, Chip0

	Filter Position	0HA	0HB	1HA	1HB	F	2HA	2HB	3HA	3HB
[V/V]	Mean	.972	.975	.975	.988	0	.984	.988	.987	.985
	Max	.973	.976	.975	.989	0	.985	.989	.989	.986
	Min	.971	.974	.974	.987	0	.982	.985	.984	.982
	Std/ Mean	.039%	.063%	.026%	.029%	0	.099%	.109%	.147%	.096%
p	Mean	.982	.984	.983	.980	0	.984	.982	.983	.983
	Max	.985	.985	.984	.981	0	.986	.985	.985	.984
	Min	.979	.982	.982	.979	0	.983	.980	.981	.982
	Std/ Mean	.140%	.051%	.051%	.057%	0	.046%	.133%	.122%	.037%
p [rad/s]	Mean	2846	2936	2928	2934	1	2900	2795	2796	2873
	Max	2951	2962	2961	3008	1	2957	2912	2909	2922
	Min	2779	2861	2906	2870	1	2815	2734	2724	2773
	Std/ Mean	.346%	.203%	.169%	.191%	0	.165%	.254%	.271%	.219%
c [Hz]	Mean	577	598	595	592	2	591	567	568	584
	Max	602	602	602	607	2	603	594	594	593
	Min	563	583	591	579	2	574	555	555	565
	Std/ Mean	.377%	.201%	.174%	.194%	0	.163%	.293%	.305%	.215%
r [V/V]	Mean	.141	.142	.142	.139	1	.143	.141	.142	.142

	Max	.143	.143	.143	1.140	.144	.143	.144	.143
	Min	.139	.141	.141	1.138	.142	.139	.140	.141
	Std/Mean	.091%	.034%	.033%	0.037%	.030%	.087%	.080%	.024%

Table 13. Statistics of measurements by location of vertical filters, chip 0

	Filter Position	F0VA	F1VA	F1VB	F2VA	F3VA	F3VB
K [V/V]	Mean	0.973	0.976	0.977	0.982	0.988	0.986
	Max	0.974	0.979	0.979	0.984	0.989	0.987
	Min	0.972	0.974	0.975	0.979	0.985	0.983
	Std/Mean	0.034%	0.134%	0.064%	0.128%	0.067%	0.074%
Qp	Mean	0.984	0.981	0.983	0.984	0.983	0.984
	Max	0.985	0.982	0.984	0.985	0.985	0.985
	Min	0.983	0.980	0.980	0.983	0.982	0.983
	Std/Mean	0.034%	0.052%	0.072%	0.047%	0.072%	0.047%
ωp [rad/s]	Mean	12955	12862	12959	12895	12838	12951
	Max	13003	12973	13015	12953	12911	13000
	Min	12822	12787	12908	12816	12783	12871
	Std/Mean	0.266%	0.215%	0.231%	0.193%	0.195%	0.138%
Fc [Hz]	Mean	2602	2579	2601	2590	2578	2601
	Max	2611	2600	2610	2602	2592	2611
	Min	2574	2563	2591	2574	2565	2584
	Std/Mean	0.270%	0.212%	0.219%	0.198%	0.198%	0.138%
Mr [V/V]	Mean	1.142	1.140	1.141	1.143	1.142	1.142
	Max	1.143	1.141	1.142	1.143	1.143	1.143
	Min	1.142	1.139	1.140	1.142	1.141	1.142
	Std/Mean	0.022%	0.034%	0.047%	0.030%	0.047%	0.030%

Table 14. Statistics of measurements by location of horizontal filters, eight devices

	Filter Position	0HA	0HB	1HA	1HB	2HA	2HB	3HA	3HB
[V/V]	Mean	.975	.977	.978	.988	.978	.978	.978	.975

	Max	.982	.988	.987	.001	.988	.989	.989	.986
	Min	.967	.966	.973	.983	.967	.967	.966	.966
	Std/Mean	.332%	.601%	.435%	.398%	.648%	.658%	.603%	.486%
p	Mean	.983	.983	.982	.981	.983	.982	.982	.982
	Max	.987	.986	.989	.985	.987	.987	.987	.987
	Min	.977	.980	.976	.961	.978	.970	.976	.975
	Std/Mean	.180%	.118%	.282%	.395%	.207%	.340%	.228%	.183%
p [rad/s]	Mean	2904	2937	2929	2966	2901	2904	2898	2923
	Max	3039	3049	3069	3058	3060	3069	3069	3052
	Min	2737	2733	2761	2870	2741	2734	2724	2773
	Std/Mean	.487%	.419%	.525%	.298%	.504%	.632%	.476%	.366%
c [Hz]	Mean	590	597	594	600	589	589	588	593
	Max	616	621	620	621	623	623	616	617
	Min	560	559	562	574	560	555	555	565
	Std/Mean	.464%	.411%	.456%	.393%	.513%	.598%	.480%	.367%
r [V/V]	Mean	.142	.142	.141	.140	.142	.141	.141	.141
	Max	.145	.144	.146	.143	.145	.145	.145	.144
	Min	.137	.139	.136	.126	.138	.132	.137	.136
	Std/Mean	.117%	.077%	.183%	.255%	.135%	.221%	.148%	.119%

Table 15. Statistics of measurements by location of vertical filters, eight devices

	Filter Position	F0VA	F1VA	F1VB	F2VA	F3VA	F3VB
K [V/V]	Mean	0.974	0.976	0.982	0.975	0.977	0.977
	Max	0.984	0.990	0.992	0.984	0.989	0.990
	Min	0.965	0.966	0.970	0.969	0.971	0.968
	Std/Mean	0.411%	0.641%	0.560%	0.443%	0.475%	0.552%
Q p	Mean	0.982	0.984	0.981	0.983	0.983	0.982
	Max	0.988	0.990	0.990	0.985	0.989	0.989
	Min	0.971	0.980	0.962	0.980	0.978	0.964
	Std/Mean	0.337%	0.305%	0.664%	0.121%	0.253%	0.433%
ω p [rad/s]	Mean	12968	12920	12813	12912	12974	13001
	Max	13096	13055	13015	13031	13107	13186

	Min	12799	12783	12650	12743	12783	12804
	Std/Mean	0.443%	0.512%	0.615%	0.403%	0.552%	0.564%
Fc [Hz]	Mean	2602	2595	2570	2592	2605	2609
	Max	2629	2628	2610	2617	2630	2633
	Min	2569	2563	2543	2559	2565	2570
	Std/Mean	0.425%	0.568%	0.562%	0.399%	0.542%	0.522%
Mr [V/V]	Mean	1.141	1.143	1.141	1.142	1.142	1.141
	Max	1.145	1.147	1.147	1.143	1.147	1.146
	Min	1.133	1.139	1.126	1.139	1.138	1.128
	Std/Mean	0.219%	0.199%	0.429%	0.079%	0.165%	0.281%

Table 16. Frequency response parameters evaluation, Chip0.

Filter	K	Fc -3dB	Mr [V/V]	Qp	ωp [rad/s]
F0HA	1.002	2597	1.139	0.991	12774
F0HB	1.004	2598	1.141	0.991	12767
F3HA	1.000	2597	1.137	0.991	12786
F3HB	1.004	2598	1.142	0.990	12774
F0VA	1.003	2597	1.140	0.990	12780
F3VA	1.004	2597	1.140	0.989	12780
F3VB	1.002	2597	1.138	0.990	12786

Table 17. Relative errors between the frequency response and our proposal, chip0

Filter	K	Fc -3dB	Mr [V/V]	Qp	ωp [rad/s]
F0HA	3.033%	0.770%	0.180%	0.910%	0.569%
F0HB	3.206%	0.809%	0.041%	0.901%	0.619%
F3HA	2.823%	0.770%	0.292%	0.985%	0.470%
F3HB	2.943%	0.019%	0.004%	0.619%	1.269%
F0VA	2.774%	0.020%	0.178%	0.642%	1.219%
F3VA	2.889%	0.020%	0.192%	0.568%	1.219%
F3VB	2.868%	0.176%	0.344%	0.613%	1.320%

Table 18. Relative errors of frequency response with respect to the specifications, chip0

Filter	K	Fc -3dB	Mr [V/V]	Qp	ωp [rad/s]
F0HA	0.219%	1.744%	0.371%	0.696%	0.699%
F0HB	0.398%	1.783%	0.150%	0.687%	0.650%
F3HA	0.003%	1.744%	0.483%	0.773%	0.798%
F3HB	0.425%	1.783%	0.049%	0.615%	0.699%
F0VA	0.251%	1.744%	0.231%	0.639%	0.749%
F3VA	0.370%	1.744%	0.245%	0.564%	0.749%
F3VB	0.193%	1.744%	0.386%	0.626%	0.798%

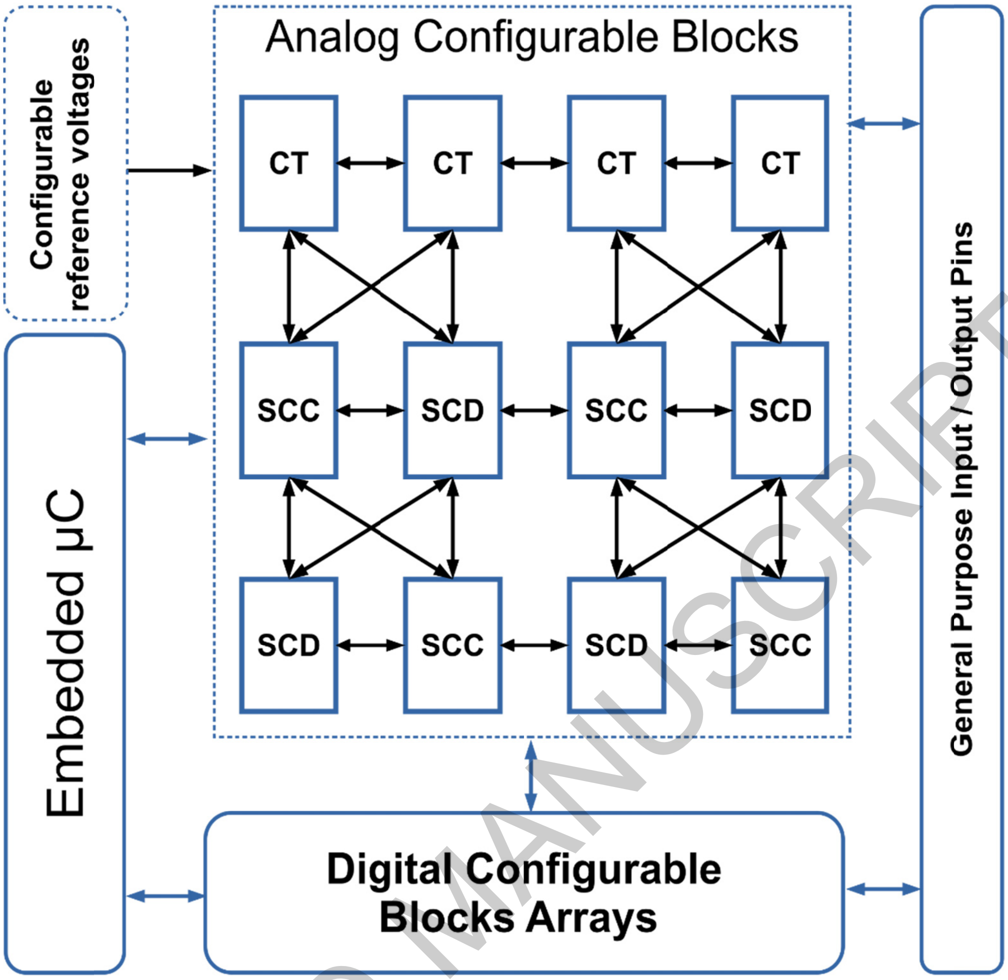

Figure 13. PSoC1 architectural description

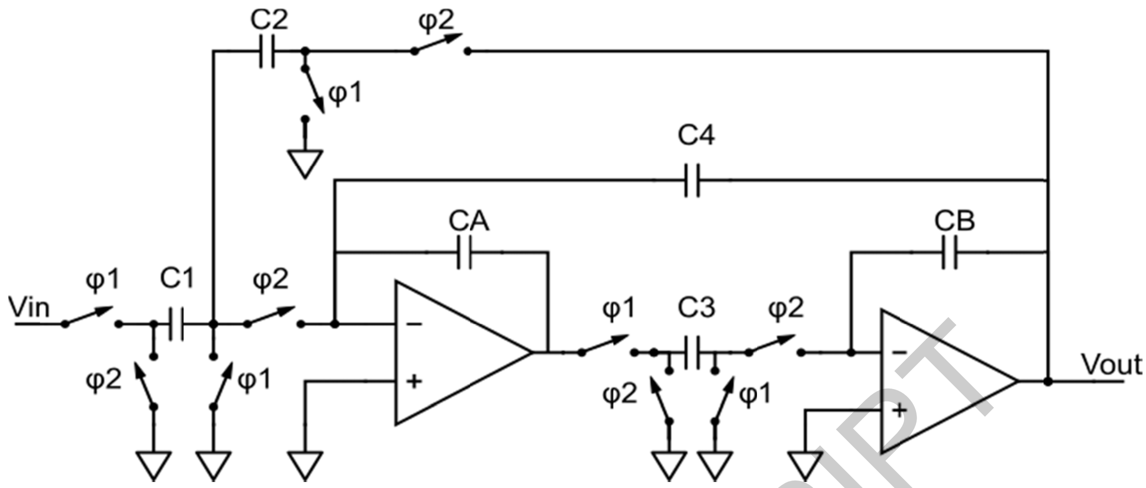

Figure 2. Schematic diagram of the filter under test

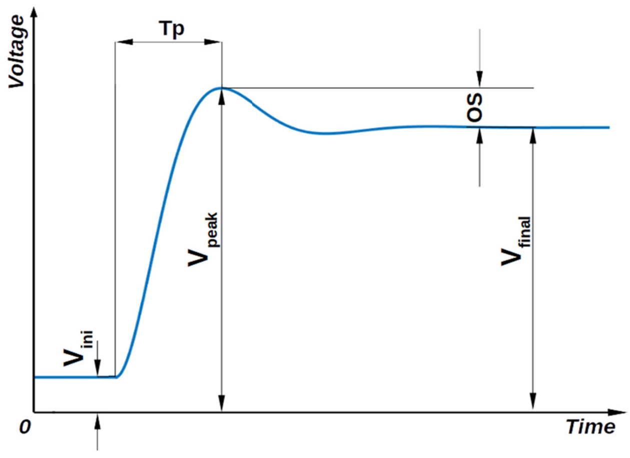

Figure 3. Second-order filter step response, and test parameters Tp, OS, V_{ini}, V_{final}, and V_{peak}.

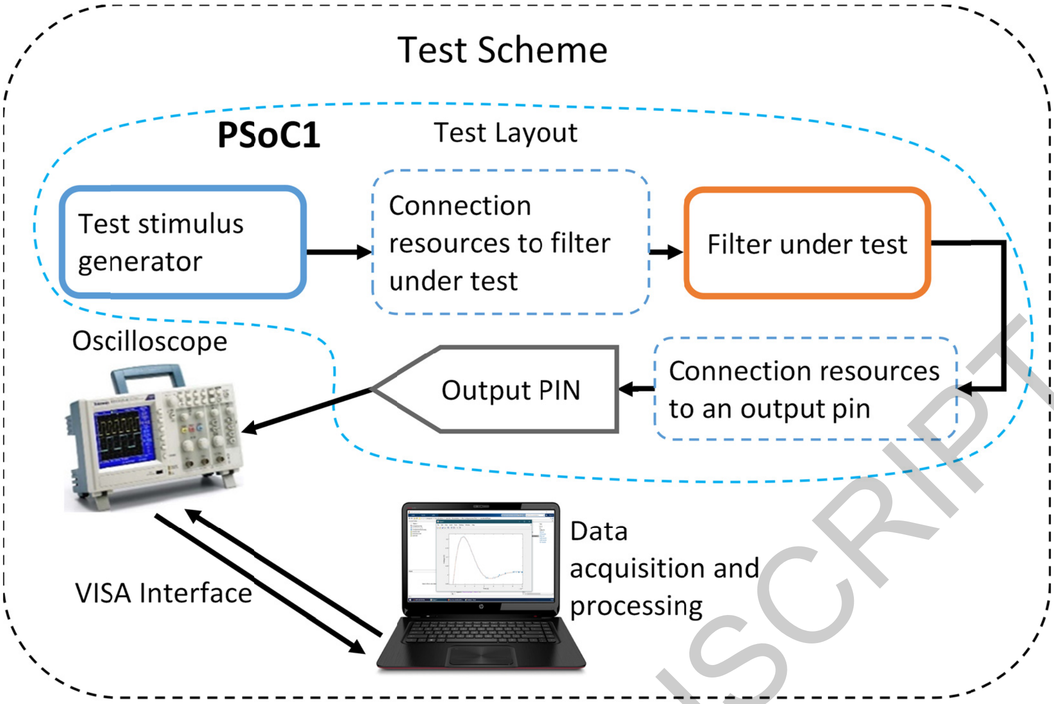

Figure 4. General test scheme

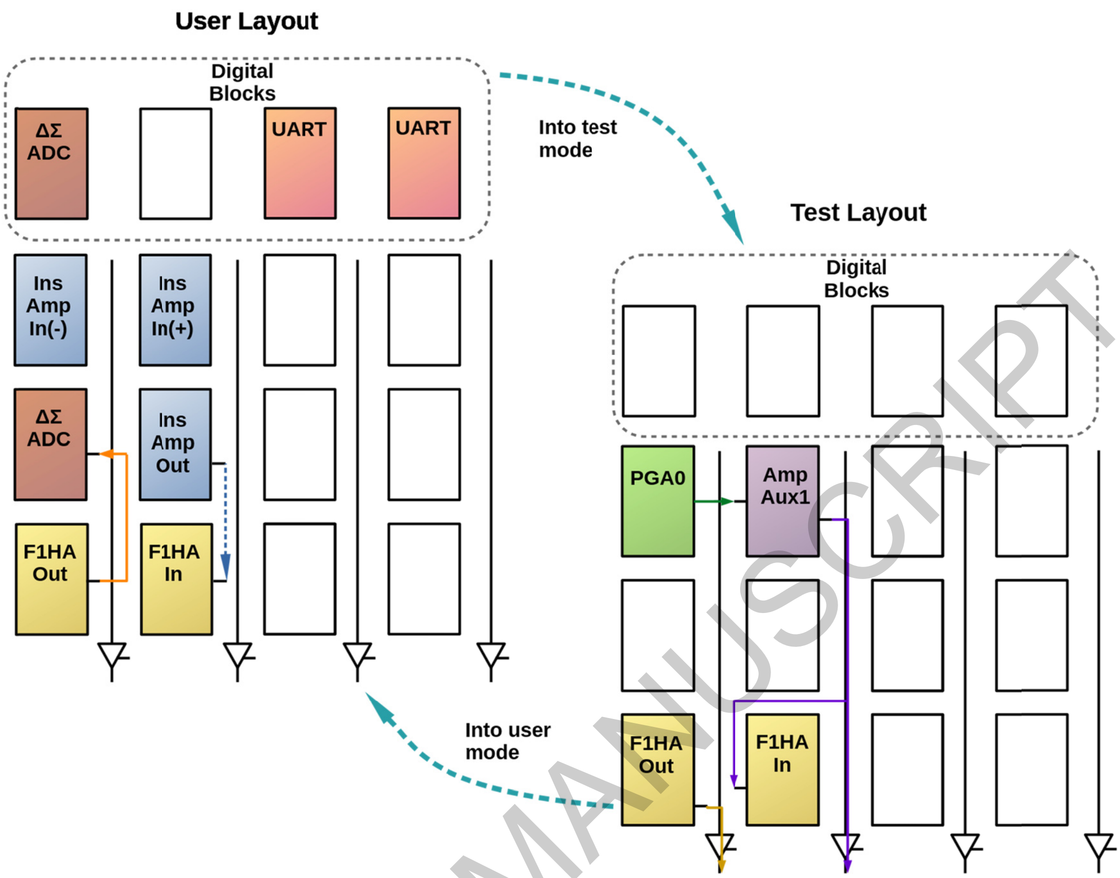

Figure 5. Normal to test mode switching example

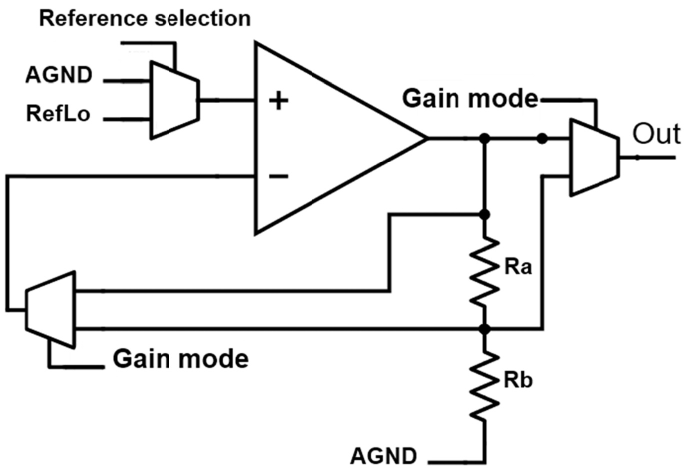

Figure 6. Simplified scheme of a PGA configured as a step signal generator

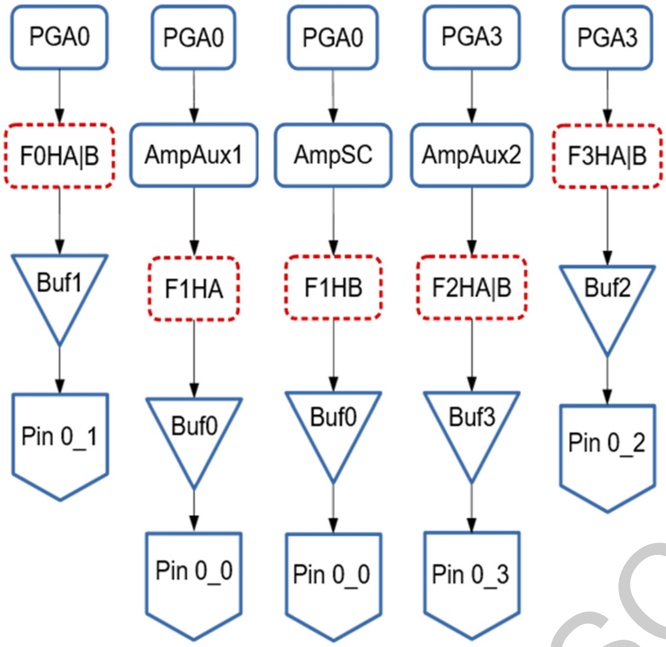

Figure 7. Resources used to test horizontal filters.

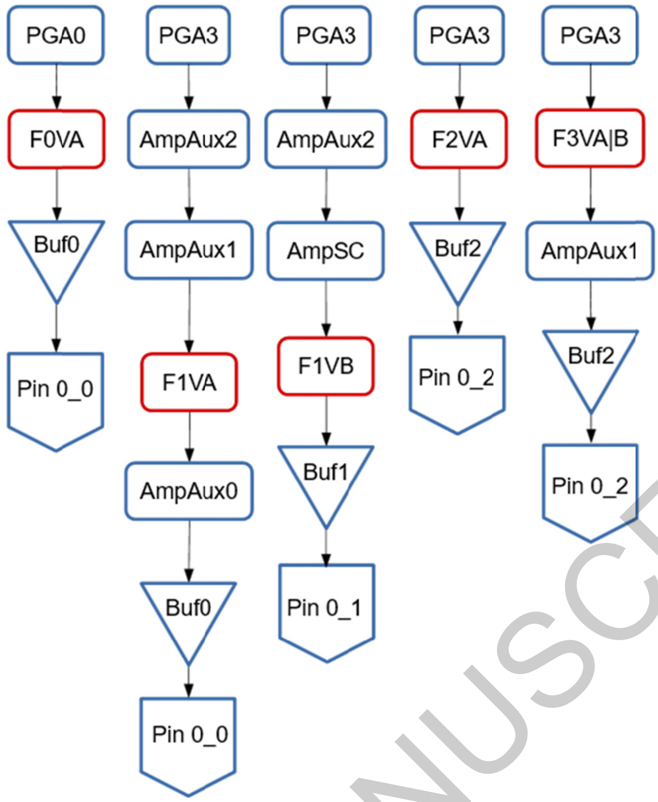

Figure 8. Resources used to test vertical filters

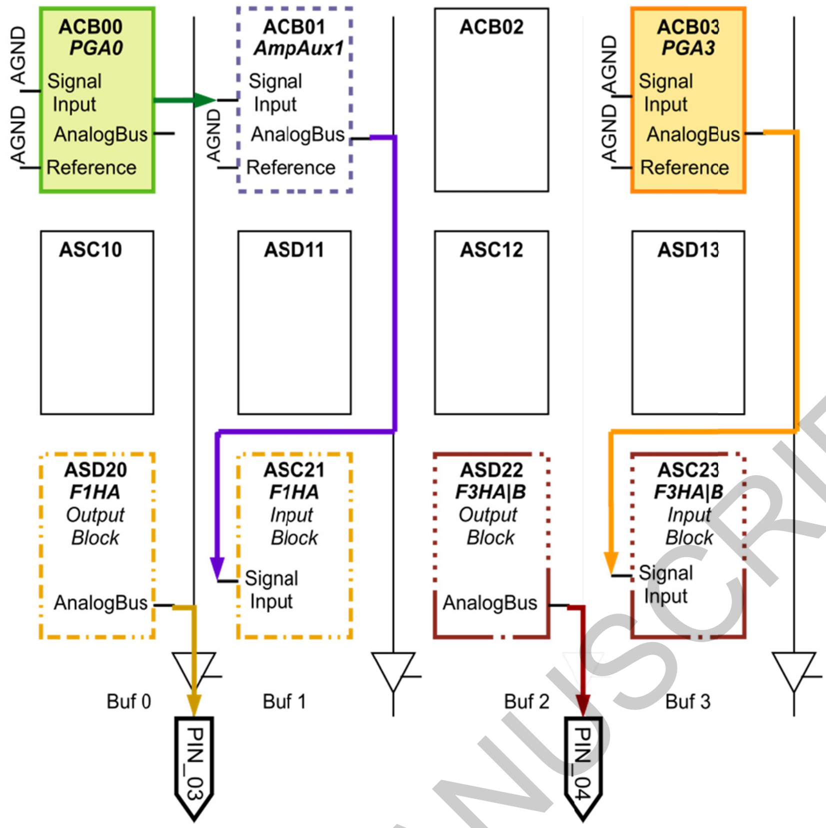

Figure 9. Connection scheme for testing horizontal filters in row 2

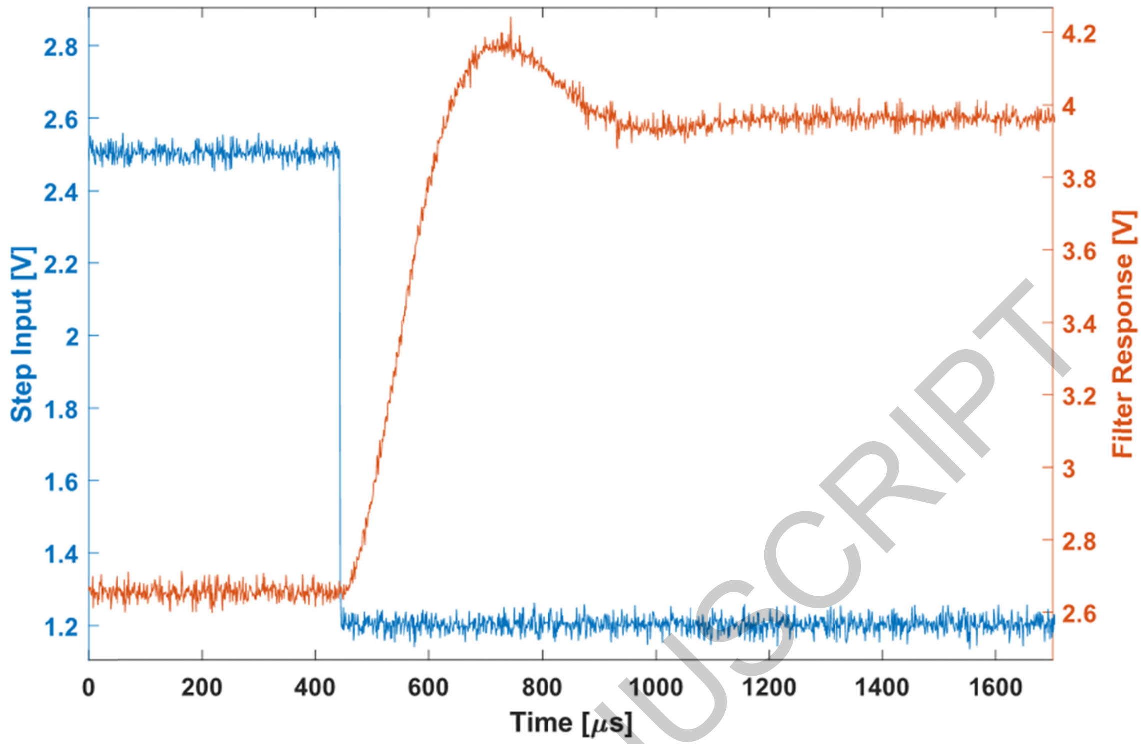

Figure 10. Experimental measurement of filter FIVB without averaging

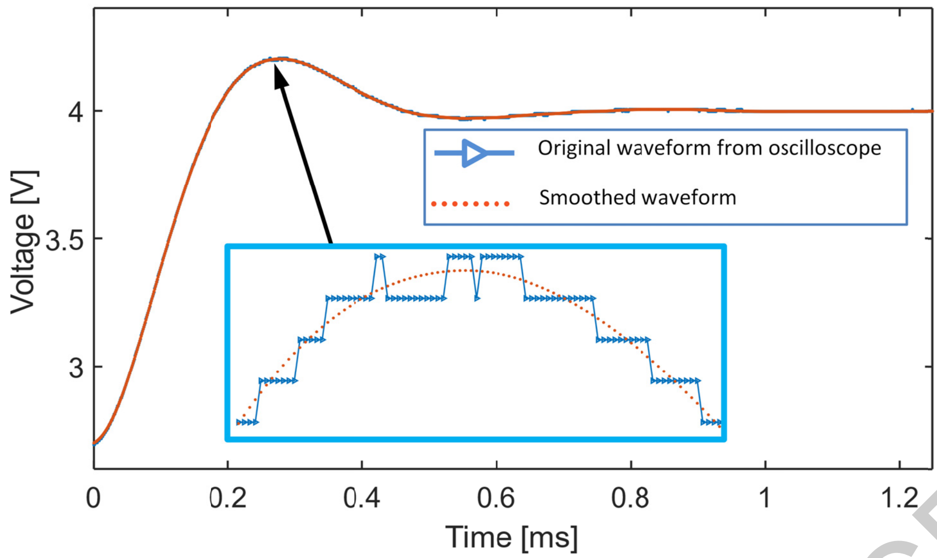

Figure 11. Waveform obtained from the oscilloscope (average mode) and its smoothed curve

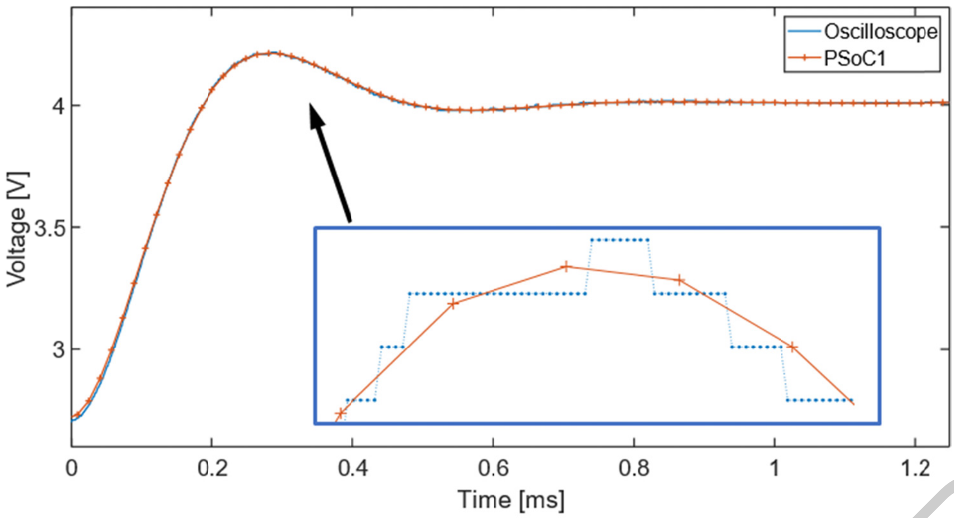

Figure 12. Comparison between measurements using an oscilloscope and a PSoC1 ADC