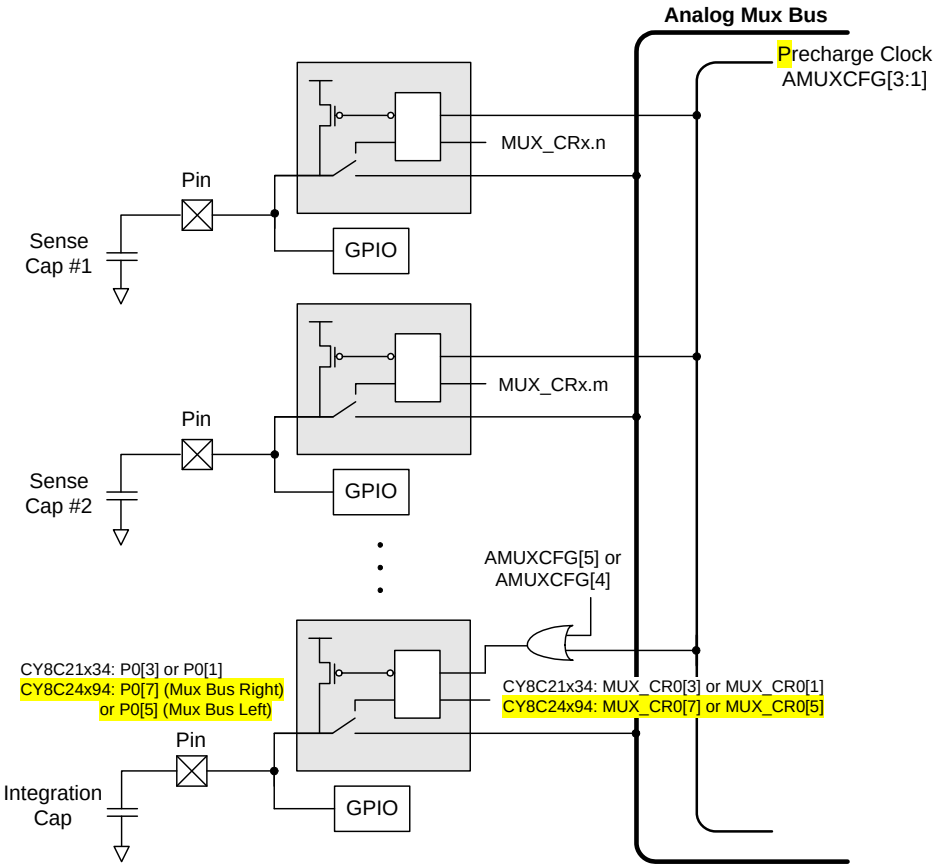

Figure 33-3. CY8C24x94, CY8C21x34, CY8C21x34B, CY7C64215, CY7C603xx, CYWUSB6953 Capacitance Sense Example Diagram

33.3.2 Chip-Wide Analog Input

The analog bus forms a multiplexer across many IO pins. This allows any of these pins to be brought into the analog system for processing, as shown in Figure 33-1. The Port 0 pins are also brought through separate mux paths to the continuous time block, so Port 0 inputs can be routed to the analog system by either path. In the CY8C24x94 and CY7C64215, some Port 2 inputs have a dedicated path to switched capacitor blocks.

In the CY8C21x34, CY8C21x34B, CY7C603xx, and CYWUSB6953 PSoC devices, the pins can be connected to a single bus. In the CY8C24x94 and CY7C64215 PSoC devices, odd pins are connected to one bus, even pins to the other bus. The two mux buses can be shorted together using the switch controlled by the SplitMux bit.

33.3.3 Crosspoint Switch

The bidirectional nature of the analog mux switches allows a direct connection between any of the IO pins, as shown in Figure 33-1. Enabling two (or more) pins at the same time connects these pins together, with approximately 400 ohms of resistance between each pin and the analog mux bus. As long as the clock choice in the AMUX_CFG register is set to the fixed ‘0’ case, the switches will be static, controlled only by the state of the individual switch enable bits in the MUX_CRx registers. The crosspoint can be reconfigured at any time and the user can provide a break-before-make function with firmware if needed.