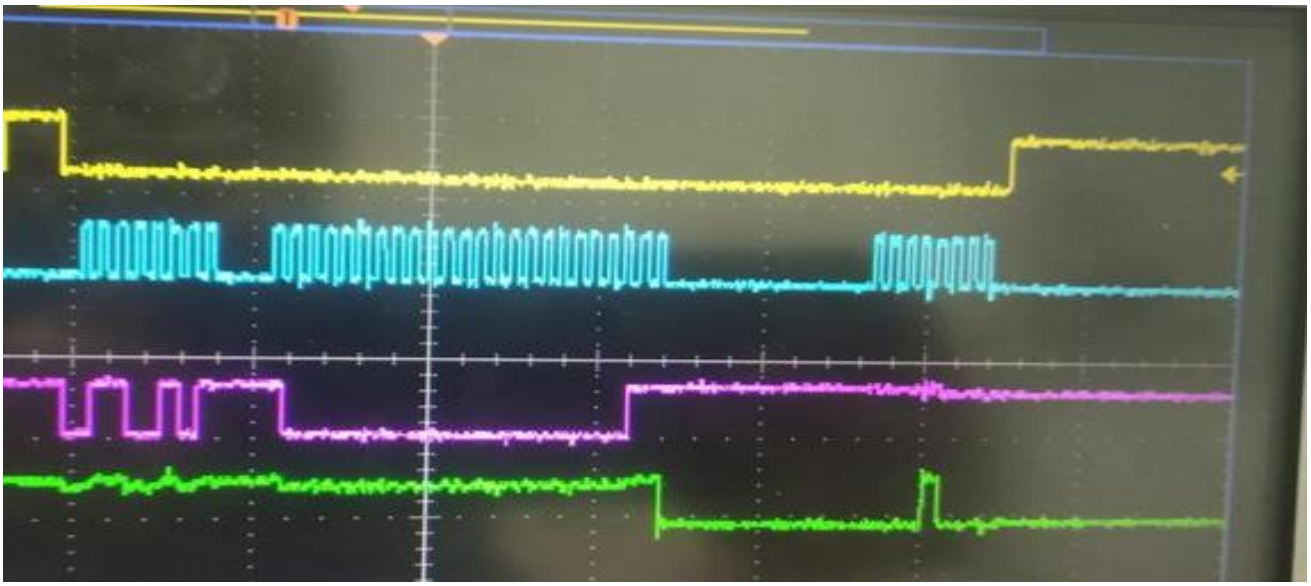
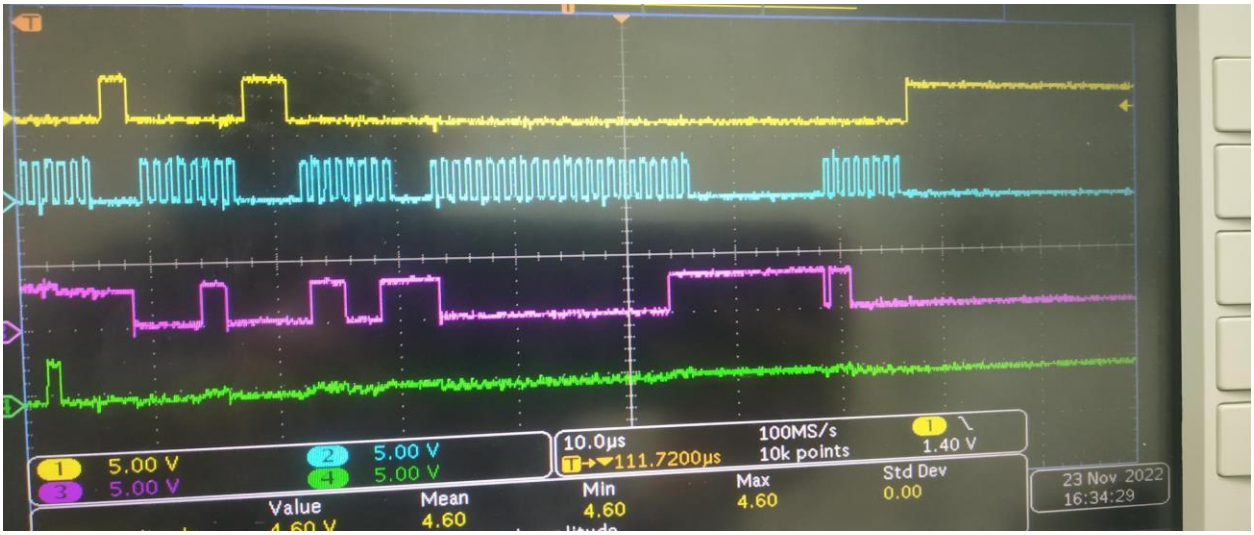
READ MODE (1S-1S-1S) -CFGR 2



Bit number	Name	Function	Read/Write N = Nonvolatile V = Volatile	Factory default (binary)	Description
CFR2N[7] CFR2V[7]	ADRBYT	Address Byte Length selection between 3 or 4 bytes for Instructions	N -> R/W V -> R/W	0	Description: The ADRBYT bit controls the expected address length for all instructions that require address and is selectable between 3 Bytes or 4 Bytes. Selection Options: 0 = Instructions will use 3 Bytes for address 1 = Instructions will use 4 Bytes for address Dependency: N/A
CFR2N[6] CFR2V[6]	QPI-IT	QPI Interface & Protocol Selection - I/O width set to 4 bits (4-4-4)	N -> R/W V -> R/W	0	Description: The QPI-IT bit selects the I/O width of the device to be 4-bits wide. When configured to 4-bits (QPI-IT, QUADIT), WP# becomes DQ2 and DQ3_RESET# becomes DQ3. The QPI-IT transactions require Opcode, Address and Data always sent on all four I/Os. Selection Options: 0 = Data Width set to 1 or 2 bits wide (1x - Single, 2x - Dual) - Legacy Protocol 1 = Data Width set to 4 wide (4x - Quad) - QPI Protocol Dependency: N/A
CFR2N[5] CFR2V[5]	DQ3RST	DQ3 and RESET Selection for DQ3 - Multiplexed operation on I/O #3	N -> R/W V -> R/W	0	Description: The DQ3RST bit controls the RESET# behavior on DQ3 signal. When enabled, a LOW on DQ3 will perform a hardware reset while CS# is HIGH. This multiplexed functionality on DQ3 is only available when QUADIT or QPI-IT interface modes are enabled. Disabling QUADIT or QPI-IT modes makes DQ3 a dedicated RESET# pin. Selection Options: 0 = DQ3 has no multiplexed RESET# function 1 = DQ3 performs a hardware reset when LOW provided CS# is HIGH Dependency: N/A
CFR2N[4] CFR2V[4]	RESRVD	Reserved for future use	N -> R/W V -> R/W	0	These bits are Reserved for future use. This bit must always be written/loaded to its default state.
CFR2N[3:0] CFR2V[3:0]	MEMLAT[3:0]	Memory Array Read Latency selection - Dummy cycles required for initial data access	N -> R/W V -> R/W	1000	Description: The MEMLAT[3:0] bits control the read latency (dummy cycles) delay in all variable latency memory array and nonvolatile register read transactions. MEMLAT selection allows the user to adjust the read latency during normal operation based on different operating frequencies (see **Table 49**). Selection Options: 0000 = 0 Latency Cycle Selection based on transaction opcodes ….. 1111 = 15 Latency Cycles Selection based on transaction opcodes Dependency: N/A

WRITE MODE(1S-1S-1S)

WRITE TO SET THE BIT[6] & BIT[5]OF CFR 2 TO ENABLE QPI AND MULTIPLEX BIT FOR DATA AND RESET



READ MODE (4S-4S-4S)

ITS NOT ABLE TO DETECT