AN217010

Migrating from S25FL164K Serial NOR Flash to S25FL064L Serial NOR Flash

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Related Application Notes: None

AN217010 provides guidelines for migrating from Cypress's S25FL164K serial NOR Flash to the S25FL064L serial NOR Flash family of products. It describes the similarities and differences in specifications between them to facilitate this conversion.

Contents

1 Introduction

This document provides guidelines for migrating from Cypress's S25FL164K Serial NOR Flash to the S25FL064L Serial NOR Flash family of products. It discusses the known differences that may be encountered when facilitating this conversion.

The S25FL164K is a 3.0-V, single-supply flash memory device based on 90-nm floating gate technology. The S25FL064L is also a 3.0-V, single-supply flash memory device, but it is based on an advanced 65-nm floating gate process technology. The S25FL064L flash offers additional features such as extended 4-byte addressing, array protection, individual and regional protection, read/write any register, Double Data Rate (DDR), and Quad Peripheral Interface (QPI). Refer to the S25FL064L datasheet for a full description of all new features and functions.

2 Feature Comparison

The S25FL064L supports a superset of the S25FL164K feature set. Table 1 summarizes the feature similarities and differences, which are discussed in detail in later sections.

Table 1. Feature Comparison

Feature/Parameter	S25FL064L	S25FL164K
Technology Node	65-nm NOR Flash	90-nm NOR Flash
Architecture	Floating Gate	Floating Gate
Density	64 Mb	64 Mb
Bus Width	x1, x2, x4	x1, x2, x4
Supply Voltage	2.7 V–3.6 V	2.7 V–3.6 V
Normal Read Speed (SIO)	6.25 MBps (50 MHz)	6.25 MBps (50 MHz)
Fast Read Speed (SIO)	13.5 MBps (108 MHz)	13.5 MBps (108 MHz)
Dual Read Speed (DIO)	27 MBps (108 MHz)	27 MBps (108 MHz)
Quad Read Speed (QIO)	52 MBps (108 MHz)	52 MBps (108 MHz)
Quad Read Speed (QIO-DDR)	54 MBps (54 MHz)	–
Program Buffer Size	256 Bytes	256 Bytes
Erase Sector/Block Size	4 KB/32 KB/64 KB	4 KB/64 KB
Parameter Sector Size	–	4 KB
Security Registers	Four 256 Byte	Three 256 Byte
Data Protection	Legacy Block Individual Block Lock Pointer Region	Legacy Block Pointer Region
Suspend/Resume	Erase/Program	Erase/Program
Addressing	3/4 Byte + Bank	3 Byte
Hardware Reset	Yes	No
Operating Temperature	–40 °C to +85 °C	–40 °C to +85 °C
	–40 °C to +105 °C	–40 °C to +105 °C
	–40 °C to +125 °C	No
Deep Power Down	Yes – 2 µA (typical)	Yes – 2 µA (typical)
ID and SFDP Interface	Yes	Yes
Packages	8-lead SOIC (208 mils)	8-lead SOIC (208 mils)
	USON (4x4 mm)	8-Contact WSON (5x6 mm)
	24-Ball FBGA (6x8 mm)	24-Ball FBGA (6x8 mm)
	-	16-lead SOIC (300 mil)

3 Command Set Comparison

Table 2 summarizes the supported commands for each device. Pertinent differences will be discussed in subsequent sections.

Table 2. Command Set Comparison

Function	Command	Description	S25FL064L	S25FL164K
Read Device ID	RDID	Read ID (JEDEC Manufacturer ID)	9Fh	9Fh
	RSFDP	Read JEDEC Serial Flash Discoverable Parameters	5Ah	5Ah
	RDQID	Read Quad ID	AFh	–
	RUID	Read Unique ID	4Bh	5Ah
	READ_ID	Read Manufacturer and Device Identification	–	90h
Register Access	RDSR1	Read Status Register 1	05h	05h
	RDSR2	Read Status Register 2	07h	–
	RDCR1/RDSR2	Read Configuration Register 1/Status Register 2	35h	35h
	RDCR2	Read Configuration Register 2	15h	-–
	RDCR3/RDSR3	Read Configuration Register 3/Status Register 3	33h	33h
	RDAR	Read Any Register	65h	–
	WRR	Write Register (Status-1 and Conf-1,2,3) / (Status – 1,2,3)	01h	01h
	WRDI	Write Disable	04h	04h
	WREN	Write Enable for Nonvolatile Data Change	06h	06h
	WRENV	Write Enable for Volatile Status and Configuration Registers	50h	50h
	WRAR	Write Any Register	71h	–
	CLSR	Clear Status Register	30h	–
	4BEN	Enter 4-Byte Address Mode	B7h	–
	4BEX	Exit 4-Byte Address Mode	E9h	–
	SBL	Set Burst Length	77h	77h
	QPIEN	Enter QPI	38h	–
	QPIEX	Exit QPI	F5h	–
	DLPRD	Data Learning Pattern Read	41h	–
	PDLRNV	Program NV Data Learning Register	43h	–
	WDLRV	Write Volatile Data Learning Register	4Ah	–
Read Flash Array	READ	Read	03h	03h
	4READ	Read (4-Byte Address)	13h	–
	FAST_READ	Fast Read	0Bh	0Bh
	4FAST_READ	Fast Read (4-Byte Address)	0Ch	–
	DOR	Dual Output Read	3Bh	3Bh
	4DOR	Dual Output Read (4-Byte Address)	3Ch	–
	QOR	Quad Output Read	6Bh	6Bh
	4QOR	Quad Output Read (4-Byte Address)	6Ch	–
	DIOR	Dual I/O Read	BBh	BBh

Function	Command	Description	S25FL064L	S25FL164K
	4DIOR	Dual I/O Read (4-Byte Address)	BCh	–
	QIOR	Quad I/O Read	EBh	EBh
	4QIOR	Quad I/O Read (4-Byte Address)	ECh	–
	DDRQIOR	DDR Quad I/O Read	EDh	–
	4DDRQIOR	DDR Quad I/O Read (4-Byte Address)	EEh	–
Program Flash Array	PP	Page Program	02h	02h
	4PP	Page Program (4-Byte Address)	12h	–
	QPP	Quad Page Program	32h	–
	4QPP	Quad Page Program (4-Byte Address)	34h	–
Erase Flash Array	SE	Sector Erase	20h	20h
	4SE	Sector Erase (4-Byte Address)	21h	–
	HBE	Half Block Erase	52h	–
	4HBE	Half Block Erase (4-Byte Address)	53h	–
	BE	Block Erase	D8h	D8h
	4BE	Block Erase (4-Byte Address)	DCh	–
	CE	Chip Erase/Bulk Erase	60h	60h
	CE	Chip Erase/Bulk Erase (alternate instruction)	C7h	C7h
Erase/Program Suspend/Resume	EPS	Erase/Program Suspend	75h	75h
	EPR	Erase/Program Resume	7Ah	7Ah
Security Region Array	SECRE	Security Region Erase	44h	44h
	SECRP	Security Region Program	42h	42h
	SECRR	Security Region Read	48h	48h
Array Protection	IBLRD	IBL Read	3Dh	–
	4IBLRD	IBL Read (4-Byte Address)	E0h	–
	IBL	IBL Lock	36h	–
	4IBL	IBL Lock (4-Byte Address)	E1h	–
	IBUL	IBL Unlock	39h	–
	4IBUL	IBL Unlock (4-Byte Address)	E2h	–
	GBL	Global IBL Lock	7Eh	–
	GBUL	Global IBL Unlock	98h	–
	SPRP	Set Pointer Region Protection	FBh	39h
	4SPRP	Set Pointer Region Protection (4-Byte Address)	E3h	–
Individual and Region Protection	IRPRD	IRP Register Read	2Bh	–
	IRPP	IRP Register Program	2Fh	–
	PRRD	Protection Register Read	A7h	–
	PRL	Protection Register Lock (NVLOCK Bit Write)	A6h	–
	PASSRD	Password Read	E7h	–
	PASSP	Password Program	E8h	–

Function	Command	Description	S25FL064L	S25FL164K
	PASSU	Password Unlock	EAh	–
Reset	RSTEN	Software Reset Enable	66h	66h
	RST	Software Reset	99h	99h
	MBR	Mode Bit Reset	FFh	FFh
Deep Power Down	DPD	Deep Power Down	B9h	B9h
	RES	Release from Deep Power Down/Device ID	ABh	ABh

The primary areas of concern when migrating from S25FL164K to S25FL064L are AC/DC specification differences and package/pinout differences. S25FL064L offers additional features such as extended 4-byte addressing, array protection, individual and region protection, read/write any register, DDR, and QPI.

3.1 Device Identification

In S25FL164K, the Manufacturer/Device ID (90h) command outputs one byte of manufacturer's identification, followed by one byte of device identification. Table 3 provides the byte sequence showing the Manufacturer and Device ID values output by the command. The S25F064L does not have a Manufacturer/Device ID command.

Table 3. S25FL164K Manufacturer/Device ID Command Byte Sequence

Device	Command	Dummy	Dummy	00h	Manufacturer	Device ID
	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6
S25FL164K	90h	XXh	XXh	00h	01	16h

The JEDEC ID (9Fh) command for S25FL164K, called the "RDID (9Fh) command" for S25FL064L, outputs one byte of manufacturer identification followed by two bytes of device identification Table 4 provides the byte sequence, showing the identification values output by the command.

Table 4. S25FL164K and S25FL064L JEDEC ID Command Byte Sequence

Device	Command	Manufacturer	Device ID	Capacity
	Byte 1	Byte 2	Byte 3	Byte 4
S25FL164K	9Fh	01h	40h	17h
S25FL064L	9Fh	01h	60h	17h

Serial Flash Discoverable Parameters (SFDP) are provided in both devices and are accessed by the 5Ah command (Read SFDP Register/Read Unique ID Number for the S25FL164K; RSFDP for the S25FL064L). SFDP, which is address-based, is defined in the JEDEC-216B specification and consists of a header table that identifies the SFDP. See Table 5 for the SFDP address/byte sequences. For details on the SFDP data format, consult the datasheets.

Table 5. SFDP Header and Parameter Address Map

Device	SFDP Header			SFDP Parameters		
	Address Start	–	Address End	Address Start	–	Address End
S25FL164K	0000h	–	007Fh	0080h	–	00BFh
S25FL064L	0000h	–	02FFh	0300h	–	05FFh

3.2 Unique Identification

The Unique ID provides a 64-bit unique number for each device. In S25FL164K, the unique ID number can be read by the RSFDP command (5Ah) with address F8h to FFh. S25FL064L provides a dedicated RUID command (4Bh). The address map for unique identification for both devices is shown in Table 6 and Table 7.

Table 6. S25FL164K Unique ID Address Map

Device	UID		
	Address F8h	–	Address FFh
S25FL164K	UID_Byte0	–	UID_Byte7

Table 7. S25FL064L Unique ID Address Map

Device	UID			Additional UID Bytes		
	Address 00h	–	Address 07h	Address 08h	–	Address 0Fh
S25FL064L	UID_Byte0	–	UID_Byte7	UID_Byte8	–	UID_Byte15

3.3 Extended Addressing

S25FL164K uses a 3-byte (24-bit) address to access up to 16 MB of flash address space. Since the 64-MB density for the S25FL164K translates to 8 MB of flash address space, the 3-byte addressing scheme is sufficient. However, to accommodate densities above 16 MB for multi-chip packages, the S25FL064L supports additional addressing options, which are listed in the next two sections.

3.3.1 Extended Addressing with Legacy Instructions

S25FL064L provides a configuration bit, which when enabled, changes all 3-byte address commands to 4-byte address commands. Table 8 lists all of the legacy commands requiring 4-byte addressing when the address configuration bit is set to CR2NV[1]=ADP_NV=1 or CR2V[1]=ADP=1.

Table 8. Legacy Commands Requiring 4-Byte Addressing after POR when CR2NV[1]=ADP_NV Is Set

Function	Command	Description	S25FL064L
Read Device ID	RSFDP	Read JEDEC Serial Flash Discoverable Parameters	5Ah
Register Access	RDAR	Read Any Register	65h
	WRAR	Write Any Register	71h
Read Flash Array	READ	Read	03h
	FAST_READ	Fast Read	0Bh
	DOR	Dual Output Read	3Bh
	QOR	Quad Output Read	6Bh
	DIOR	Dual I/O Read	BBh
	QIOR	Quad I/O Read	EBh
	DDRQIOR	DDR Quad I/O Read	EDh
Program Flash Array	PP	Page Program	02h
	QPP	Quad Page Program	32h
Erase Flash Array	SE	Sector Erase	20h
	HBE	Half Block Erase	52h
	BE	Block Erase	D8h

Function	Command	Description	S25FL064L
Security Region Array	SECRE	Security Region Erase	44h
	SECRP	Security Region Program	42h
	SECRR	Security Region Read	48h
Array Protection	IBLRD	IBL Read	3Dh
	IBL	IBL Lock	36h
	IBUL	IBL Unlock	39h
	SPRP	Set Pointer Region Protection	FBh

3.3.2 Extended Addressing with New 4-Byte Instructions

The S25FL064L has new instructions that always require 4-byte addresses. Table 9 lists all of the 4-byte commands.

Table 9. New Commands Requiring 4-Byte Addressing

Function	Command	Description	S25FL064L
Read Flash Array	4READ	Read (4-Byte Address)	13h
	4FAST_READ	Fast Read (4-Byte Address)	0Ch
	4DOR	Dual Output Read (4-Byte Address)	3Ch
	4QOR	Quad Output Read (4-Byte Address)	6Ch
	4DIOR	Dual I/O Read (4-Byte Address)	BCh
	4QIOR	Quad I/O Read (4-Byte Address)	ECh
	4DDRQIOR	DDR Quad I/O Read (4-Byte Address)	EEh
Program Flash Array	4PP	Page Program (4-Byte Address)	12h
	4QPP	Quad Page Program (4-Byte Address)	34h
Erase Flash Array	4SE	Sector Erase (4-Byte Address)	21h
	4HBE	Half Block Erase (4-Byte Address)	53h
	4BE	Block Erase (4-Byte Address)	DCh
Array Protection	4IBLRD	IBL Read (4-Byte Address)	E0h
	4IBL	IBL Lock (4-Byte Address)	E1h
	4IBUL	IBL Unlock (4-Byte Address)	E2h
	4SPRP	Set Pointer Region Protection (4-Byte Address)	E3h

3.4 Status and Configuration Registers

The initial power-up and post-power-up configuration of the S25FL164K and S25FL064L devices is determined by configuration bits stored in the internal configuration registers. The status registers, in addition to storing some configuration bits, also provide the status for embedded operations. Table 10 summarizes the supported registers for each device.

Table 10. Register Set Comparison/Matching

S25FL064L Registers	S25FL164K Registers
Status Register 1	Status Register 1
Status Register 2	
Configuration Register 1	Status Register 2
Configuration Register 2	
Configuration Register 3	Status Register 3
Individual and Region Protection Register	
Password Register	
Individual Block Lock Access Register	
Pointer Region Protection Register	
DDR Data Learning Register	

For the type and functionality of each configuration/status bit, consult each device's respective datasheet.

3.5 Deep Power-Down Mode

S25FL164K and S25FL064L both support Deep Power-Down modes. The same command can be used to read the device's electronic identification (ID) number.

3.6 Security Regions/Security Registers

Both the S25FL164K and S25FL064L support security regions consisting of four 256-byte regions, separately addressable from the main flash memory array. S25F164K Region 0 is used by Cypress to store and protect the SFDP information. The security regions that are not used for SFDP can be erased, programmed, and protected individually. Table 11 shows the address space regions for both devices.

Table 11. Secure Region Definitions

Security Region	Address (S25FL164K)	Address (S25FL064L)
0 (SFDP for S25FL164K)	0000h – 00FFh	0000h – 00FFh
1	1000h – 10FFh	0100h – 01FFh
2	2000h – 20FFh	0200h – 02FFh
3	3000h – 30FFh	0300h – 03FFh

3.7 Double Data Rate (DDR) Read Commands

The S25FL064L supports the DDR Quad I/O Read command. A 4-byte address version of this command is also available. The S25FL164K does not support any DDR Read commands.

3.8 Data Protection

The S25FL164K and S25FL064L flash devices implement data protection schemes that shield program and erase operations. Table 12 shows the data protection schemes supported in each device. For more details on the protection schemes, consult the respective device datasheets.

Table 12. Data Protection Schemes Supported

Device Type	Block Protection	Individual Block Lock Protection	Pointer Protection	Region Protection
S25FL164K	Yes	–	Yes	Yes
S25FL064L	Yes	Yes	Yes	Yes

3.9 Erase and Program Suspend/Resume Operations

S25FL164K and S25FL064L support program and erase suspend and resume commands, which allow program and erase operations to be individually suspended (EPS:75h) and resumed (EPR: 7Ah) to access data in blocks that are not being modified. For S25FL064L, Status Register 2 is added to allow the host software to determine if a particular operation is in suspension. Also, the Read Status Register 2 (RDSR2:07h) command has been added to access this new register.

4 Hardware Comparison

Pertinent hardware differences are discussed in the subsequent sections.

4.1 HOLD Functionality

S25FL164K supports serial communications hold (stop) through the HOLD# pin. HOLD# is a multiplexed pin used during quad communication as IO3. S25FL064L does not support hold functionality. Instead, HOLD# is replaced by RESET# and acts like a hardware reset when CS# is HIGH. RESET# is again multiplexed with IO3 for Quad mode.

4.2 Software Reset

S25FL164K and S25FL064L support the Software Rest command (RSTEN:66h, RESET:99h), which restores the device to its initial power-up state.

4.3 DC Parameters

Table 13 compares the DC parameters of S25FL164K and S25FL064L. While most parameter differences should not cause performance issues when migrating, it is highly recommended that you carefully review all the parameter differences for any potential impact.

Table 13. DC Parameter Comparison

Symbol	Parameter Operating Temperature Range –40°C to +105°C	S25FL064L			S25FL164K			Units
		Min	Typical	Max	Min	Typical	Max	
V_{DD}	Supply Voltage	2.7	3	3.6	2.7	3	3.6	V
V_{DD} (min)	V_{DD} (minimum operation voltage)	2.7			2.7			V
V_{DD} (cutoff)	V_{DD} (cutoff where reinitialization is needed)	2.4			2.4			V
V_{DD} (low)	V_{DD} (low voltage for initialization to occur)	1			1			V
V_{IL}	Input Low Voltage	–0.5		0.3 x V_{DD}	–0.5		0.3 x V_{DD}	V
V_{IH}	Input High Voltage	0.7 x V_{DD}		V_{DD} + 0.4	0.7 x V_{DD}		V_{DD} +0.4	V
V_{OL}	Output Low Voltage			0.2			0.2	V
V_{OH}	Output High Voltage	V_{DD} – 0.2			V_{DD} – 0.2			V
I_{LI}	Input Leakage Current			±4			±2	µA
I_{LO}	Output Leakage Current			±4			±2	µA
I_{CC1}	Active Power Supply Current (READ) – Serial SDR		25	35		9	13.5	mA
	Active Power Supply Current (READ) – Serial DDR		30	35				mA
I_{CC2}	Active Power Supply Current (Page Program)		40	50		20	25	mA
I_{CC3}	Active Power Supply Current (WRR or WRAR)		40	50		8	12	mA
I_{CC4}	Active Power Supply Current (SE)		40	50		20	25	mA
I_{CC5}	Active Power Supply Current (HBE, BE)		40	50		20	25	mA
I_{SB}	Standby Current		20	40		15	25	µA
I_{DPD}	Deep Power-Down Current		2	20		2	8	µA
I_{POR}	Power-On Reset Current		15	20				mA

4.4 Single Data Rate (SDR) AC Parameters

Table 14 compares the AC parameters of S25FL164K and S25FL064L. While most parameter differences should not cause performance issues when migrating, it is highly recommended that you carefully review all the parameter differences for any potential impact.

Table 14. SDR AC Parameter Comparison

Symbol	Parameter Operating Temperature Range –40°C to +105°C	S25FL064L			S25FL164K			Units
		Min	Typ	Max	Min	Typ	Max	
f_{SCK} - 1	SCK Clock Frequency for dual and quad commands			108			108	MHz
f_{SCK} - 2	SCK Clock Frequency for READ and 4READ instructions			50			50	MHz
P_{SCK}	SCK Clock Period	1/ f_{SCK}			9.25			
t_{WH}, t_{CH}	Clock High Time	50% P_{SCK} -5%			3.3			ns
t_{WL}, t_{CL}	Clock Low Time	50% P_{SCK} -5%			4.3			ns
t_{CRT}, t_{CLCH}	Clock Rise Time (slew rate)	0.1			0.1			V/ns
t_{CFT}, t_{CHCL}	Clock Fall Time (slew rate)	0.1			0.1			V/ns
t_{CS}	CS# High Time (any Read instructions)	20			7			ns
	CS# High Time (all other non-Read instructions)	50			40			ns
t_{CSS}	CS# Active Setup Time (relative to SCK)	3			5			ns
t_{CSH}	CS# Active Hold Time (relative to SCK)	5			5			ns
t_{SU}	Data in Setup Time	3			2			ns
t_{HD}	Data in Hold Time	2			5			ns
t_V	Clock Low to Output Valid			8			7	ns
t_{HO}	Output Hold Time	1			2			ns
t_{DIS}	Output Disable Time			8			7	ns
t_{WPS}	WP# Setup Time	20			20			ns
t_{WPH}	WP# Hold Time	100			100			ns
t_{DP}	CS# High to Deep Power-Down Mode			3			3	µs
t_{RES}	CS# High to Release from Deep Power-Down Mode			5			3	µs
t_{QEN}	QIO or QPI Enter mode, time needed to issue next command			1.5				µs
t_{QEXN}	QIO or QPI Exit mode, time needed to issue next command			1				µs

4.5 Embedded Algorithm Performance

Table 15 compares the embedded algorithm performance parameters of S25FL164K and S25FL064L. While most parameter differences should not cause performance issues when migrating, it is highly recommended that you carefully review all the parameter differences for any potential impact.

Table 15. Embedded Algorithm Performance Parameter Comparison

Symbol	Parameter Operating Temperature Range –40°C to +105°C	S25FL064L			S25FL164K			Units
		Min	Typical	Max	Min	Typical	Max	
t_W	Nonvolatile Register Write Time		220	1200		2	85	ms
t_{PP}	Page Programming (256 bytes)		450	1350		700	3000	µs
t_{BP1}	Byte Programming (first byte)		75	90		15	50	µs
t_{BP2}	Additional Byte Programming (after first byte)		10	30		2.5	12	µs
t_{SE}	Sector Erase Time (4-KB physical sectors)		65	270		50	450	ms
t_{HBE}	Half Block Erase Time (32-KB physical sectors)		300	600				ms
t_{BE}	Block Erase Time (64-KB physical sectors)		450	1150		500	2000	ms
t_{CE}	Chip Erase Time		55	150		64	256	s

5 Summary

Migration from S25FL164K to S25FL064L is straightforward and requires minimal accommodation with regard to either system software or hardware. After the accommodations are done, if required, the S25FL064L flash can enable the use of higher density devices with greater performance in existing systems and additional features of extended 4-byte addressing, array protection, individual and region protection, read/write any register, DDR, and QPI.

6 Related Documents

Table 16. Cypress SPI NOR Flash Product Datasheets

Product Family	Spec. Number	Title
FL1-K Family	002-00497	S25FL116K, S25FL132K, S25FL164K 16 Mbit (2 Mbyte), 32 Mbit (4 Mbyte), 64 Mbit (8 Mbyte) 3.0V SPI Flash Memory
FL-L Family	002-12878	S25FL064L Flash Datasheet – 64-Mbit (8-Mbyte) 3.0 V FL-L SPI Flash Memory

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