Table 9-4: SMC_GSTAT Register Fields (Continued)

Bit No. (Access)	Bit Name	Description/Enumeration	
1 (R/NW)	BRQSTAT	Bus Request Status. The SMC_GSTAT.BRQSTAT bit indicates the $\overline{\text{SMC\_BR}}$ pin status. This pin is active when the bus is requested for a transaction.	
		0	Inactive BR
		1	Active BR (bus requested)
0 (R/NW)	BGSTAT	Bus Grant Status. The SMC_GSTAT.BGSTAT bit indicates the $\overline{\text{SMC\_BG}}$ pin status. This pin is active when bus is granted for a transaction.	
		0	Inactive BG
		1	Active BG (bus granted)

Bank 0 Control Register

The SMC_B0CTL register enables bank 0 accesses and configures the memory access features for this bank.

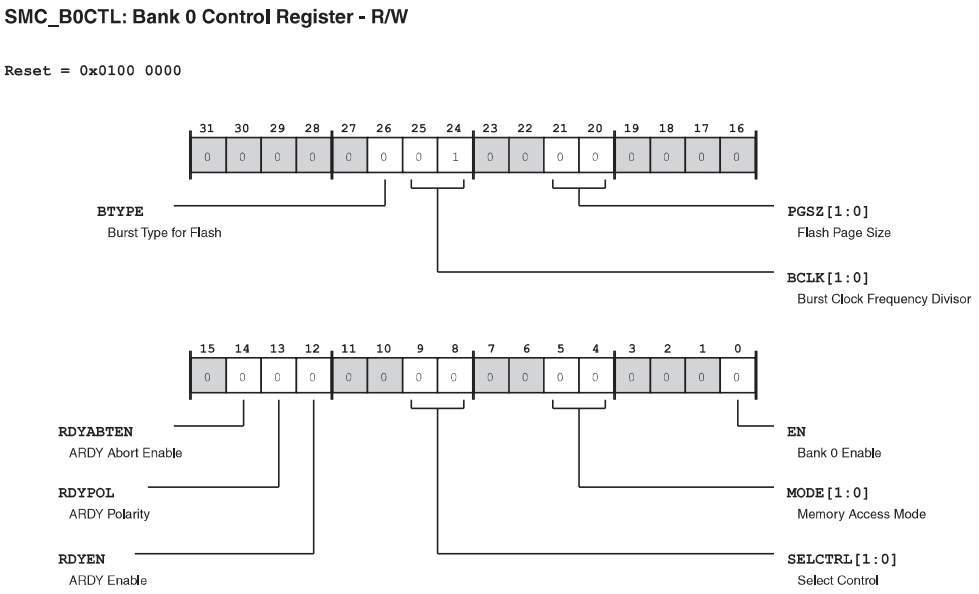

Figure 9-16: SMC_B0CTL Register Diagram

Table 9-5: SMC_B0CTL Register Fields

Bit No. (Access)	Bit Name	Description/Enumeration	
26 (R/W)	BTYPE	Burst Type for Flash. The SMC_BOCTL.BTYPE bit selects the burst type that the SMC uses for accesses using sync burst flash protocol.	
		0	Wrap
		1	Sequential
25:24 (R/W)	BCLK	Burst Clock Frequency Divisor. The SMC_BOCTL.BCLK bits select the divisor that the SMC uses to determine the clock frequency for accesses using sync burst flash protocol.	
		0	Burst clock = SCLK ÷ 1
		1	Burst clock = SCLK ÷ 2
		2	Burst clock = SCLK ÷ 3
		3	Burst clock = SCLK ÷ 4
21:20 (R/W)	PGSZ	Flash Page Size. The SMC_BOCTL.PGSZ bits select the flash page size, if page flash or sync burst flash protocol has been enabled (SMC_BOCTL.MODE> 1). Note that the SMC_BOCTL.PGSZ bits must be set to match the flash protocol of the external flash memory device in the system. The typical SMC_BOCTL.PGSZ selection for external devices supporting async flash or async flash page protocols is 4 or 8 words. The typical SMC_BOCTL.PGSZ selection for external devices supporting sync burst flash protocol is 16 words.	
		0	4 words
		1	8 words
		2	16 words
		3	16 words

Table 9-5: SMC_B0CTL Register Fields (Continued)

Bit No. (Access)	Bit Name	Description/Enumeration	
14 (R/W)	RDYABTEN	ARDY Abort Enable. The SMC_BOCTL.RDYABTEN bit enables the abort counter for the SMC_ARDY pin, if enabled (SMC_BOCTL.RDYEN =1). After SMC_BOTIM.RAT or SMC_BOTIM.WAT cycles, the SMC starts sampling the SMC_ARDY pin and starts the abort down counter (if enabled). The abort count is 64 cycles of SCLK. If the SMC detects that SMC_ARDY remains de-asserted when the counter expires, the SMC aborts the access and returns an error response back on the system bus.	
		0	Disable abort counter
		1	Enable abort counter
13 (R/W)	RDYPOL	ARDY Polarity. The SMC_BOCTL.RDYPOL bit selects the polarity (active high or low) for the SMC_ARDY pin, if enabled (SMC_BOCTL.RDYEN =1). When the SMC samples the SMC_ARDY pin in the selective active state, the transaction completes.	
		0	Low active ARDY
		1	High active ARDY
12 (R/W)	RDYEN	ARDY Enable. The SMC_BOCTL.RDYEN bit enables SMC_ARDY pin operation for bank 0 accesses. When enabled, the SMC uses SMC_ARDY (after the access time countdown) to determine completion of access to this memory bank. When disabled, the SMC ignores SMC_ARDY for accesses to this memory bank.	
		0	Disable ARDY
		1	Enable ARDY
9:8 (R/W)	SELCTRL	Select Control. The SMC_BOCTL.SELCTRL bits select the handling of the $\overline{\text{SMC\_AMSn}}$, $\overline{\text{SMC\_ARE}}$, $\overline{\text{SMC\_AOE}}$, and $\overline{\text{SMC\_AWE}}$ pins for memory access control.	
		0	AMS0 only
		1	AMS0 ored with ARE
		2	AMS0 ored with AOE
		3	AMS0 ored with AWE

Table 9-5: SMC_B0CTL Register Fields (Continued)

Bit No. (Access)	Bit Name	Description/Enumeration	
5:4 (R/W)	MODE	Memory Access Mode. The SMC_BOCTL.MODE bits select the protocol the SMC uses for static memory read/write access. Note that the write protocol for async flash, async flash page, and sync burst flash are all similar; only the read protocols differ for these modes.	
		0	Async SRAM protocol
		1	Async flash protocol
		2	Async flash page protocol
		3	Sync burst flash protocol
0 (R/W)	EN	Bank 0 Enable. The SMC_BOCTL.EN bit enables accesses to the memory in bank 0. When this bit is disabled, accesses to bank 0 return an error response.	
		0	Disable access
		1	Enable access

Bank 0 Timing Register

The SMC_BOTIM register configures bank 0 read and write access, setup, and hold timing for this bank. Note that read and write timing configurations are independent and may differ.

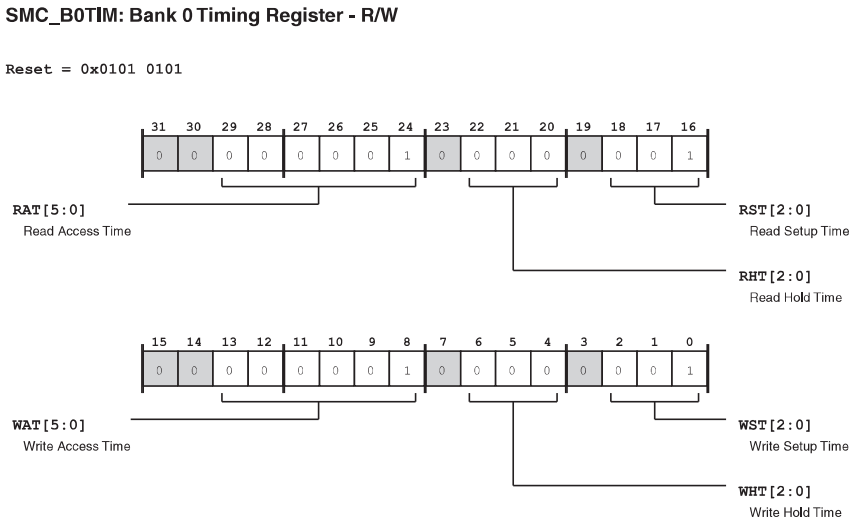

Figure 9-17: SMC_B0TIM Register Diagram

Table 9-6: SMC_B0TIM Register Fields

Bit No. (Access)	Bit Name	Description/Enumeration	
29:24 (R/W)	RAT	Read Access Time. The SMC_B0TIM.RAT bits select the access time (in SCLK cycles) that the SMC asserts the SMC_ARE pin for a read access. The access time is from 1 to 63 SCLK cycles.	
		0	Not supported
		1	1 SCLK clock cycle
		63	63 SCLK clock cycles
22:20 (R/W)	RHT	Read Hold Time. The SMC_B0TIM.RHT bits select the hold time (in SCLK cycles) that the SMC waits after de-asserting the SMC_ARE pin before asserting the SMC_AOE pin for the next access. The hold time is from 0 to 7 SCLK cycles.	
		0	0 SCLK clock cycles
		1	1 SCLK clock cycle
		7	7 SCLK clock cycles
18:16 (R/W)	RST	Read Setup Time. The SMC_B0TIM.RST bits select the setup time (in SCLK cycles) that the SMC asserts the SMC_AOE pin before asserting the SMC_ARE pin for an access. The setup time is from 1 to 8 SCLK cycles.	
		0	8 SCLK clock cycles
		1	1 SCLK clock cycle
		7	7 SCLK clock cycles
13:8 (R/W)	WAT	Write Access Time. The SMC_B0TIM.WAT bits select the access time (in SCLK cycles) that the SMC asserts the SMC_AWE pin for a write access. The access time is from 1 to 63 SCLK cycles.	
		0	Not supported
		1	1 SCLK clock cycle
		63	63 SCLK clock cycles

Table 9-6: SMC_B0TIM Register Fields (Continued)

Bit No. (Access)	Bit Name	Description/Enumeration	
6:4 (R/W)	WHT	Write Hold Time. The SMC_B0TIM.WHT bits select the hold time (in SCLK cycles) that the SMC waits after de-asserting the SMC_AWE pin before de-asserting the SMC_AOE pin for the current access. The hold time is from 0 to 7 SCLK cycles.	
		0	0 SCLK clock cycles
		1	1 SCLK clock cycle
		7	7 SCLK clock cycles
2:0 (R/W)	WST	Write Setup Time. The SMC_B0TIM.WST bits select the setup time (in SCLK cycles) that the SMC asserts the SMC_AOE pin before asserting the SMC_AWE pin for a write access. The setup time is from 1 to 8 SCLK cycles.	
		0	8 SCLK clock cycles
		1	1 SCLK clock cycle
		7	7 SCLK clock cycles

Bank 0 Extended Timing Register

The SMC_B0ETIM register configures extensions to access times and idle times, augmenting the setup, hold, and access times configured with the SMC_B0TIM register.

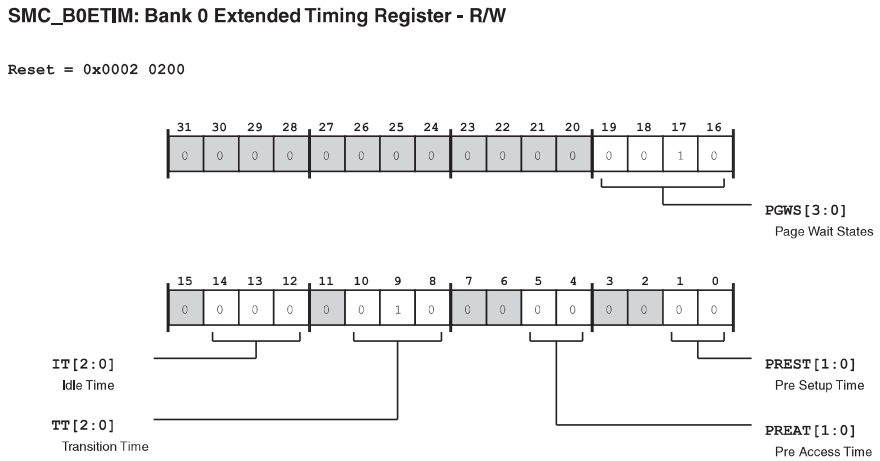

Figure 9-18: SMC_B0ETIM Register Diagram

Table 9-7: SMC_B0ETIM Register Fields

Bit No. (Access)	Bit Name	Description/Enumeration	
19:16 (R/W)	PGWS	Page Wait States. The SMC_BOETIM.PGWS bits select a page access extension time (in SCLK cycles) that the SMC waits during read accesses when configured for flash page protocol (SMC_BOCTL.MODE =2). The wait time is from 1 to 15 SCLK cycles.	
		0	Not supported
		1	1 SCLK clock cycles
		15	15 SCLK clock cycles
14:12 (R/W)	IT	Idle Time. The SMC_BOETIM.IT bits select a bus idle time (in SCLK cycles) that the SMC waits between de-asserting the $\overline{\text{SMC\_AMSn}}$ pin and asserting the $\overline{\text{SMC\_AMSn}}$ pin for the next access. Note that the SMC_BOETIM.IT period may be extended using the SMC_BOETIM.TT selection. The idle time is from 0 to 7 SCLK cycles.	
		0	0 SCLK clock cycles
		7	7 SCLK clock cycles
10:8 (R/W)	TT	Transition Time. The SMC_BOETIM.TT bits select a bus idle time (in SCLK cycles) that the SMC extends the SMC_BOETIM.IT to allow for the subsequent access either using a different transfer direction or accessing a different bank. The transition time is from 1 to 7 SCLK cycles.	
		0	No bank transition
		1	1 SCLK clock cycle
		7	7 SCLK clock cycles
5:4 (R/W)	PREAT	Pre Access Time. The SMC_BOETIM.PREAT bits select the pre-access time (in SCLK cycles) that the SMC waits after de-asserting the $\overline{\text{SMC\_AOE}}$/$\overline{\text{ADV}}$ pin before asserting the $\overline{\text{SMC\_ARE}}$/$\overline{\text{SMC\_AWE}}$ pin for the current access. The pre-access time is from 0 to 3 SCLK cycles.	
		0	0 SCLK clock cycles
		3	3 SCLK clock cycles

Table 9-7: SMC_B0ETIM Register Fields (Continued)

Bit No. (Access)	Bit Name	Description/Enumeration	
1:0 (R/W)	PREST	Pre Setup Time. The SMC_B0ETIM.PREST bits select the pre-setup time (in SCLK cycles) that the SMC asserts the SMC_AMSn pin before asserting the SMC_AOE/ADV pin for an access. The pre-setup time is from 0 to 3 SCLK cycles.	
		0	0 SCLK clock cycles
		3	3 SCLK clock cycles

Bank 1 Control Register

The SMC_B1CTL register enables bank 1 accesses and configures the memory access features for this bank.

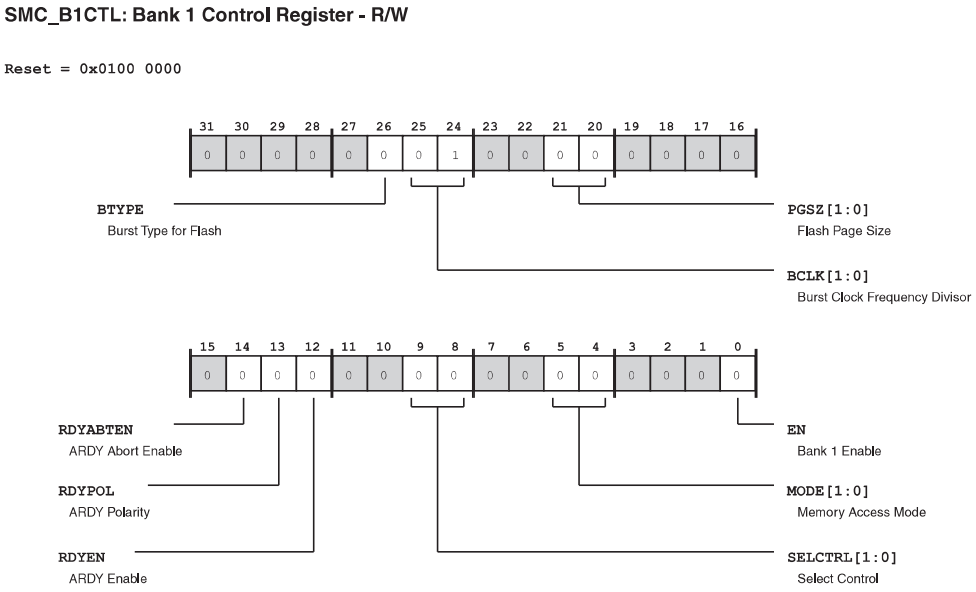

Figure 9-19: SMC_B1CTL Register Diagram