Xccela™ Flash Memory Data Sheet Brief

MT35X 1.8/3V, Octal I/O, 4KB/32KB/128KB Sector Erase

Features

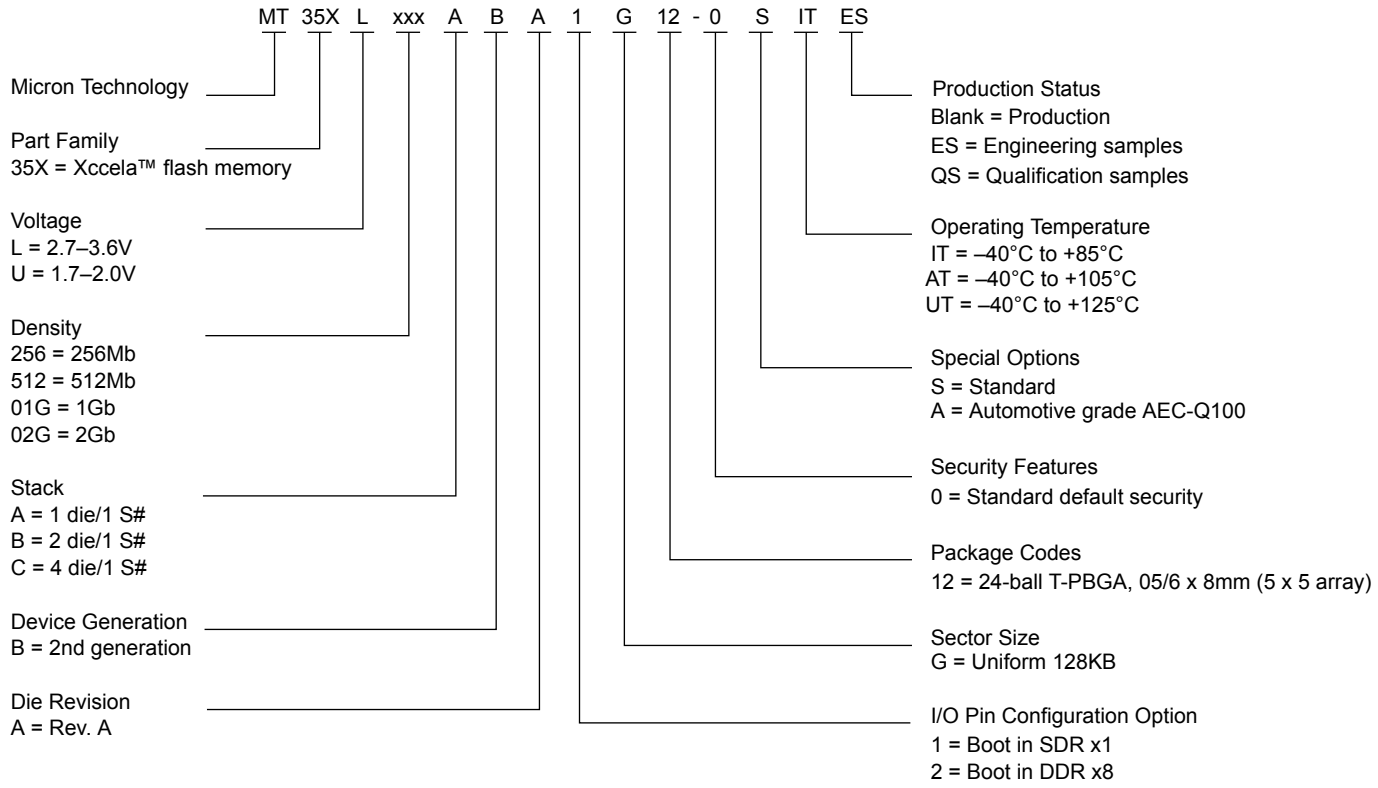
- SPI-compatible Xccela™ bus interface
  - Octal DDR protocol
  - Extended-SPI protocol with octal commands
- Single and double transfer rate (SDR/DDR)
- Clock frequency:
  - 166 MHz (MAX) in SDR (166 MB/s) (1.8V)
  - 200 MHz (MAX) in DDR (400 MB/s) with DQS (1.8V)
  - 133 MHz (MAX) in SDR (133 MB/s) (3.0V)
  - 133 MHz (MAX) in DDR (266MB/s) with DQS (3.0V)
- Execute-in-place (XIP)
- PROGRAM/ERASE SUSPEND operations
- Volatile and nonvolatile configuration settings
- Software reset
- Reset pin available
- 3-byte and 4-byte address modes – enable memory access beyond 128Mb
- Dedicated 64-byte OTP area outside main memory
  - Readable and user-lockable
  - Permanent lock with PROGRAM OTP command
- Erase capability
  - Bulk erase for monolithic, die erase for stacked devices
  - Sector erase 128KB uniform granularity
  - Subsector erase 4KB, 32KB granularity
- Security and write protection
  - Volatile and nonvolatile locking and software write protection for each 128KB sector
  - Nonvolatile configuration locking and password protection
  - Protection management register offering enhanced security features
  - Hardware write protection: nonvolatile bits (BP[3:0] and TB) define protected area size
  - Program/erase protection during power-up
  - CRC detects accidental changes to raw data
- Electronic signature
  - JEDEC-standard 3-byte signature
  - Extended device ID: two additional bytes identify device factory options
- JESD47I-compliant
  - Minimum 100,000 ERASE cycles per sector
  - Data retention: 20 years (TYP)

Options	Marking
• Voltage	
– 1.7–2.0V	U
– 2.7–3.6V	L
• Density	
– 256Mb	256
– 512Mb	512
– 1Gb	01G
– 2Gb	02G
• Device stacking	
– Monolithic	A
– 2 die stacked	B
– 4 die stacked	C
• Device Generation	B
• Die revision	A
• Configuration	
– Boot in SDR x1	1
– Boot in DDR x8	2
• Sector Size	
– 128KB	G
• Packages: JEDEC-standard, RoHS-compliant	
– 24-ball T-PBGA 05/6mm x 8mm (5 x 5 array)	12
• Security features	
– Standard security	0
• Special options	
– Standard	S
– Automotive	A
• Operating temperature range	
– From –40°C to +85°C	IT
– From –40°C to +105°C	AT
– From –40°C to +125°C	UT

Part Number Ordering

Micron® **Xccela** flash devices are available in different configurations and densities. Verify valid part numbers by using Micron's part catalog search at www.micron.com. To compare features and specifications by device type, visit www.micron.com/products. Contact the factory for devices not found.

Figure 1: Part Number Ordering Information



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Device Description

This is a brief version of the MT35X data sheet. For complete information, please refer to the full NDA version.

To request access to the full NDA version of the MT35X data sheet, please contact your sales representative.

The Micron **Xccela** flash is a high-performance, multiple I/O, SPI-compatible flash memory device. It features a high-speed, low pin count **Xccela** bus interface with a DDR clock frequency of up to 200 MHz for 1.8V parts and up to 133 MHz for 3.0 V parts, using eight I/O signals and a data strobe (DQS pin).

SUSPEND and RESUME commands provide the ability to pause and resume PROGRAM/ERASE operations. Nonvolatile and volatile configuration registers enable respective default and temporary settings such as READ operation dummy clock cycles and wrap modes, memory protection, output buffer impedance, SPI protocol type and XIP mode.

Memory is organized as uniform 128KB sectors, 4KB and 32KB subsectors, and 256 byte pages. The device also includes a 64-byte one-time-programmable (OTP) memory area that can be permanently locked.

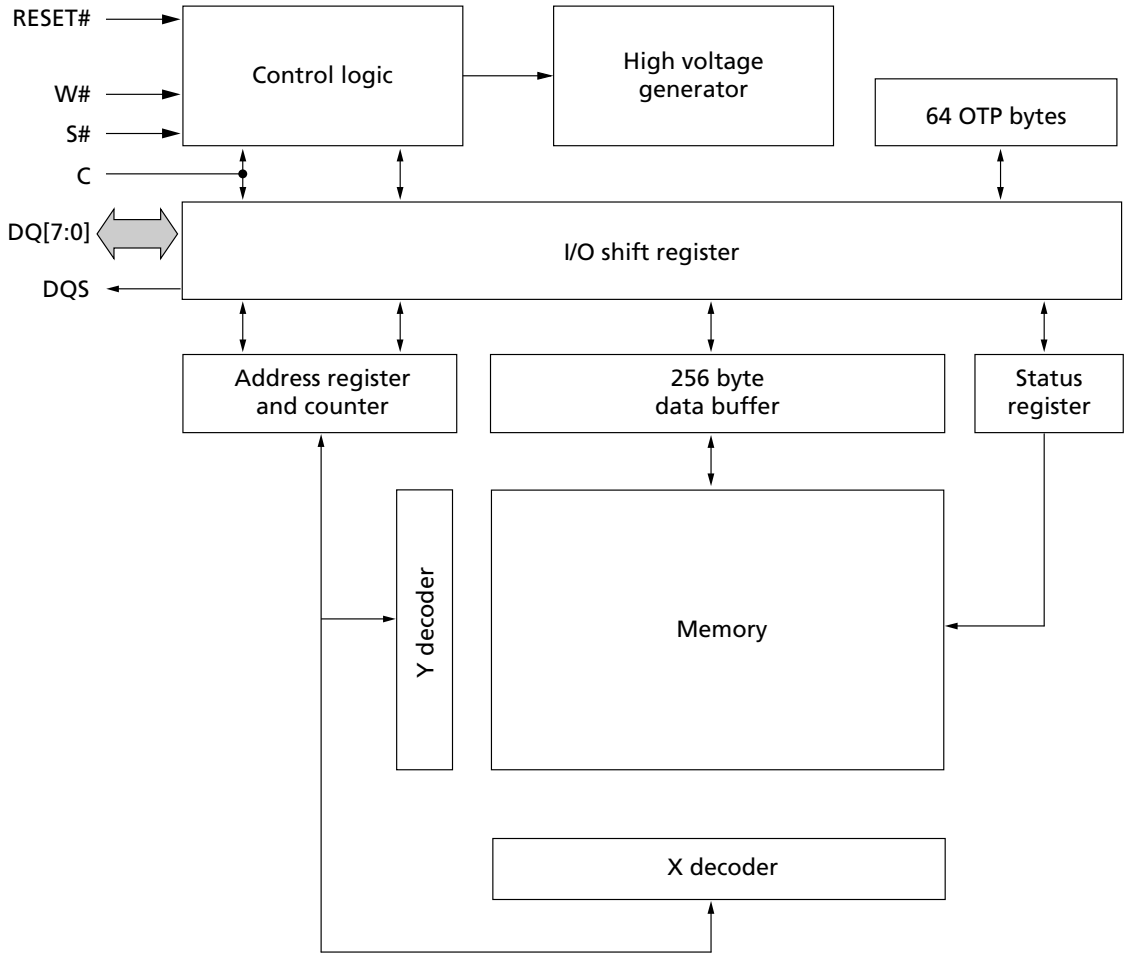
Direct boot in octal DDR protocol provides high performance and ease of use, enabling communication between the host and flash device without need to configure extended SPI protocol operations. However, the device still supports both extended SPI and octal DDR protocols to ensure legacy system support and an easy migration path. The extended SPI protocol supports address and data transmission on one or eight data lines, depending on the command.

Information in octal DDR protocol is always transmitted by eight data lines on both rising and falling clock edges. Most legacy x1 SPI commands are supported, but require only one clock cycle because the command is latched on both the rising and falling edges of the clock. Address cycles are fixed at 4-byte READ operations from the flash array.

The host is not required to drive DQS during the input operation to the memory. The data input (DQ) to the memory still relies on clock (C) to latch all address and data operations. Most register outputs require dummy clock cycles due to the critical timing from command decoding. With the help of DQS for data latching, the number of dummy clocks is transparent to the host.

Block Diagram

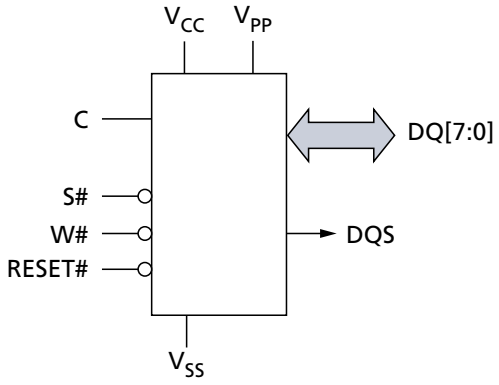
Figure 2: Block Diagram – Components and Signals



Note: 1. Each page of memory can be individually programmed, but the device is not page-erasable.

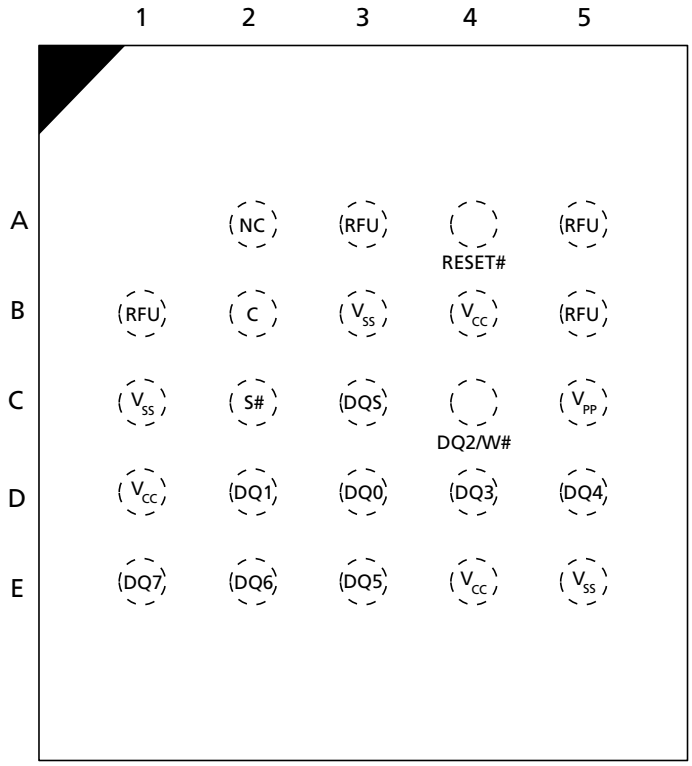
Device Logic Diagram

Figure 3: Logic Diagram



Signal Assignments

Figure 4: 24-Ball TBGA, 5 x 5 (Balls Down)



Signal Descriptions

The table below is a comprehensive list of device signals. All signals listed may not be supported. See Signal Assignments for device-specific information.

Table 1: Signal Descriptions

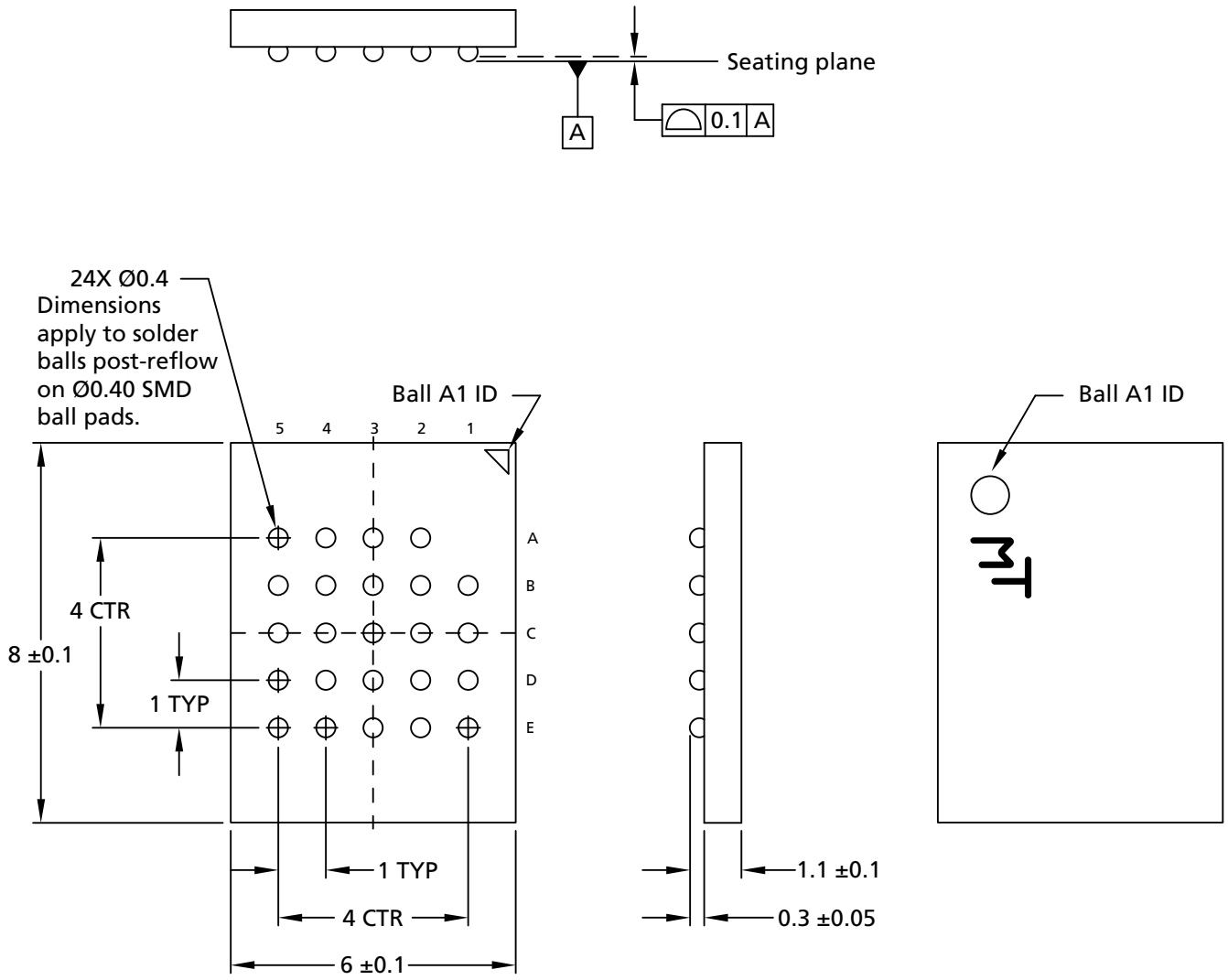
Symbol	Type	Description
C	Input	**Clock:** Provides timing for the serial interface. Command, address, or data inputs are latched on the rising edge of C. Data is shifted out on the falling edge of C.
S#	Input	**Chip select:** When S# is LOW, device is selected and in active power mode. Operations are initiated on the falling edge of S#. When S# is HIGH, device is deselected, DQ pins are tri-stated, and unless an internal WRITE operation is in progress, device enters standby mode.
RESET#	Input	**RESET:** Resets device to its default settings, such as after a volatile configuration register setting which then requires a return to the device default setting. Reset is optional when device settings are fixed by nonvolatile configuration register settings and always synchronized with the host. This pad is internally tied to weak pull-up so the pin can be floated.
W#	Input	**Write protect:** This input signal is used to freeze the status register in conjunction with the enable/disable bit of the status register. When the enable/disable bit of the status register is set to 1 and the W# signal is driven LOW, the status register nonvolatile bits become read-only and the WRITE STATUS REGISTER operation will not be executed. During the extended-SPI protocol with OCTAL READ/PROGRAM instructions, and during octal DDR protocol, this pin functions are an input/output (DQ2 functionality). This signal does not have internal pull-ups, it should not be left floated and must be driven, even if none of W#/DQ2 function is used.
DQ[7:0]	I/O	**Serial I/O:** Bidirectional signals that transfer address, data, and command information. In extended-SPI protocol, DQ0 functions as input and DQ1 as output. DQ[7:2] are not used. In octal protocol, input/output on DQ[7:0] depends on the command. Input can be latched on the rising edge of C (SDR) or on both edges of C (DDR). Data can be shifted out on the falling edge of C (SDR) or on both edges of C (DDR). In octal DDR, DQ[7:0] always function as I/O, input is latched on both edges of C, and output is shifted out on both edges of C. DQ2 is used also as write protection control.
DQS	Output	**Data strobe:** Indicates output data valid for DDR modes and is required to support high speed data output. Not required in extended-SPI protocol except to achieve high frequency for specific DDR commands. Used for READ but not for WRITE operations. Configured by nonvolatile and volatile configuration register bit 5 at address 00h. When enabled, DQS is driven to ground at S# LOW and until the device is driving output data, in which case DQS toggles to synchronize data output. When not enabled, DQS is not driven.
V_{CC}	Supply	**Supply voltage:** Core and I/O supply.
V_{PP}	Supply	**Supply voltage:** If V_{PP} is in the voltage range of V_{PPH}, the signal acts as an additional power supply for programming operation, as defined in the Operating Conditions table. The V_{PP} pad will be internally pulled up to V_{CC}, so customer can leave V_{PP} pin floated if not used.
V_{SS}	Supply	**Ground:** Core and I/O ground connection. V_{SS} is the reference for the V_{CC} supply voltage.
DNU	–	**Do not use:** Do not connect to any other signal, or power supply; must be left floating.
RFU	–	**Reserved for future use:** Reserved by Micron for future device functionality and enhancement. Recommend that these should be left floating. May be connected internally, but external connections will not affect operation.

Table 1: Signal Descriptions (Continued)

Symbol	Type	Description
NC	–	**No connect :** No internal connection; can be driven or floated.

Package Dimensions – Package Code: 12

Figure 5: 24-Ball T-PBGA (5 × 5 ball grid array) – 6mm × 8mm



Notes:
1. All dimensions are in millimeters.
2. See Part Number Ordering Information for complete package names and details.

Revision History

Rev. A – 04/18

- Initial release

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This data sheet contains initial characterization limits that are subject to change upon full characterization of production devices.

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MT35XU512ABA2G12-0AAT TR MT35XL256ABA2G12-0AAT MT35XL512ABA1G12-0SIT TR MT35XL02GCBA2G12-0SIT MT35XL512ABA2G12-0SIT MT35XU256ABA1G12-0AAT TR MT35XU01GBBA2G12-0SIT TR MT35XU512ABA2G12-0AAT MT35XU02GCBA1G12-0AUT MT35XL512ABA1G12-0AAT TR MT35XU01GBBA1G12-0SIT TR MT35XL01GBBA1G12-0SIT MT35XL512ABA1G12-0AAT MT35XL02GCBA1G12-0SIT TR MT35XU02GCBA2G12-0SIT MT35XU02GCBA1G12-0SIT TR MT35XL01GBBA1G12-0AAT TR MT35XL01GBBA2G12-0SIT MT35XL02GCBA1G12-0SIT MT35XU256ABA2G12-0AAT MT35XL01GBBA1G12-0SIT TR MT35XU02GCBA2G12-0AUT TR MT35XL01GBBA2G12-0SIT TR MT35XU01GBBA2G12-0AAT MT35XL256ABA1GSF-0AAT MT35XU512ABA1G12-0AAT MT35XU512ABA1G12-0AUT TR MT35XU256ABA2G12-0AAT TR MT35XL256ABA2GSF-0AAT MT35XU02GCBA1G12-0AUT TR MT35XU01GBBA1G12-0SIT MT35XU256ABA1G12-0AAT MT35XU512ABA1G12-0SIT TR MT35XL256ABA1GSF-0AAT TR MT35XL512ABA2G12-0AUT MT35XU512ABA1G12-0SIT MT35XL512ABA1G12-0AUT MT35XL512ABA2G12-0AAT MT35XU02GCBA1G12-0SIT MT35XL256ABA2GSF-0AAT TR MT35XU512ABA2G12-0AUT MT35XU512ABA1G12-0AAT TR MT35XL01GBBA2G12-0AAT TR MT35XL512ABA1G12-0SIT MT35XU02GCBA2G12-0SIT TR MT35XU512ABA2G12-0AUT TR MT35XU01GBBA1G12-0AAT MT35XL02GCBA2G12-0SIT TR MT35XU512ABA2G12-0SIT TR MT35XU512ABA2G12-0SIT MT35XU01GBBA1G12-0AAT TR MT35XU02GCBA2G12-0AUT MT35XL512ABA2G12-0SIT TR MT35XL256ABA2G12-0AAT TR MT35XL512ABA2G12-0AUT TR MT35XL256ABA1G12-0AAT MT35XU01GBBA2G12-0SIT MT35XL01GBBA1G12-0AAT MT35XU512ABA1G12-0AUT MT35XL512ABA1G12-0AUT TR MT35XU01GBBA2G12-0AAT TR MT35XL256ABA1G12-0AAT TR MT35XL01GBBA2G12-0AAT MT35XL512ABA2G12-0AAT TR MT35XU01GBBA1G12-0AUT MT35XU01GBBA2G12-0AUT MT35XU02GCBA1G12-0AAT MT35XU02GCBA2G12-0AAT MT35XU256ABA1G12-0AUT MT35XU256ABA2G12-0AUT MT35XU256ABA1G12-0AUT TR MT35XU256ABA2G12-0AUT TR MT35XU01GBBA2G12-0AUT TR MT35XU02GCBA1G12-0AAT TR MT35XU02GCBA2G12-0AAT TR MT35XU01GBBA1G12-0AUT TR