A New Method for Measuring Parasitics of Super Junction Power MOSFETs

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Abstract

This document proposes a new methodology to measure the voltage-dependent behavior of parasitic capacitances of super junction power MOSFETs. The measurement technique allows to extract all parasitic elements (capacitances and inductances) with only one measurement while a variable DC voltage is applied between the drain and source pin of the super junction MOSFET. The results can be used to create simulation models of MOSFETs and possibly complete power modules, that accurately represent their high frequency behavior to solve electromagnetic compatibility (EMC) problems in transient simulators, such as LTspice.

Introduction

Super junction power MOSFETs are widely used to build highly efficient switched mode power supplies with very high power density. This is due to the fact that these kind of MOSFETs can be switched at high frequencies, which in turn allows small inductors and capacitors to be used. However, high switching frequencies demand short switching transitions, which is at the expense of more conducted and radiated emissions due to high di/dt and du/dt thus impairing the electromagnetic compatibility (EMC) of the circuit [1].

Microelectronic developers are trying to counteract these emissions by building smart gate drivers to improve the over all device performance [2], but this development presents new challenges to the simulation models for transient simulators like LTspice. Apart from functionality and temperature behavior, developers must be able to accurately model the high frequency behavior of the whole electronic circuit in order to build devices that are not only efficient, but can also pass an EMC test first time right.

Unfortunately the Spice models of most manufacturers of super junction power MOSFET are not suitable to fulfill those requirements. In general there are two types of models:

1. ”Analytical models” [3] are calculation-based and quite accurate, but often extend the necessary simulation time for EMC-simulations [4]. The modeling process often involves utilizing finite element analysis (FEA) to estimate the parasitic elements based on material and geometry of the power MOSFET [5].

2. ”Behavioral models” have been proposed to tackle the problem of EMC-simulation in countless papers [4, 6–8]. The accuracy of these models strongly depends either on adequate information from the manufacturer, or accurate extraction of the parasitics from measurements.

This paper discusses a new method to accurately measure the voltage behavior of the parasitic capacitances and other parasitics, like lead inductances, and terminal resistances without any prior knowledge about the internal structure of the transistor. It further shows how a behavioral model for fast EMC-simulation can then be extracted out of the measurements.

The Behavioral MOSFET Model

Fig. 1 shows the basic structure of a n-channel super junction power MOSFET, similar to [9] or [10]. Typically, the structure is vertical. Here the voltage rating is basically a function of the doping level and the thickness of the N-layer, while the current rating is a function of the channel width. Super junction power MOSFET can therefore sustain both high currents in the on-state and high blocking voltages in the off-state, which makes them usable for the application in high-voltage switched mode power supplies.

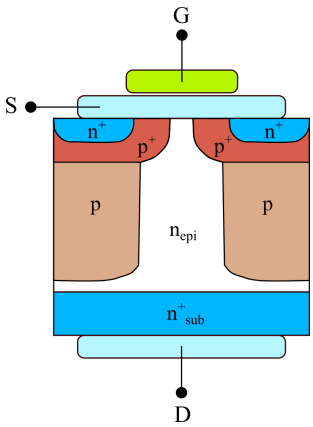

Fig. 1: Basic structure of an n-channel super-junction power MOSFET.

The structure of a super junction power MOSFET has many implications on its simulation model. While the capacitance between gate and source, C_{GS}, can be assumed to be remotely constant, the gate-drain capacitance C_{GD} is highly dependent on the gate-drain voltage V_{GD} and the drain-source voltage V_{DS} due to the varying extension of the depletion region when the MOSFET is in off-state [11].

Last but not least the impedance of the bonding wires to drain, gate and source, as well as the housing have an influence on the simulation model. A simple way to get an sufficiently accurate and fast model for EMC-simulations is with the help of a ”behavioral model”, which is depicted in Fig. 2. The behavior of the MOSFET itself is modeled with a voltage dependent current source I_{DS}. The second current source I_{SD} models the behavior of the body diode. The model also includes all the parasitic capacitances mentioned above, as well as the distributed inductance of the bonding wires and connectors, modeled by the resistances R_G, R_S and R_D and the stray inductances L_D, L_G and L_S.

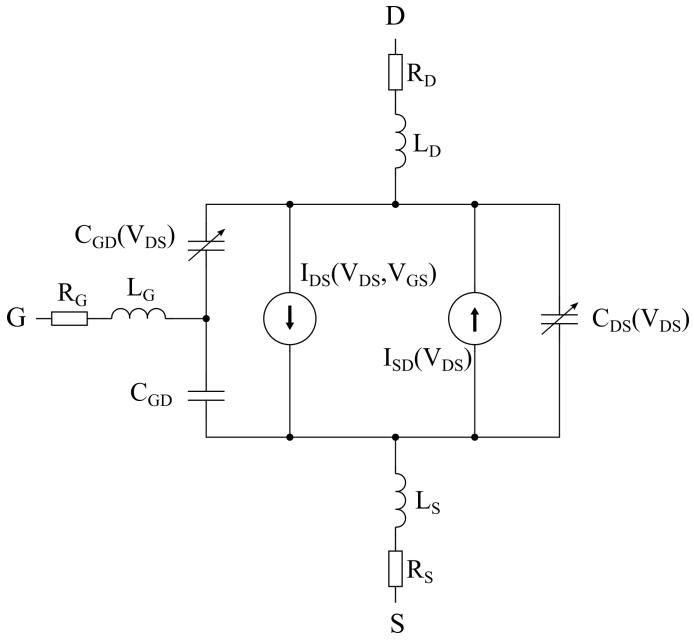

Fig. 2: Behavioral model of a super junction power MOSFET including equivalents of the parasitic elements.

Advantages of a New Measurement Method

The Traditional Method

Traditionally most of the data-sheets offer three values for the parasitic capacitances of the power MOSFET, which are labeled C_{iss}, C_{oss} and C_{rss}. All of them are defined in terms of the equivalent circuit capacities, like in equation (1), (2) and (3). The usual method to measure the parasitic capacitances is commonly known and well described (for instance in the referenced application note by Keysight [11]). To highlight the differences to the proposed measurement setup, it shall be described briefly below.

$$C_{iss} = C_{GS} + C_{GD}, \quad C_{DS}\ shorted \tag{1}$$

$$C_{oss} = C_{DS} + C_{GD} \tag{2}$$

$$C_{rss} = C_{GD} \tag{3}$$

The three parasitic capacitances C_{iss}, C_{oss} and C_{rss} are most commonly measured as it is shown in the Figs. 3, 4 and 5 respectively. The capacitance meter thereby uses a small signal with a single frequency of usually 10 kHz or 100 kHz to measure the value of the parasitic capacitances. Additional short-circuits and -capacitors have to be used to counteract the influence of all other parasitics while one measurement is done.

Problems with the Traditional Method

With the previously described measurement method, only the parasitic capacitances can be determined. All other parasitics, like the distributed inductances, which are needed for a good behavioral model, have to be either guessed from experience, or confidingly taken from the data-sheet of the manufacturer. In addition, a total of three individual measurements are necessary to determine all capacitances. The new method proposed here is intended to make do with a single measurement.

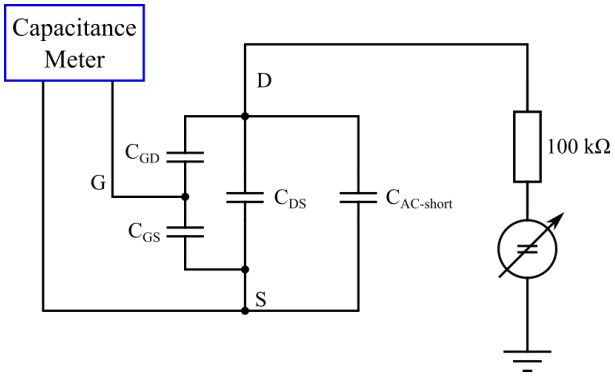

Fig. 3: Schematic to measure the input capacitance C_{iss}.

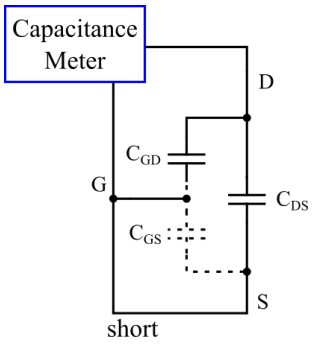

Fig. 4: Schematic to measure the output capacitance C_{oss}.

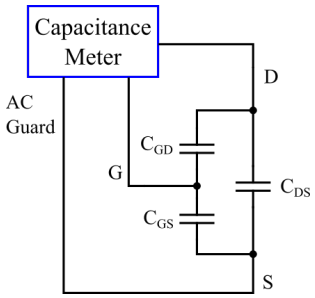

Fig. 5: Schematic to measure the reverse capacitance $C_{rss} = C_{GD}$.

Improvements with Frequency & Voltage Dependent Measurements

With the proposed method, scattering parameters (S-parameters) can be measured with a vector network analyzer (VNA) in order to evaluate all the parasitics of a MOSFET. This method is common practice in the field of high-frequency engineering and power electronics and is described in great detail in chapter 7 of [12].

The proposed measurement circuit, shown in Fig. 6 is quite similar to the method shown in [13], but allows to measure the parasitics not only as a function of frequency, but also as a function of the drain-source voltage V_{DS}. The VNA is connected to the gate- and the source-pin of a super junction power MOSFET. The drain-pin of the MOSFET is connected to HF-ground, which is also the reference for the VNA. A high-voltage source is used to apply different drain-source voltages, while a DC blocker keeps the high DC voltage away from the VNA, since the measurement device would be seriously damaged otherwise. In addition, two RF filters ensure that the connected voltage source does not falsify the measurement in a frequency range from 10 kHz to 2 GHz.

The VNA measures all the scattering parameters S_{11}, S_{21}, S_{12} and S_{22} while the DC-voltage V_{DS} is

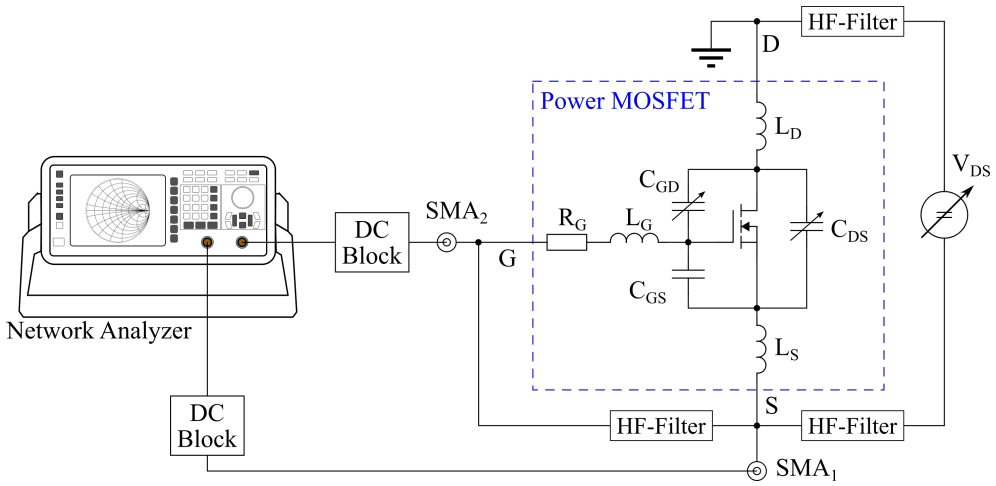

Fig. 6: Block diagram of the two-port S-parameter measurement setup to measure the parasitics of a super junction power MOSFET.

stepwise increased to 300 V with a step size of 1 V. The S-parameters are then converted to Z-parameters with the help of eqs. (4) to (7) where Z_0 is the characteristic impedance of each port of the VNA, which is 50 Ω. Fig. 9 shows the impedance characteristic of all parasitics of the MOSFET using the example of Z_21. It can be seen, that the resonance frequency changes with drain-source voltage, which is a result of the voltage dependent gate-drain capacitances C_{GD} and C_{GS}.

$$Z_{11} = \frac{(1+S_{11})(1-S_{22})+S_{12}S_{21}}{(1-S_{11})(1-S_{22})-S_{12}S_{21}} \cdot Z_0 \tag{4}$$

$$Z_{21} = \frac{2S_{21}}{(1-S_{11})(1-S_{22})-S_{12}S_{21}} \cdot Z_0 \tag{5}$$

$$Z_{12} = \frac{2S_{12}}{(1-S_{11})(1-S_{22})-S_{12}S_{21}} \cdot Z_0 \tag{6}$$

$$Z_{22} = \frac{(1-S_{11})(1+S_{22})+S_{12}S_{21}}{(1-S_{11})(1-S_{22})-S_{12}S_{21}} \cdot Z_0 \tag{7}$$

Furthermore the whole impedance characteristic shows capacitive behavior at low frequencies and inductive behavior for high frequencies (due to the parasitic inductances L_G, L_S and L_D). As it is described in great detail in [5] and [13], the parasitic capacitances C_{GS}, C_{GD} and C_{DS} can be calculated by taking impedance values at low frequencies and putting them into eqs. (8) to (10) and eqs. (11) to (13).

$$X_{C_D} = Z_{21} \; or \; Z_{12} \tag{8}$$

$$X_{C_G} = Z_{22} - Z_{21} \; or \; Z_{22} - Z_{12} \tag{9}$$

$$X_{C_S} = Z_{11} - Z_{21} \;\; or \;\; Z_{11} - Z_{12} \tag{10}$$

$$C_{GS} = \frac{2\pi f \cdot X_{C_D}}{X_{C_D}(X_{C_G}) + X_{C_D}(X_{C_S}) + (X_{C_S})(X_{C_G})} \tag{11}$$

$$C_{GD} = \frac{2\pi f \cdot (X_{C_S})}{X_{C_D}(X_{C_G}) + X_{C_D}(X_{C_S}) + (X_{C_S})(X_{C_G})} \tag{12}$$

$$C_{DS} = \frac{2\pi f \cdot (X_{C_G})}{X_{C_D}(X_{C_G}) + X_{C_D}(X_{C_S}) + (X_{C_S})(X_{C_G})} \tag{13}$$

The parasitic inductances are consequently calculated by taking some values at high frequencies and putting them into eqs. (14) to (16) and eqs. (18) to (17).

$$X_{L_D} = Z_{21} \;\; or \;\; Z_{12} \tag{14}$$

$$X_{L_G} = Z_{22} - Z_{21} \;\; or \;\; Z_{22} - Z_{12} \tag{15}$$

$$X_{L_S} = Z_{11} - Z_{21} \;\; or \;\; Z_{11} - Z_{12} \tag{16}$$

$$L_D = \frac{X_{L_D}}{2\pi f} \tag{17}$$

$$L_G = \frac{X_{L_G}}{2\pi f} \tag{18}$$

$$L_S = \frac{X_{L_S}}{2\pi f} \tag{19}$$

Fig. 7 and 8 show the calculated parasitic capacitances as a function of the drain-source voltage V_{DS}. As expected, one can clearly see that the capacities C_{DS} and C_{GD} are highly dependent on the voltage, especially in the range between 0 V and 50 V. In addition, it can be seen that the capacitance of C_{GS} remains the same over the entire voltage range, which was also to be expected. The datasheet of the measured MOSFET shows similar results as it can be seen in Fig. 8. The measured values from 7 can directly be used to model the voltage dependent capacitances for a simulation model of the MOSFET.

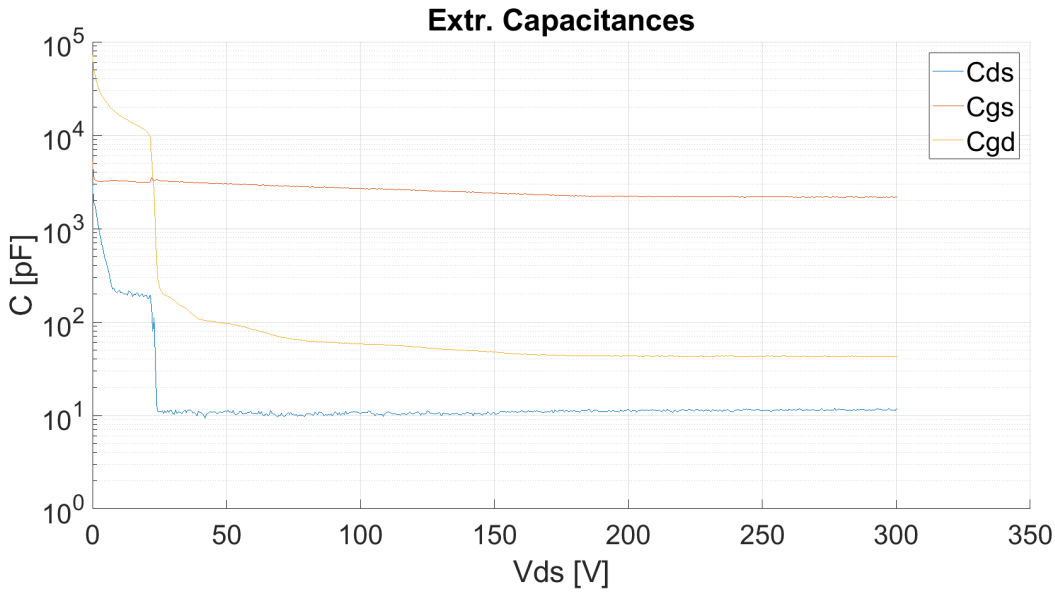

Fig. 7: Parasitic capacitances C_{DS}, C_{GS} and C_{GD} as a function of the drain-source voltage V_{DS}.

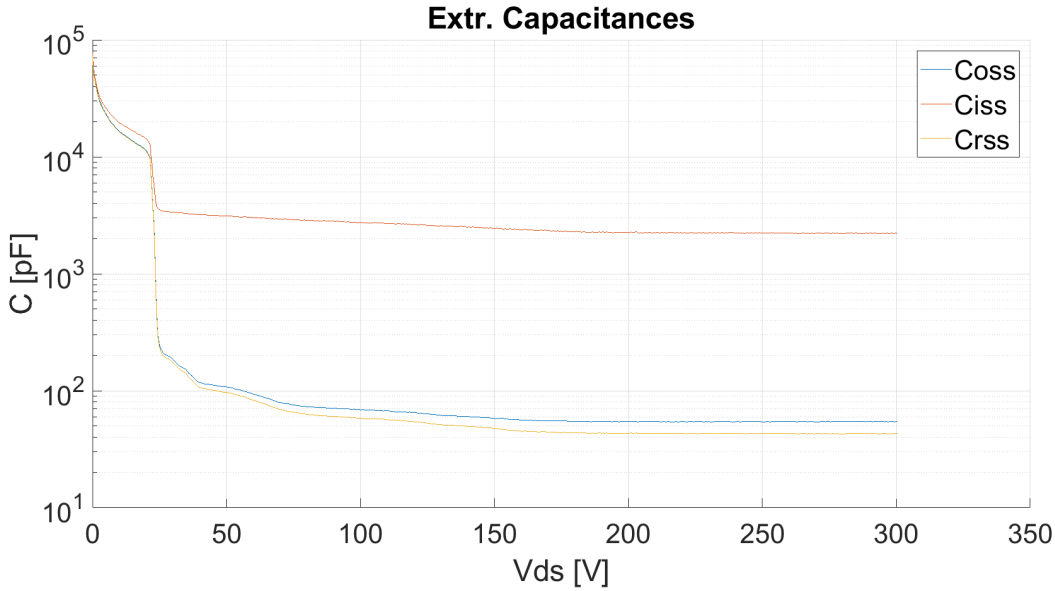

Fig. 8: C_{oss}, C_{iss} and C_{rss} as a function of the drain-source voltage V_{DS}.

Conclusion

This paper presents a new method to measure all parasitics of a super junction power MOSFET in dependency of the drain-source voltage V_{DS}. The shown measurement results can be used in order to generate behavioral models of such MOSFETs, which are commonly used in transient EMC-simulations, as they significantly decrease the simulation time. The paper compares the traditional measurement method, which requires three measurements, with the new measurement method, which can obtain the values of all parasictic elements with just one single measurement. The work demonstrates that the basic measurement principal is already getting plausible results. Improvements of the measurement system to decrease the noise in the measurement in order to get highly accurate simulation models are currently ongoing.

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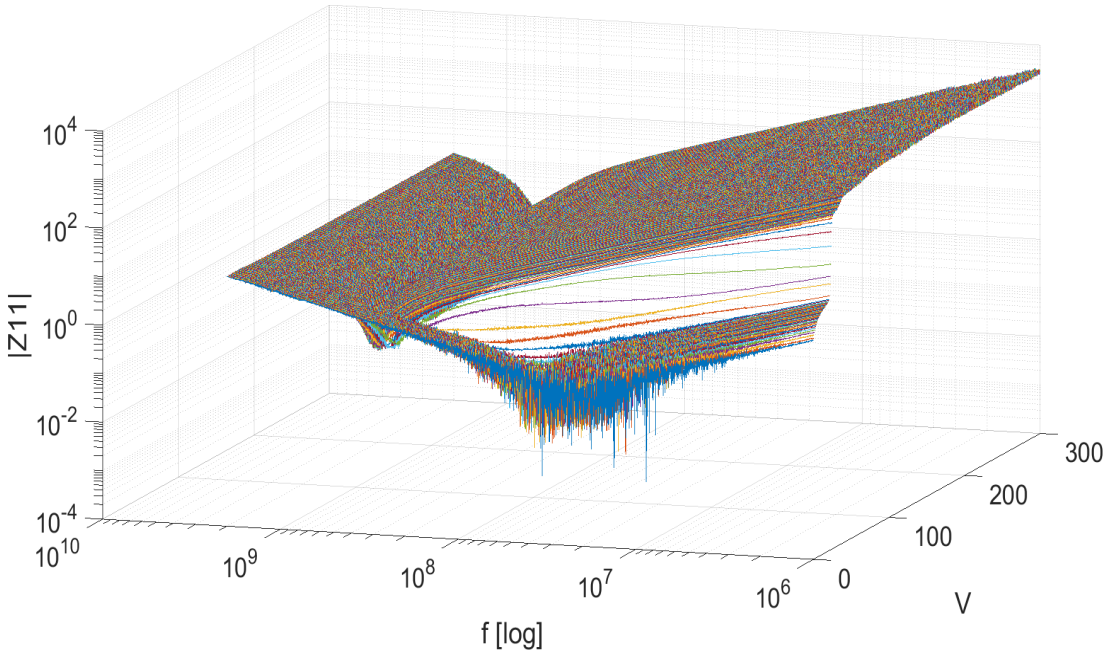

Fig. 9: Measurement of Z_{11} between gate and source of a super junction power MOSFET.

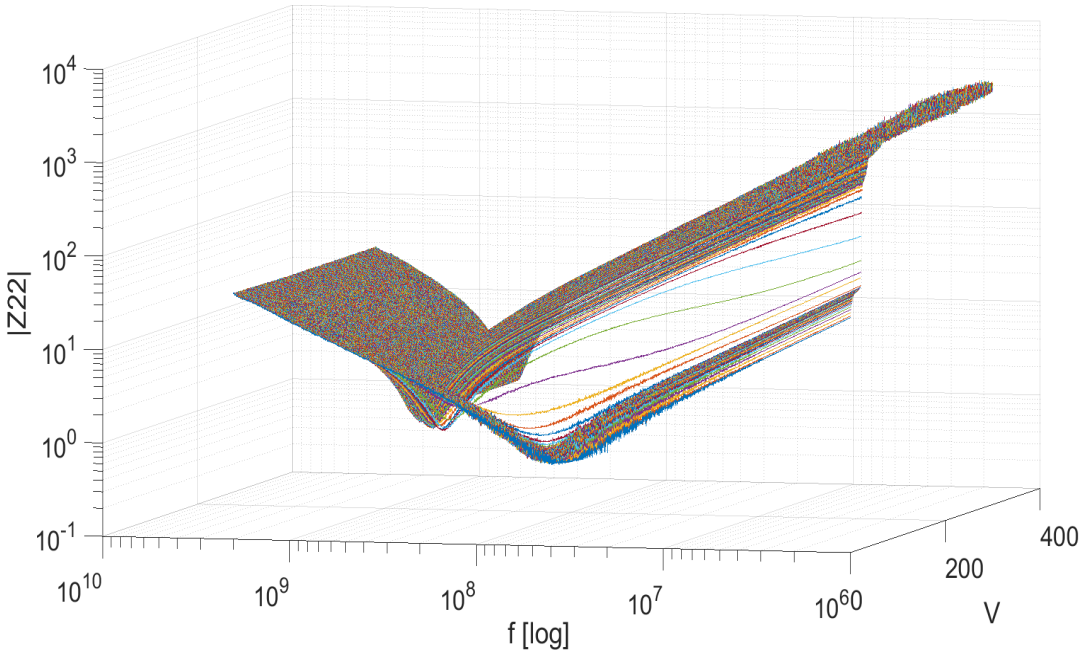

Fig. 10: Measurement of Z_{22} between gate and source of a super junction power MOSFET.