View this file with a JavaScript-enabled browser to enable all features.

Static Timing Analysis

Project : EMG
Build Time : 09/28/18 17:52:20
Device : CY8C5868AXI-LP035
Temperature : 0C - 85/125C
VDDA : 5.00
VDDABUF : 5.00
VDDD : 5.00
VDDIO0 : 5.00
VDDIO1 : 5.00
VDDIO2 : 5.00
VDDIO3 : 5.00
VUSB : 5.00
Voltage : 5.0

Expand All | Collapse All | Show All Paths | Hide All Paths

+ Timing Violation Section

Note: If your design will only ever run at typical room temperatures, selecting the narrower temperature range in the system DWR for your application helps the tool to find timing-compliant routing solutions.

Violation	Source Clock	Destination Clock	Slack(ns)
Async			
	\ADC_DelSig_1:DEC\/interrupt	CyBUS_CLK	

+ Clock Summary Section

Clock	Domain	Nominal Frequency	Required Frequency	Maximum Frequency	Violation
ADC_DelSig_1_Ext_CP_Clk	ADC_DelSig_1_Ext_CP_Clk	24.000 MHz	24.000 MHz	N/A	
ADC_DelSig_1_Ext_CP_Clk (routed)	ADC_DelSig_1_Ext_CP_Clk (routed)	24.000 MHz	24.000 MHz	N/A	
ClockBlock/aclk_glb_ff_0	ClockBlock/aclk_glb_ff_0	UNKNOWN	UNKNOWN	N/A	
CyILO	CyILO	100.000 kHz	100.000 kHz	N/A	
CyIMO	CyIMO	24.000 MHz	24.000 MHz	N/A	
CyMASTER_CLK	CyMASTER_CLK	24.000 MHz	24.000 MHz	N/A	
CyBUS_CLK	CyMASTER_CLK	24.000 MHz	24.000 MHz	48.626 MHz	
ADC_DelSig_1_theACLK	CyMASTER_CLK	1.600 MHz	1.600 MHz	N/A	
CyPLL_OUT	CyPLL_OUT	24.000 MHz	24.000 MHz	N/A	
\ADC_DelSig_1:DSM\/dec_clock	\ADC_DelSig_1:DSM\/dec_clock	UNKNOWN	UNKNOWN	N/A	
\ADC_DelSig_1:DEC\/interrupt	\ADC_DelSig_1:DSM\/dec_clock	UNKNOWN	UNKNOWN	N/A	

+ Register to Register Section

+ Setup Subsection

+ Source Clock : CyBUS_CLK : Positive edge(Required Frequency 24 MHz)

+ Destination Clock : CyBUS_CLK : Positive edge(Required Frequency 24 MHz)

Path Delay Requirement : 41.6667ns(24 MHz)

Source	Destination

Source	Destination
\Timer:TimerUDB:sT32:timerdp:u0\/z0	\Timer:TimerUDB:sT32:timerdp:u3\/ci

Type	Location	Fanout	Instance/Net	Source
datapathcell2	U(1,1)	1	\Timer:TimerUDB:sT32:timerdp:u0\	\Timer:TimerUDB:sT32:timerdp:u\/clock
Route		1	\Timer:TimerUDB:sT32:timerdp:u0.z0__sig\	\Timer:TimerUDB:sT32:timerdp:u\/z0
datapathcell3	U(0,1)	1	\Timer:TimerUDB:sT32:timerdp:u1\	\Timer:TimerUDB:sT32:timerdp:u\/z0i
Route		1	\Timer:TimerUDB:sT32:timerdp:u1.z0__sig\	\Timer:TimerUDB:sT32:timerdp:u\/z0
datapathcell4	U(0,0)	1	\Timer:TimerUDB:sT32:timerdp:u2\	\Timer:TimerUDB:sT32:timerdp:u\/z0i
Route		1	\Timer:TimerUDB:sT32:timerdp:u2.z0__sig\	\Timer:TimerUDB:sT32:timerdp:u\/z0
datapathcell5	U(1,0)	1	\Timer:TimerUDB:sT32:timerdp:u3\	\Timer:TimerUDB:sT32:timerdp:u\/z0i
Route		1	\Timer:TimerUDB:per_zero\	\Timer:TimerUDB:sT32:timerdp:u\/z0_comb
datapathcell2	U(1,1)	1	\Timer:TimerUDB:sT32:timerdp:u0\	\Timer:TimerUDB:sT32:timerdp:u\/cs_addr_0
Route		1	\Timer:TimerUDB:sT32:timerdp:u0.co_msb__sig\	\Timer:TimerUDB:sT32:timerdp:u\/co_msb
datapathcell3	U(0,1)	1	\Timer:TimerUDB:sT32:timerdp:u1\	\Timer:TimerUDB:sT32:timerdp:u\/ci
Route		1	\Timer:TimerUDB:sT32:timerdp:u1.co_msb__sig\	\Timer:TimerUDB:sT32:timerdp:u\/co_msb
datapathcell4	U(0,0)	1	\Timer:TimerUDB:sT32:timerdp:u2\	\Timer:TimerUDB:sT32:timerdp:u\/ci
Route		1	\Timer:TimerUDB:sT32:timerdp:u2.co_msb__sig\	\Timer:TimerUDB:sT32:timerdp:u\/co_msb
datapathcell5	U(1,0)	1	\Timer:TimerUDB:sT32:timerdp:u3\	
Clock				

Source	Destination
\Timer:TimerUDB:sT32:timerdp:u1\/z0	\Timer:TimerUDB:sT32:timerdp:u3\/ci

Type	Location	Fanout	Instance/Net	Source
datapathcell3	U(0,1)	1	\Timer:TimerUDB:sT32:timerdp:u1\	\Timer:TimerUDB:sT32:timerdp:u\/clock
Route		1	\Timer:TimerUDB:sT32:timerdp:u1.z0__sig\	\Timer:TimerUDB:sT32:timerdp:u\/z0
datapathcell4	U(0,0)	1	\Timer:TimerUDB:sT32:timerdp:u2\	\Timer:TimerUDB:sT32:timerdp:u\/z0i
Route		1	\Timer:TimerUDB:sT32:timerdp:u2.z0__sig\	\Timer:TimerUDB:sT32:timerdp:u\/z0
datapathcell5	U(1,0)	1	\Timer:TimerUDB:sT32:timerdp:u3\	\Timer:TimerUDB:sT32:timerdp:u\/z0i
Route		1	\Timer:TimerUDB:per_zero\	\Timer:TimerUDB:sT32:timerdp:u\/z0_comb
datapathcell2	U(1,1)	1	\Timer:TimerUDB:sT32:timerdp:u0\	\Timer:TimerUDB:sT32:timerdp:u\/cs_addr_0
Route		1	\Timer:TimerUDB:sT32:timerdp:u0.co_msb__sig\	\Timer:TimerUDB:sT32:timerdp:u\/co_msb
datapathcell3	U(0,1)	1	\Timer:TimerUDB:sT32:timerdp:u1\	\Timer:TimerUDB:sT32:timerdp:u\/ci
Route		1	\Timer:TimerUDB:sT32:timerdp:u1.co_msb__sig\	\Timer:TimerUDB:sT32:timerdp:u\/co_msb
datapathcell4	U(0,0)	1	\Timer:TimerUDB:sT32:timerdp:u2\	\Timer:TimerUDB:sT32:timerdp:u\/ci
Route		1	\Timer:TimerUDB:sT32:timerdp:u2.co_msb__sig\	\Timer:TimerUDB:sT32:timerdp:u\/co_msb
datapathcell5	U(1,0)	1	\Timer:TimerUDB:sT32:timerdp:u3\	
Clock				

Source	Destination
\Timer:TimerUDB:sT32:timerdp:u2\/z0	\Timer:TimerUDB:sT32:timerdp:u3\/ci

Type	Location	Fanout	Instance/Net	Source
datapathcell4	U(0,0)	1	\Timer:TimerUDB:sT32:timerdp:u2\	\Timer:TimerUDB:sT32:timerdp:u\/clock
Route		1	\Timer:TimerUDB:sT32:timerdp:u2.z0__sig\	\Timer:TimerUDB:sT32:timerdp:u\/z0
datapathcell5	U(1,0)	1	\Timer:TimerUDB:sT32:timerdp:u3\	\Timer:TimerUDB:sT32:timerdp:u\/z0i
Route		1	\Timer:TimerUDB:per_zero\	\Timer:TimerUDB:sT32:timerdp:u\/z0_comb
datapathcell2	U(1,1)	1	\Timer:TimerUDB:sT32:timerdp:u0\	\Timer:TimerUDB:sT32:timerdp:u\/cs_addr_0
Route		1	\Timer:TimerUDB:sT32:timerdp:u0.co_msb__sig\	\Timer:TimerUDB:sT32:timerdp:u\/co_msb
datapathcell3	U(0,1)	1	\Timer:TimerUDB:sT32:timerdp:u1\	\Timer:TimerUDB:sT32:timerdp:u\/ci
Route		1	\Timer:TimerUDB:sT32:timerdp:u1.co_msb__sig\	\Timer:TimerUDB:sT32:timerdp:u\/co_msb
datapathcell4	U(0,0)	1	\Timer:TimerUDB:sT32:timerdp:u2\	\Timer:TimerUDB:sT32:timerdp:u\/ci

Source			Destination	
Type	**Location**	**Fanout**	**Instance/Net**	**Source**
Route		1	\Timer:TimerUDB:sT32:timerdp:u2.co_msb__sig\	\Timer:TimerUDB:sT32:timerdp:u\/co_msb
datapathcell5	U(1,0)	1	\Timer:TimerUDB:sT32:timerdp:u3\	
Clock				

\Timer:TimerUDB:sT32:timerdp:u0\/z0	\Timer:TimerUDB:sT32:timerdp:u3\/ci

Type	**Location**	**Fanout**	**Instance/Net**	**Source**
datapathcell2	U(1,1)	1	\Timer:TimerUDB:sT32:timerdp:u0\	\Timer:TimerUDB:sT32:timerdp:u\/clock
Route		1	\Timer:TimerUDB:sT32:timerdp:u0.z0__sig\	\Timer:TimerUDB:sT32:timerdp:u\/z0
datapathcell3	U(0,1)	1	\Timer:TimerUDB:sT32:timerdp:u1\	\Timer:TimerUDB:sT32:timerdp:u\/z0i
Route		1	\Timer:TimerUDB:sT32:timerdp:u1.z0__sig\	\Timer:TimerUDB:sT32:timerdp:u\/z0
datapathcell4	U(0,0)	1	\Timer:TimerUDB:sT32:timerdp:u2\	\Timer:TimerUDB:sT32:timerdp:u\/z0i
Route		1	\Timer:TimerUDB:sT32:timerdp:u2.z0__sig\	\Timer:TimerUDB:sT32:timerdp:u\/z0
datapathcell5	U(1,0)	1	\Timer:TimerUDB:sT32:timerdp:u3\	\Timer:TimerUDB:sT32:timerdp:u\/z0i
Route		1	\Timer:TimerUDB:per_zero\	\Timer:TimerUDB:sT32:timerdp:u\/z0_comb
datapathcell3	U(0,1)	1	\Timer:TimerUDB:sT32:timerdp:u1\	\Timer:TimerUDB:sT32:timerdp:u\/cs_addr_0
Route		1	\Timer:TimerUDB:sT32:timerdp:u1.co_msb__sig\	\Timer:TimerUDB:sT32:timerdp:u\/co_msb
datapathcell4	U(0,0)	1	\Timer:TimerUDB:sT32:timerdp:u2\	\Timer:TimerUDB:sT32:timerdp:u\/ci
Route		1	\Timer:TimerUDB:sT32:timerdp:u2.co_msb__sig\	\Timer:TimerUDB:sT32:timerdp:u\/co_msb
datapathcell5	U(1,0)	1	\Timer:TimerUDB:sT32:timerdp:u3\	
Clock				

\Timer:TimerUDB:sT32:timerdp:u0\/z0	\Timer:TimerUDB:rstSts:stsreg\/status_0

Type	**Location**	**Fanout**	**Instance/Net**	**Source**
datapathcell2	U(1,1)	1	\Timer:TimerUDB:sT32:timerdp:u0\	\Timer:TimerUDB:sT32:timerdp:u0\/clock
Route		1	\Timer:TimerUDB:sT32:timerdp:u0.z0__sig\	\Timer:TimerUDB:sT32:timerdp:u0\/z0
datapathcell3	U(0,1)	1	\Timer:TimerUDB:sT32:timerdp:u1\	\Timer:TimerUDB:sT32:timerdp:u1\/z0i
Route		1	\Timer:TimerUDB:sT32:timerdp:u1.z0__sig\	\Timer:TimerUDB:sT32:timerdp:u1\/z0
datapathcell4	U(0,0)	1	\Timer:TimerUDB:sT32:timerdp:u2\	\Timer:TimerUDB:sT32:timerdp:u2\/z0i
Route		1	\Timer:TimerUDB:sT32:timerdp:u2.z0__sig\	\Timer:TimerUDB:sT32:timerdp:u2\/z0
datapathcell5	U(1,0)	1	\Timer:TimerUDB:sT32:timerdp:u3\	\Timer:TimerUDB:sT32:timerdp:u3\/z0i
Route		1	\Timer:TimerUDB:per_zero\	\Timer:TimerUDB:sT32:timerdp:u3\/z0_comb
macrocell11	U(1,1)	1	\Timer:TimerUDB:status_tc\	\Timer:TimerUDB:status_tc\/main_1
Route		1	\Timer:TimerUDB:status_tc\	\Timer:TimerUDB:status_tc\/q
statusicell2	U(1,0)	1	\Timer:TimerUDB:rstSts:stsreg\	
Clock				

\Timer:TimerUDB:sT32:timerdp:u0\/z0	\Timer:TimerUDB:sT32:timerdp:u2\/ci

Type	**Location**	**Fanout**	**Instance/Net**	**Source**
datapathcell2	U(1,1)	1	\Timer:TimerUDB:sT32:timerdp:u0\	\Timer:TimerUDB:sT32:timerdp:u\/clock
Route		1	\Timer:TimerUDB:sT32:timerdp:u0.z0__sig\	\Timer:TimerUDB:sT32:timerdp:u\/z0
datapathcell3	U(0,1)	1	\Timer:TimerUDB:sT32:timerdp:u1\	\Timer:TimerUDB:sT32:timerdp:u\/z0i
Route		1	\Timer:TimerUDB:sT32:timerdp:u1.z0__sig\	\Timer:TimerUDB:sT32:timerdp:u\/z0
datapathcell4	U(0,0)	1	\Timer:TimerUDB:sT32:timerdp:u2\	\Timer:TimerUDB:sT32:timerdp:u\/z0i
Route		1	\Timer:TimerUDB:sT32:timerdp:u2.z0__sig\	\Timer:TimerUDB:sT32:timerdp:u\/z0
datapathcell5	U(1,0)	1	\Timer:TimerUDB:sT32:timerdp:u3\	\Timer:TimerUDB:sT32:timerdp:u\/z0i
Route		1	\Timer:TimerUDB:per_zero\	\Timer:TimerUDB:sT32:timerdp:u\/z0_comb
datapathcell2	U(1,1)	1	\Timer:TimerUDB:sT32:timerdp:u0\	\Timer:TimerUDB:sT32:timerdp:u\/cs_addr_0
Route		1	\Timer:TimerUDB:sT32:timerdp:u0.co_msb__sig\	\Timer:TimerUDB:sT32:timerdp:u\/co_msb
datapathcell3	U(0,1)	1	\Timer:TimerUDB:sT32:timerdp:u1\	\Timer:TimerUDB:sT32:timerdp:u\/ci

Source				Destination
Type	**Location**	**Fanout**	**Instance/Net**	**Source**
Route		1	\Timer:TimerUDB:sT32:timerdp:u1.co_msb__sig\	\Timer:TimerUDB:sT32:timerdp:u\ \/co_msb
datapathcell4	U(0,0)	1	\Timer:TimerUDB:sT32:timerdp:u2\	
Clock				

\Timer:TimerUDB:sT32:timerdp:u3\/z0_comb	\Timer:TimerUDB:sT32:timerdp:u3\/ci

Type	**Location**	**Fanout**	**Instance/Net**	**Source**
datapathcell5	U(1,0)	1	\Timer:TimerUDB:sT32:timerdp:u3\	\Timer:TimerUDB:sT32:timerdp:u\ \/clock
Route		1	\Timer:TimerUDB:per_zero\	\Timer:TimerUDB:sT32:timerdp:u\ \/z0_comb
datapathcell2	U(1,1)	1	\Timer:TimerUDB:sT32:timerdp:u0\	\Timer:TimerUDB:sT32:timerdp:u\ \/cs_addr_0
Route		1	\Timer:TimerUDB:sT32:timerdp:u0.co_msb__sig\	\Timer:TimerUDB:sT32:timerdp:u\ \/co_msb
datapathcell3	U(0,1)	1	\Timer:TimerUDB:sT32:timerdp:u1\	\Timer:TimerUDB:sT32:timerdp:u\ \/ci
Route		1	\Timer:TimerUDB:sT32:timerdp:u1.co_msb__sig\	\Timer:TimerUDB:sT32:timerdp:u\ \/co_msb
datapathcell4	U(0,0)	1	\Timer:TimerUDB:sT32:timerdp:u2\	\Timer:TimerUDB:sT32:timerdp:u\ \/ci
Route		1	\Timer:TimerUDB:sT32:timerdp:u2.co_msb__sig\	\Timer:TimerUDB:sT32:timerdp:u\ \/co_msb
datapathcell5	U(1,0)	1	\Timer:TimerUDB:sT32:timerdp:u3\	
Clock				

\Timer:TimerUDB:sT32:timerdp:u1\/z0	\Timer:TimerUDB:sT32:timerdp:u3\/ci

Type	**Location**	**Fanout**	**Instance/Net**	**Source**
datapathcell3	U(0,1)	1	\Timer:TimerUDB:sT32:timerdp:u1\	\Timer:TimerUDB:sT32:timerdp:u\ \/clock
Route		1	\Timer:TimerUDB:sT32:timerdp:u1.z0__sig\	\Timer:TimerUDB:sT32:timerdp:u\ \/z0
datapathcell4	U(0,0)	1	\Timer:TimerUDB:sT32:timerdp:u2\	\Timer:TimerUDB:sT32:timerdp:u\ \/z0i
Route		1	\Timer:TimerUDB:sT32:timerdp:u2.z0__sig\	\Timer:TimerUDB:sT32:timerdp:u\ \/z0
datapathcell5	U(1,0)	1	\Timer:TimerUDB:sT32:timerdp:u3\	\Timer:TimerUDB:sT32:timerdp:u\ \/z0i
Route		1	\Timer:TimerUDB:per_zero\	\Timer:TimerUDB:sT32:timerdp:u\ \/z0_comb
datapathcell3	U(0,1)	1	\Timer:TimerUDB:sT32:timerdp:u1\	\Timer:TimerUDB:sT32:timerdp:u\ \/cs_addr_0
Route		1	\Timer:TimerUDB:sT32:timerdp:u1.co_msb__sig\	\Timer:TimerUDB:sT32:timerdp:u\ \/co_msb
datapathcell4	U(0,0)	1	\Timer:TimerUDB:sT32:timerdp:u2\	\Timer:TimerUDB:sT32:timerdp:u\ \/ci
Route		1	\Timer:TimerUDB:sT32:timerdp:u2.co_msb__sig\	\Timer:TimerUDB:sT32:timerdp:u\ \/co_msb
datapathcell5	U(1,0)	1	\Timer:TimerUDB:sT32:timerdp:u3\	
Clock				

\Timer:TimerUDB:sT32:timerdp:u1\/z0	\Timer:TimerUDB:rstSts:stsreg\/status_0

Type	**Location**	**Fanout**	**Instance/Net**	**Source**
datapathcell3	U(0,1)	1	\Timer:TimerUDB:sT32:timerdp:u1\	\Timer:TimerUDB:sT32:timerdp:u1 \/clock
Route		1	\Timer:TimerUDB:sT32:timerdp:u1.z0__sig\	\Timer:TimerUDB:sT32:timerdp:u1 \/z0
datapathcell4	U(0,0)	1	\Timer:TimerUDB:sT32:timerdp:u2\	\Timer:TimerUDB:sT32:timerdp:u2 \/z0i
Route		1	\Timer:TimerUDB:sT32:timerdp:u2.z0__sig\	\Timer:TimerUDB:sT32:timerdp:u2 \/z0
datapathcell5	U(1,0)	1	\Timer:TimerUDB:sT32:timerdp:u3\	\Timer:TimerUDB:sT32:timerdp:u3 \/z0i
Route		1	\Timer:TimerUDB:per_zero\	\Timer:TimerUDB:sT32:timerdp:u3 \/z0_comb
macrocell11	U(1,1)	1	\Timer:TimerUDB:status_tc\	\Timer:TimerUDB:status_tc\/main_1
Route		1	\Timer:TimerUDB:status_tc\	\Timer:TimerUDB:status_tc\/q
statusicell2	U(1,0)	1	\Timer:TimerUDB:rstSts:stsreg\	
Clock				

\Timer:TimerUDB:sT32:timerdp:u1\/z0	\Timer:TimerUDB:sT32:timerdp:u2\/ci

Type	**Location**	**Fanout**	**Instance/Net**	**Source**
datapathcell3	U(0,1)	1	\Timer:TimerUDB:sT32:timerdp:u1\	\Timer:TimerUDB:sT32:timerdp:u\ \/clock
Route		1	\Timer:TimerUDB:sT32:timerdp:u1.z0__sig\	\Timer:TimerUDB:sT32:timerdp:u\ \/z0
datapathcell4	U(0,0)	1	\Timer:TimerUDB:sT32:timerdp:u2\	\Timer:TimerUDB:sT32:timerdp:u\ \/z0i
Route		1	\Timer:TimerUDB:sT32:timerdp:u2.z0__sig\	\Timer:TimerUDB:sT32:timerdp:u\ \/z0

Source				Destination
Type	**Location**	**Fanout**	**Instance/Net**	**Source**
datapathcell5	U(1,0)	1	\Timer:TimerUDB:sT32:timerdp:u3\	\Timer:TimerUDB:sT32:timerdp:u \/z0i
Route		1	\Timer:TimerUDB:per_zero\	\Timer:TimerUDB:sT32:timerdp:u \/z0_comb
datapathcell2	U(1,1)	1	\Timer:TimerUDB:sT32:timerdp:u0\	\Timer:TimerUDB:sT32:timerdp:u \/cs_addr_0
Route		1	\Timer:TimerUDB:sT32:timerdp:u0.co_msb__sig\	\Timer:TimerUDB:sT32:timerdp:u \/co_msb
datapathcell3	U(0,1)	1	\Timer:TimerUDB:sT32:timerdp:u1\	\Timer:TimerUDB:sT32:timerdp:u \/ci
Route		1	\Timer:TimerUDB:sT32:timerdp:u1.co_msb__sig\	\Timer:TimerUDB:sT32:timerdp:u \/co_msb
datapathcell4	U(0,0)	1	\Timer:TimerUDB:sT32:timerdp:u2\	
Clock				

+ Hold Subsection

+ Source Clock : CyBUS_CLK : Positive edge

+ Destination Clock : CyBUS_CLK : Positive edge

Source				Destina
\Timer:TimerUDB:sT32:timerdp:u0\/co_msb				\Timer:TimerUDB:sT32:timerdp:u1\/c
Type	**Location**	**Fanout**	**Instance/Net**	**Source**
datapathcell2	U(1,1)	1	\Timer:TimerUDB:sT32:timerdp:u0\	\Timer:TimerUDB:sT32:timerdp:u \/clock
Route		1	\Timer:TimerUDB:sT32:timerdp:u0.co_msb__sig\	\Timer:TimerUDB:sT32:timerdp:u \/co_msb
datapathcell3	U(0,1)	1	\Timer:TimerUDB:sT32:timerdp:u1\	
Clock				
\Timer:TimerUDB:sT32:timerdp:u1\/co_msb				\Timer:TimerUDB:sT32:timerdp:u2\/c
Type	**Location**	**Fanout**	**Instance/Net**	**Source**
datapathcell3	U(0,1)	1	\Timer:TimerUDB:sT32:timerdp:u1\	\Timer:TimerUDB:sT32:timerdp:u \/clock
Route		1	\Timer:TimerUDB:sT32:timerdp:u1.co_msb__sig\	\Timer:TimerUDB:sT32:timerdp:u \/co_msb
datapathcell4	U(0,0)	1	\Timer:TimerUDB:sT32:timerdp:u2\	
Clock				
\Timer:TimerUDB:sT32:timerdp:u2\/co_msb				\Timer:TimerUDB:sT32:timerdp:u3\/c
Type	**Location**	**Fanout**	**Instance/Net**	**Source**
datapathcell4	U(0,0)	1	\Timer:TimerUDB:sT32:timerdp:u2\	\Timer:TimerUDB:sT32:timerdp:u \/clock
Route		1	\Timer:TimerUDB:sT32:timerdp:u2.co_msb__sig\	\Timer:TimerUDB:sT32:timerdp:u \/co_msb
datapathcell5	U(1,0)	1	\Timer:TimerUDB:sT32:timerdp:u3\	
Clock				
\Delay_PWM:PWMUDB:status_0\/q				\Delay_PWM:PWMUDB:genblk8:stsreg\/
Type	**Location**	**Fanout**	**Instance/Net**	**Source**
macrocell27	U(3,0)	1	\Delay_PWM:PWMUDB:status_0\	\Delay_PWM:PWMUDB:status_0 \/clock_0
Route		1	\Delay_PWM:PWMUDB:status_0\	\Delay_PWM:PWMUDB:status_0\/q
statusicell1	U(3,0)	1	\Delay_PWM:PWMUDB:genblk8:stsreg\	
Clock				
\Delay_PWM:PWMUDB:genblk1:ctrlreg\/control_7				\Delay_PWM:PWMUDB:runmode_enable\/
Type	**Location**	**Fanout**	**Instance/Net**	**Source**
controlcell2	U(3,0)	1	\Delay_PWM:PWMUDB:genblk1:ctrlreg\	\Delay_PWM:PWMUDB:genblk1:ctrlreg\/clock
Route		1	\Delay_PWM:PWMUDB:control_7\	\Delay_PWM:PWMUDB:genblk1:ctrlreg\/contro
macrocell25	U(3,0)	1	\Delay_PWM:PWMUDB:runmode_enable\	
Clock				
\Sync_2:genblk1[0]:INST\/out				Count_2/clk_en
Type	**Location**	**Fanout**	**Instance/Net**	**Source**
synccell	U(3,1)	1	\Sync_2:genblk1[0]:INST\	\Sync_2:genblk1[0]:INST\/clock
Route		1	Net_302	\Sync_2:genblk1[0]:INST\/out
macrocell21	U(2,1)	1	Count_2	
Clock				
\Sync_2:genblk1[0]:INST\/out				Count_1/clk_en

Source				Destina
Type	**Location**	**Fanout**	**Instance/Net**	**Source**
synccell	U(3,1)	1	\Sync_2:genblk1[0]:INST\	\Sync_2:genblk1[0]:INST\/clock
Route		1	Net_302	\Sync_2:genblk1[0]:INST\/out
macrocell22	U(2,1)	1	Count_1	
Clock				

\Sync_2:genblk1[0]:INST\/out	Count_0/clk_en

Type	**Location**	**Fanout**	**Instance/Net**	**Source**
synccell	U(3,1)	1	\Sync_2:genblk1[0]:INST\	\Sync_2:genblk1[0]:INST\/clock
Route		1	Net_302	\Sync_2:genblk1[0]:INST\/out
macrocell23	U(2,1)	1	Count_0	
Clock				

\Delay_PWM:PWMUDB:sP8:pwmdp:u0\/cl0_comb	\Delay_PWM:PWMUDB:prevCompare1\/ma

Type	**Location**	**Fanout**	**Instance/Net**	**Source**
datapathcell1	U(3,0)	1	\Delay_PWM:PWMUDB:sP8:pwmdp:u0\	\Delay_PWM:PWMUDB:sP8:pwmdp:u0\/clock
Route		1	\Delay_PWM:PWMUDB:cmp1_less\	\Delay_PWM:PWMUDB:sP8:pwmdp:u0\/cl0_comb
macrocell26	U(3,0)	1	\Delay_PWM:PWMUDB:prevCompare1\	
Clock				

\Delay_PWM:PWMUDB:sP8:pwmdp:u0\/cl0_comb	Net_938/main_2

Type	**Location**	**Fanout**	**Instance/Net**	**Source**
datapathcell1	U(3,0)	1	\Delay_PWM:PWMUDB:sP8:pwmdp:u0\	\Delay_PWM:PWMUDB:sP8:pwmdp:u0\/clock
Route		1	\Delay_PWM:PWMUDB:cmp1_less\	\Delay_PWM:PWMUDB:sP8:pwmdp:u0\/cl0_comb
macrocell28	U(3,0)	1	Net_938	
Clock				

+ Asynchronous Clock Crossing Section

+ Source Clock \ADC_DelSig_1:DEC\/interrupt

+ Destination Clock CyBUS_CLK

Source	Destination
\Sync_1:genblk1[2]:INST\/out	\Timer:TimerUDB:sT32:timerdp:u3\/f0_load

Type	**Location**	**Fanout**	**Instance/Net**	**Source**
synccell	U(2,0)	1	\Sync_1:genblk1[2]:INST\	\Sync_1:genblk1[2]:INST\/clock_n
Route		1	Count_retard_2	\Sync_1:genblk1[2]:INST\/out
macrocell10	U(1,1)	1	\Timer:TimerUDB:capt_fifo_load\	\Timer:TimerUDB:capt_fifo_load\/main_1
Route		1	\Timer:TimerUDB:capt_fifo_load\	\Timer:TimerUDB:capt_fifo_load\/q
datapathcell5	U(1,0)	1	\Timer:TimerUDB:sT32:timerdp:u3\	
Clock				

\Sync_1:genblk1[2]:INST\/out	\Timer:TimerUDB:rstSts:stsreg\/status_1

Type	**Location**	**Fanout**	**Instance/Net**	**Source**
synccell	U(2,0)	1	\Sync_1:genblk1[2]:INST\	\Sync_1:genblk1[2]:INST\/clock_n
Route		1	Count_retard_2	\Sync_1:genblk1[2]:INST\/out
macrocell10	U(1,1)	1	\Timer:TimerUDB:capt_fifo_load\	\Timer:TimerUDB:capt_fifo_load\/main_1
Route		1	\Timer:TimerUDB:capt_fifo_load\	\Timer:TimerUDB:capt_fifo_load\/q
statusicell2	U(1,0)	1	\Timer:TimerUDB:rstSts:stsreg\	
Clock				

\Sync_1:genblk1[2]:INST\/out	\Timer:TimerUDB:sT32:timerdp:u0\/f0_load

Type	**Location**	**Fanout**	**Instance/Net**	**Source**
synccell	U(2,0)	1	\Sync_1:genblk1[2]:INST\	\Sync_1:genblk1[2]:INST\/clock_n
Route		1	Count_retard_2	\Sync_1:genblk1[2]:INST\/out
macrocell10	U(1,1)	1	\Timer:TimerUDB:capt_fifo_load\	\Timer:TimerUDB:capt_fifo_load\/main_1
Route		1	\Timer:TimerUDB:capt_fifo_load\	\Timer:TimerUDB:capt_fifo_load\/q
datapathcell2	U(1,1)	1	\Timer:TimerUDB:sT32:timerdp:u0\	
Clock				

\Sync_1:genblk1[2]:INST\/out	\Timer:TimerUDB:sT32:timerdp:u2\/f0_load

Type	**Location**	**Fanout**	**Instance/Net**	**Source**

Source				Destination	
Type	**Location**	**Fanout**	**Instance/Net**	**Source**	
synccell	U(2,0)	1	\Sync_1:genblk1[2]:INST\	\Sync_1:genblk1[2]:INST\/clock_n	\Sync_1
Route		1	Count_retard_2	\Sync_1:genblk1[2]:INST\/out	\Timer:T
macrocell10	U(1,1)	1	\Timer:TimerUDB:capt_fifo_load\	\Timer:TimerUDB:capt_fifo_load\/main_1	\Timer:T
Route		1	\Timer:TimerUDB:capt_fifo_load\	\Timer:TimerUDB:capt_fifo_load\/q	\Timer:T \/f0_loa
datapathcell4	U(0,0)	1	\Timer:TimerUDB:sT32:timerdp:u2 \		SETUP
Clock					Skew

\Sync_1:genblk1[1]:INST\/out	\Timer:TimerUDB:sT32:timerdp:u3\/f0_load

Type	**Location**	**Fanout**	**Instance/Net**	**Source**	
synccell	U(2,1)	1	\Sync_1:genblk1[1]:INST\	\Sync_1:genblk1[1]:INST\/clock_n	\Sync_1
Route		1	Count_retard_1	\Sync_1:genblk1[1]:INST\/out	\Timer:T
macrocell10	U(1,1)	1	\Timer:TimerUDB:capt_fifo_load\	\Timer:TimerUDB:capt_fifo_load\/main_2	\Timer:T
Route		1	\Timer:TimerUDB:capt_fifo_load\	\Timer:TimerUDB:capt_fifo_load\/q	\Timer:T \/f0_loa
datapathcell5	U(1,0)	1	\Timer:TimerUDB:sT32:timerdp:u3 \		SETUP
Clock					Skew

\Sync_1:genblk1[1]:INST\/out	\Timer:TimerUDB:rstSts:stsreg\/status_1

Type	**Location**	**Fanout**	**Instance/Net**	**Source**	
synccell	U(2,1)	1	\Sync_1:genblk1[1]:INST\	\Sync_1:genblk1[1]:INST\/clock_n	\Sync_1:G
Route		1	Count_retard_1	\Sync_1:genblk1[1]:INST\/out	\Timer:Ti
macrocell10	U(1,1)	1	\Timer:TimerUDB:capt_fifo_load\	\Timer:TimerUDB:capt_fifo_load\/main_2	\Timer:Ti
Route		1	\Timer:TimerUDB:capt_fifo_load\	\Timer:TimerUDB:capt_fifo_load\/q	\Timer:Ti
statusicell2	U(1,0)	1	\Timer:TimerUDB:rstSts:stsreg\		SETUP
Clock					Skew

\Sync_1:genblk1[0]:INST\/out	\Timer:TimerUDB:sT32:timerdp:u3\/f0_load

Type	**Location**	**Fanout**	**Instance/Net**	**Source**	
synccell	U(2,1)	1	\Sync_1:genblk1[0]:INST\	\Sync_1:genblk1[0]:INST\/clock_n	\Sync_1
Route		1	Count_retard_0	\Sync_1:genblk1[0]:INST\/out	\Timer:T
macrocell10	U(1,1)	1	\Timer:TimerUDB:capt_fifo_load\	\Timer:TimerUDB:capt_fifo_load\/main_3	\Timer:T
Route		1	\Timer:TimerUDB:capt_fifo_load\	\Timer:TimerUDB:capt_fifo_load\/q	\Timer:T \/f0_loa
datapathcell5	U(1,0)	1	\Timer:TimerUDB:sT32:timerdp:u3 \		SETUP
Clock					Skew

\Sync_1:genblk1[0]:INST\/out	\Timer:TimerUDB:rstSts:stsreg\/status_1

Type	**Location**	**Fanout**	**Instance/Net**	**Source**	
synccell	U(2,1)	1	\Sync_1:genblk1[0]:INST\	\Sync_1:genblk1[0]:INST\/clock_n	\Sync_1:G
Route		1	Count_retard_0	\Sync_1:genblk1[0]:INST\/out	\Timer:Ti
macrocell10	U(1,1)	1	\Timer:TimerUDB:capt_fifo_load\	\Timer:TimerUDB:capt_fifo_load\/main_3	\Timer:Ti
Route		1	\Timer:TimerUDB:capt_fifo_load\	\Timer:TimerUDB:capt_fifo_load\/q	\Timer:Ti
statusicell2	U(1,0)	1	\Timer:TimerUDB:rstSts:stsreg\		SETUP
Clock					Skew

\Sync_1:genblk1[2]:INST\/out	\Timer:TimerUDB:sT32:timerdp:u1\/f0_load

Type	**Location**	**Fanout**	**Instance/Net**	**Source**	
synccell	U(2,0)	1	\Sync_1:genblk1[2]:INST\	\Sync_1:genblk1[2]:INST\/clock_n	\Sync_1
Route		1	Count_retard_2	\Sync_1:genblk1[2]:INST\/out	\Timer:T
macrocell10	U(1,1)	1	\Timer:TimerUDB:capt_fifo_load\	\Timer:TimerUDB:capt_fifo_load\/main_1	\Timer:T
Route		1	\Timer:TimerUDB:capt_fifo_load\	\Timer:TimerUDB:capt_fifo_load\/q	\Timer:T \/f0_loa
datapathcell3	U(0,1)	1	\Timer:TimerUDB:sT32:timerdp:u1 \		SETUP
Clock					Skew

\Sync_1:genblk1[1]:INST\/out	\Timer:TimerUDB:sT32:timerdp:u0\/f0_load

Type	**Location**	**Fanout**	**Instance/Net**	**Source**	
synccell	U(2,1)	1	\Sync_1:genblk1[1]:INST\	\Sync_1:genblk1[1]:INST\/clock_n	\Sync_1
Route		1	Count_retard_1	\Sync_1:genblk1[1]:INST\/out	\Timer:T
macrocell10	U(1,1)	1	\Timer:TimerUDB:capt_fifo_load\	\Timer:TimerUDB:capt_fifo_load\/main_2	\Timer:T
Route		1	\Timer:TimerUDB:capt_fifo_load\	\Timer:TimerUDB:capt_fifo_load\/q	\Timer:T \/f0_loa
datapathcell2	U(1,1)	1	\Timer:TimerUDB:sT32:timerdp:u0 \		SETUP
Clock					Skew

+ Clock To Output Section

+ CyBUS_CLK

Source					Destinati
\Control_LED:Sync:ctrl_reg\/control_0					LED_15_5(0)_PAD
Type	**Location**	**Fanout**	**Instance/Net**	**Source**	
controlcell11	U(1,0)	1	\Control_LED:Sync:ctrl_reg\	\Control_LED:Sync:ctrl_reg\/busclk	\Control_LED:Sync
Route		1	Net_35	\Control_LED:Sync:ctrl_reg\/control_0	LED_15_5(0)/pin_i
iocell3	P6[0]	1	LED_15_5(0)	LED_15_5(0)/pin_input	LED_15_5(0)/pad_c
Route		1	LED_15_5(0)_PAD	LED_15_5(0)/pad_out	LED_15_5(0)_PAD
Clock					Clock path delay

+ Asynchronous Constraints

+ Recovery

+ Source Clock : CyBUS_CLK : Positive edge(Required Frequency 24 MHz)

+ Destination Clock : CyBUS_CLK : Positive edge(Required Frequency 24 MHz)

Path Delay Requirement : 41.6667ns(24 MHz)

Source				Destination
\Control_Reset_Timer:Sync:ctrl_reg\/control_0				\Timer:TimerUDB:rstSts:stsreg\/reset
Type	**Location**	**Fanout**	**Instance/Net**	**Source**
controlcell15	U(0,1)	1	\Control_Reset_Timer:Sync:ctrl_reg\	\Control_Reset_Timer:Sync:ctrl_reg\/busc
Route		1	Net_380	\Control_Reset_Timer:Sync:ctrl_reg\/cont
statusicell2	U(1,0)	1	\Timer:TimerUDB:rstSts:stsreg\	
Clock				

+ Removal

+ Source Clock : CyBUS_CLK : Positive edge

+ Destination Clock : CyBUS_CLK : Positive edge

Source				De
\Control_Reset_Timer:Sync:ctrl_reg\/control_0				\Timer:TimerUDB:rstSts:stsr
Type	**Location**	**Fanout**	**Instance/Net**	**Source**
controlcell15	U(0,1)	1	\Control_Reset_Timer:Sync:ctrl_reg\	\Control_Reset_Timer:Sync:ctrl_reg\/busc
Route		1	Net_380	\Control_Reset_Timer:Sync:ctrl_reg\/cont
statusicell2	U(1,0)	1	\Timer:TimerUDB:rstSts:stsreg\	
Clock				