Application Note

Cell Supervision Circuit (CSC) using TLE9012AQU & TLE9015QU

About this document

Application schematic for multi-cell monitoring and balancing ICs TLE9012AQU & TLE9015QU designed for Li-ion battery packs used in hybrid electric vehicles (HEV), plug-in hybrid electric vehicles (PHEV), battery electric vehicles (BEV) as well as in stationary Lithium-Ion batteries.

Components:

- RC filter for 16 bit high resolution ADC measurement
- Balancing resistors allowing passive balancing up to 150 mA balancing current
- EMC network for BCI robustness
- iso UART Communication Interface requires external circuit for robust serial communication between CSCs with up to 2 Mbps
- Buffer caps and other supporting components at the CSC input pins

Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

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1 Application schematic of one Cell Supervision Circuit (CSC)

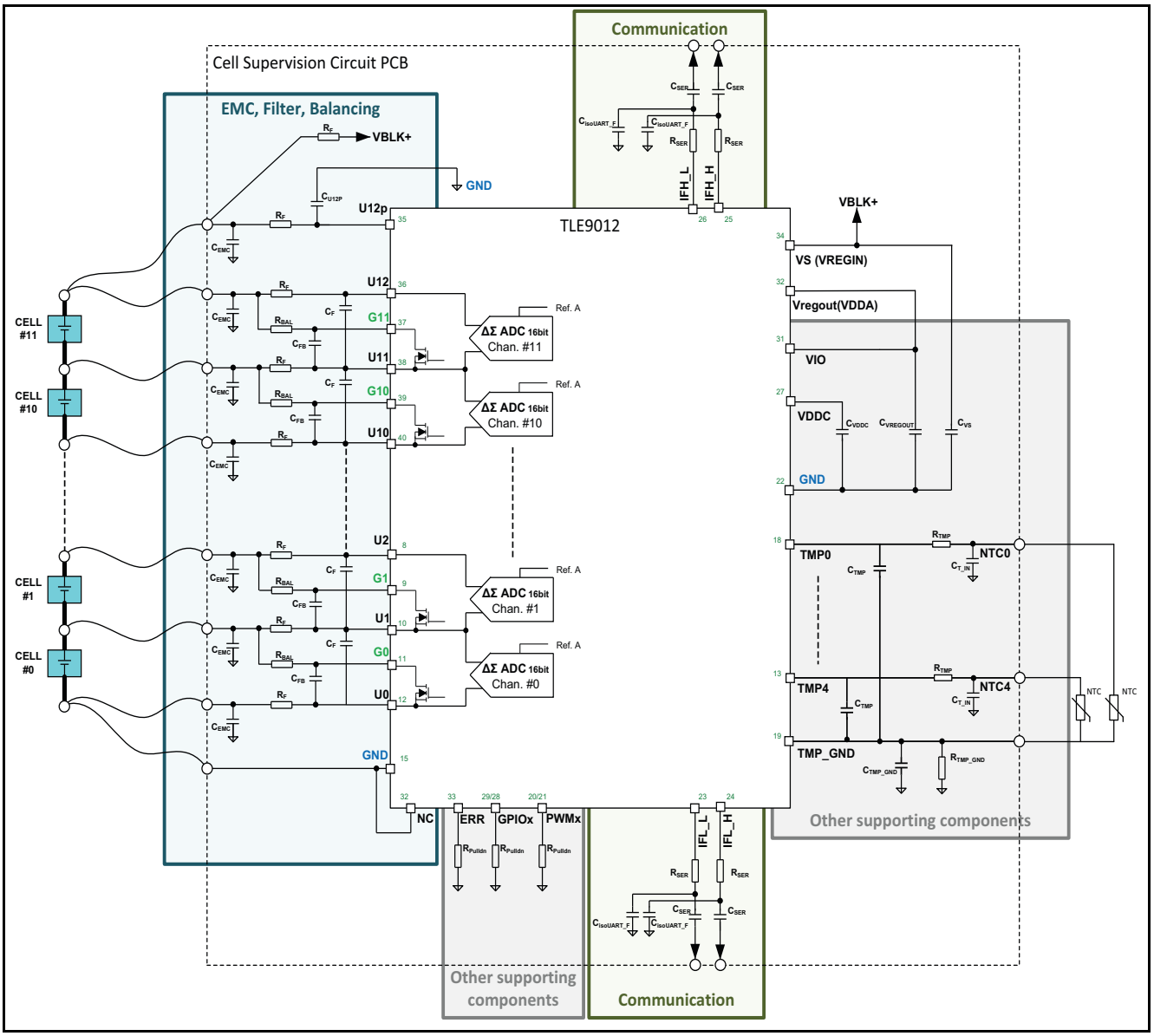

Figure 1 Schematic of one CSC

1.1 BOM - EMC, filter and balancing network

Table 1 BOM - EMC, filter and balancing network

		Status as is on Evaluation-Board			Possible optimization for series development	Layout hints and general comments
	Pin function	**Value**	**Package**	**Characteristics**		
C_F	Filter capacitors	330 nF	SM0603	16 V, Open Mode principal preferred	Other voltage characteristics e.g. 10 V also possible and can be reduced to e.g. 0402.	Should be placed as close as possible to the U_x pins, especially important for C_F between U11 and U12 (see **Chapter 1.4**).
C_{FB}	Filter capacitors	100 nF	SM0402	50 V, Open Mode principal preferred	Other voltage characteristics e.g. 10 V also possible.	Please adjust this capacitor value accordingly if you want to change the balancing resistor value to keep τ constant.
R_F	Filter resistors	5.1 Ω	SM1206	Anti surge	Can be reduced to e.g. 0805. Please take maximum peak currents during hot plug event into account when choosing resistor package and type.	ADC input impedance during measurement conversion is typically 200 kΩ. This value can be used to calculate the voltage drop over that resistor during measurement conversion.
C_{U12P}	Filter capacitor	100 nF	SM0805	100 V, Open Mode principal preferred	Can be reduced to e.g. 0603.	
C_{EMC}	EMC network	1 nF	SM0805	100 V, Open Mode principal preferred	Can be reduced to e.g. 0603.	Optional. This capacitor can be helpful for EMC. It depends on the system setup incl. board layout, BCI injection point etc. whether this is really needed. The capacitor should be placed close to the connector of the sensing wire.

Application schematic of one Cell Supervision Circuit (CSC)

Table 1 BOM - EMC, filter and balancing network

		Status as is on Evaluation-Board			Possible optimization for series development	Layout hints and general comments
	Pin function	**Value**	**Package**	**Characteristics**		
R_{BAL}	Balancing resistors	56 Ω	SM1210		Resistor value in parallel setup is made for max. 150 mA balancing current. Can be optimized based on balancing current requirements.	
R_{VS}	Input resistor VS	5.1 Ω	SM1206	Anti-surge	Can be reduced to e.g. 0805. Please take maximum peak currents during hot plug event into account when choosing resistor package and type.	

1.2 BOM communication circuit between Cell Supervision Circuit

Table 2 BOM communication circuit between Cell Supervision Circuit

		Status as is on Evaluation-Board			Possible optimization for series development	Layout hints and general comments
	Pin function	**Value**	**Package**	**Characteristics**		
$C_{isoUART\_F}$	EMC network	220 pF	SM0603	100 V	Can be reduced to e.g. 10 V and different package e.g. 0402.	The $C_{isoUART\_F}$ should be placed close to C_{EMC} (if used) and the common GND path should be as short as possible.
R_{SER}	iso UART network	39 Ω	SM0805			Please place this resistor close to the IC.
C_{SER}	iso UART network	1 nF	SM1206	500 V, ± 5 %, C0G	Can be reduced to e.g. 0805. It depends on the battery system requirement whether a 500 V voltage rating is needed. With no additional battery system requirement 100 V is sufficient.	Symmetric routing of communication lines improves the EMC robustness. For an improved EMC robustness we propose C0G capacitors with ±5% tolerance.

1.3 BOM of other supporting components for Cell Supervision Circuit

Table 3 BOM of other supporting components for Cell Supervision Circuit

		Status as is on Evaluation-Board			Possible optimization for series development	Layout hints and general comments
	Pin function	**Value**	**Package**	**Characteristics**		
C_{VS}	Buffer capacitor VS	100 nF	SM0805	100 V	Can be reduced to e.g. 0603.	Should be placed as close as possible to the VS pin.
C_{VDDC}	Buffer capacitor VDDC	330 nF	SM0603	25 V	Can be reduced to e.g. 10 V and can be reduced to e.g. 0402.	Should be placed as close as possible to the VDDC pin.
$C_{VREGOUT}$	Buffer capacitor	100 nF	SM0805	50 V	Can be reduced to e.g. 10 V and can be reduced to e.g. 0603.	Should be placed as close as possible to the VREGOUT pin.
C_{T_IN}	Input capacitor	4.7 nF	SM0603	50 V	Can be reduced to e.g. 10 V and can be reduced to e.g. 0402.	Should be placed as close as possible to the NTC connector pins.
C_{TMP_GND}	Temperature capacitor	10 nF	SM0603	50 V	Can be reduced to e.g. 10 V and can be reduced to e.g. 0402.	Should be placed as close as possible to the TMP_GND pin.
R_{TMP_GND}	Temperature resistor	100 Ω	SM0603		Can be reduced to e.g. 0402.	
R_{TMP}	Temperature filter	100 Ω	SM1206		Optional temperature filter resistor. Can be reduced to e.g. 0603.	
C_{TMP}	Temperature filter	10 nF	SM0603	50 V	Optional temperature filter capacitor. Can be reduced to e.g. 0402, 10 V.	Should be placed as close as possible to the TMPx pins.
R_{Pulldn}	Pull down resistor	33 kΩ	SM0603		Can be reduced to e.g. 0402.	

1.4 Layout guideline

The filter capacitors C_F should be placed as close as possible to the TLE9012AQU pins. This is especially important for channel #11 to enable an accurate voltage measurement. **Figure 2** shows an example where the filter capacitor should be placed next to the IC pins (U11, U12).

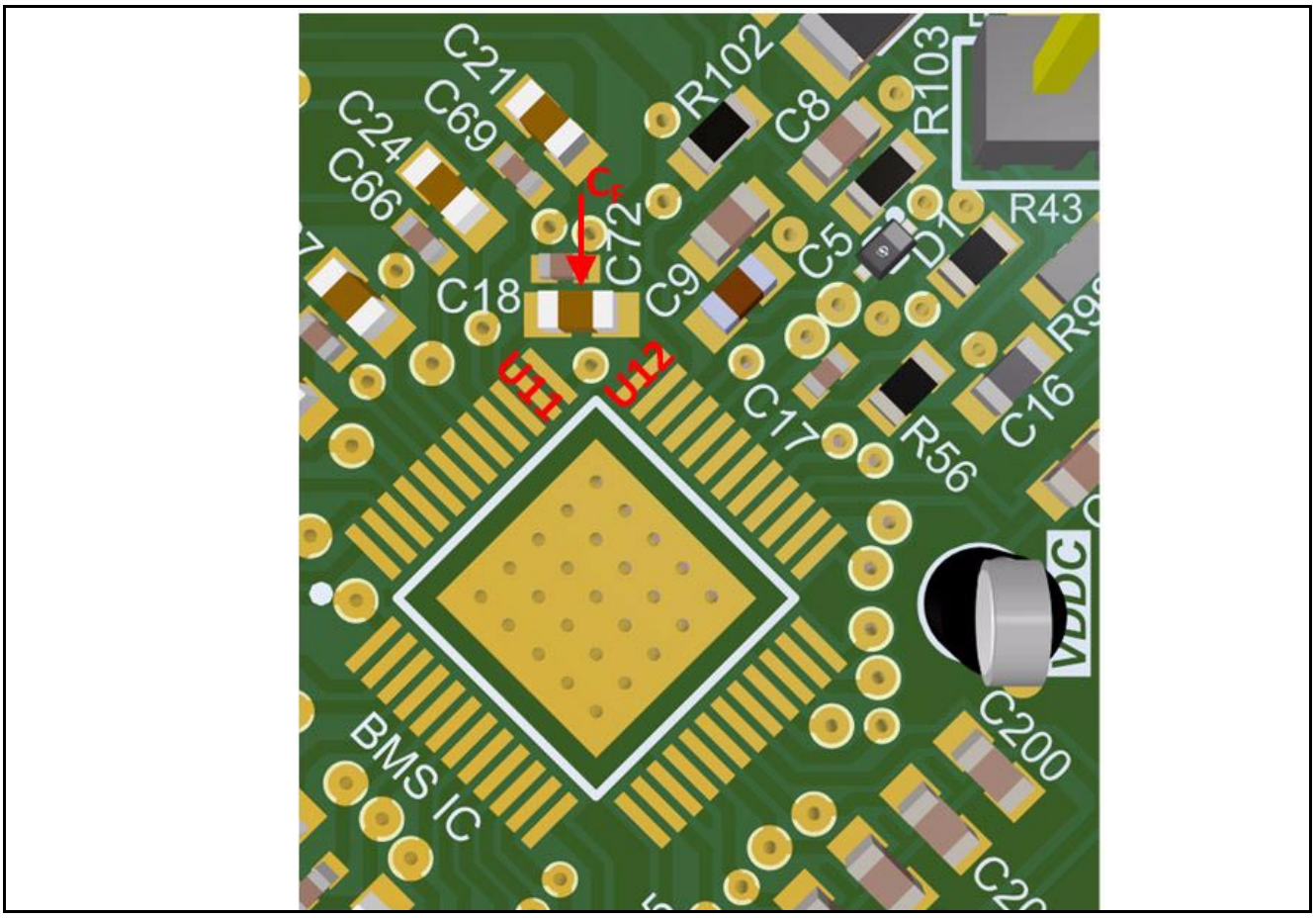

Figure 2 Channel 11 layout guideline

Furthermore, VS and U12 should be separated by routing them away from each other. This is necessary to reduce disturbances (see **Figure 3**).

Application schematic of one Cell Supervision Circuit (CSC)

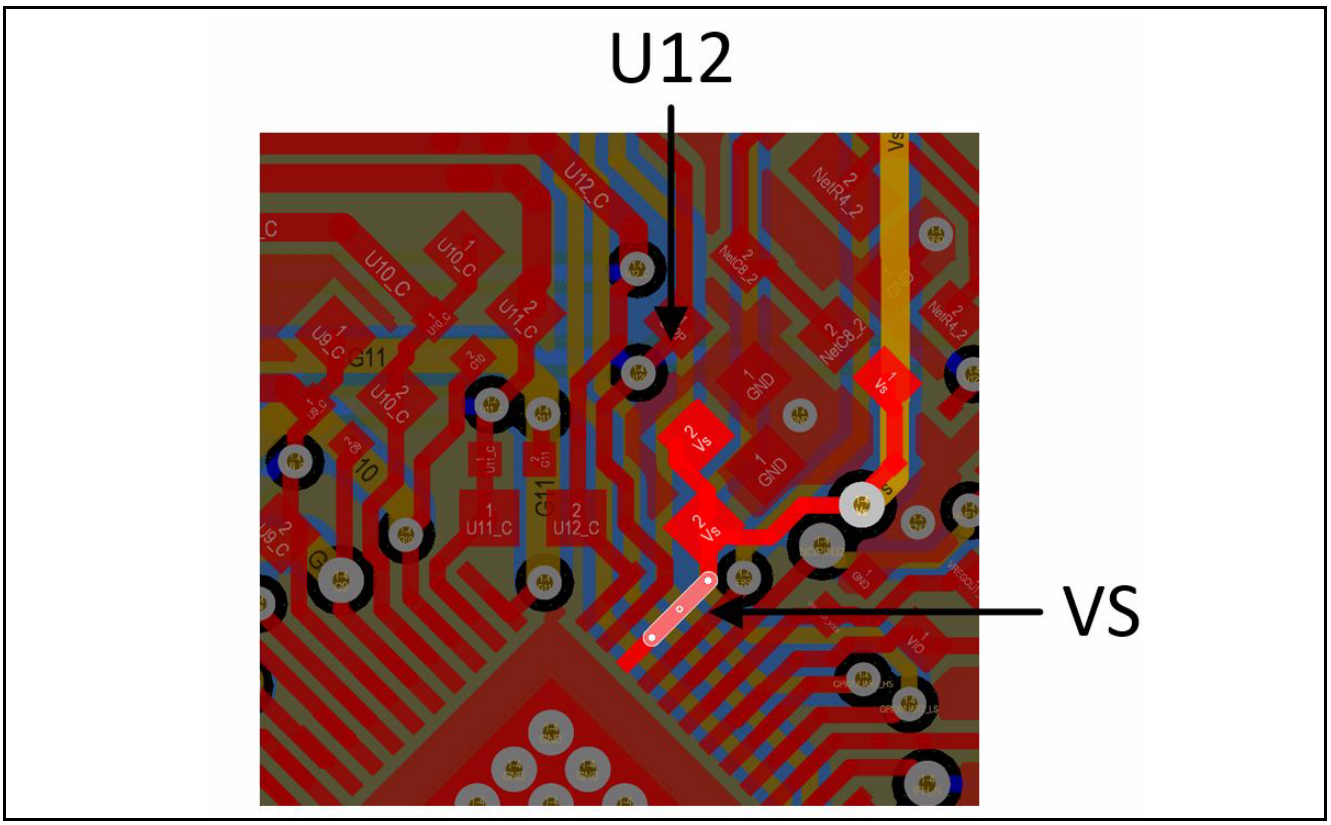

Figure 3 Routing VS and U12

1.5 Guidance for unused pins

1.5.1 Unused input pins

All unused input pins shall be connected to GND in the following way.

Input pins:

- TMP0 … TMP4: directly to GND
- PWM1, PWM0: 33 kΩ to GND (package size e.g. 0603), resistor can be shared.
- GPIO0/UART_LS, GPIO1/UART_HS: 33 kΩ to GND (package size e.g. 0603), resistor from PWM0, PWM1 can be shared here.

1.5.2 Unused output pins

All unused output pins shall stay left open.

Output pins:

- ERR

1.5.3 NC Pin 32

The NC pin 32 shall be connected to GND.

1.6 Use of CSC with less than 12 cells

Unused channels shall be connected to the negative potential of the lowest used cell. The connection can be made either directly at the pin (**Figure 4**) or at the connector (**Figure 5**).

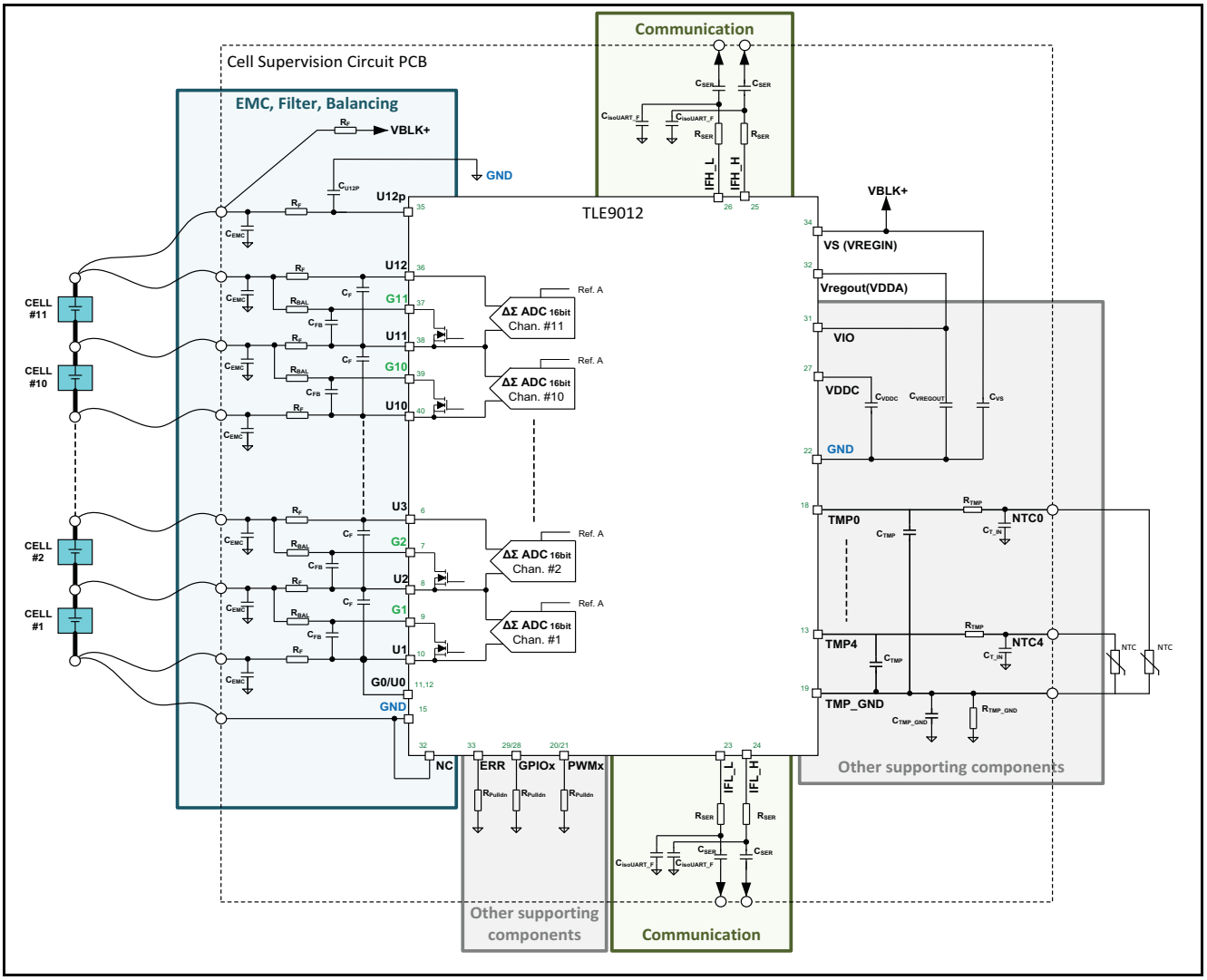

Figure 4 TLE9012AQU (12 Channel) CSCs connected to 11 cells (Pin)

Application schematic of one Cell Supervision Circuit (CSC)

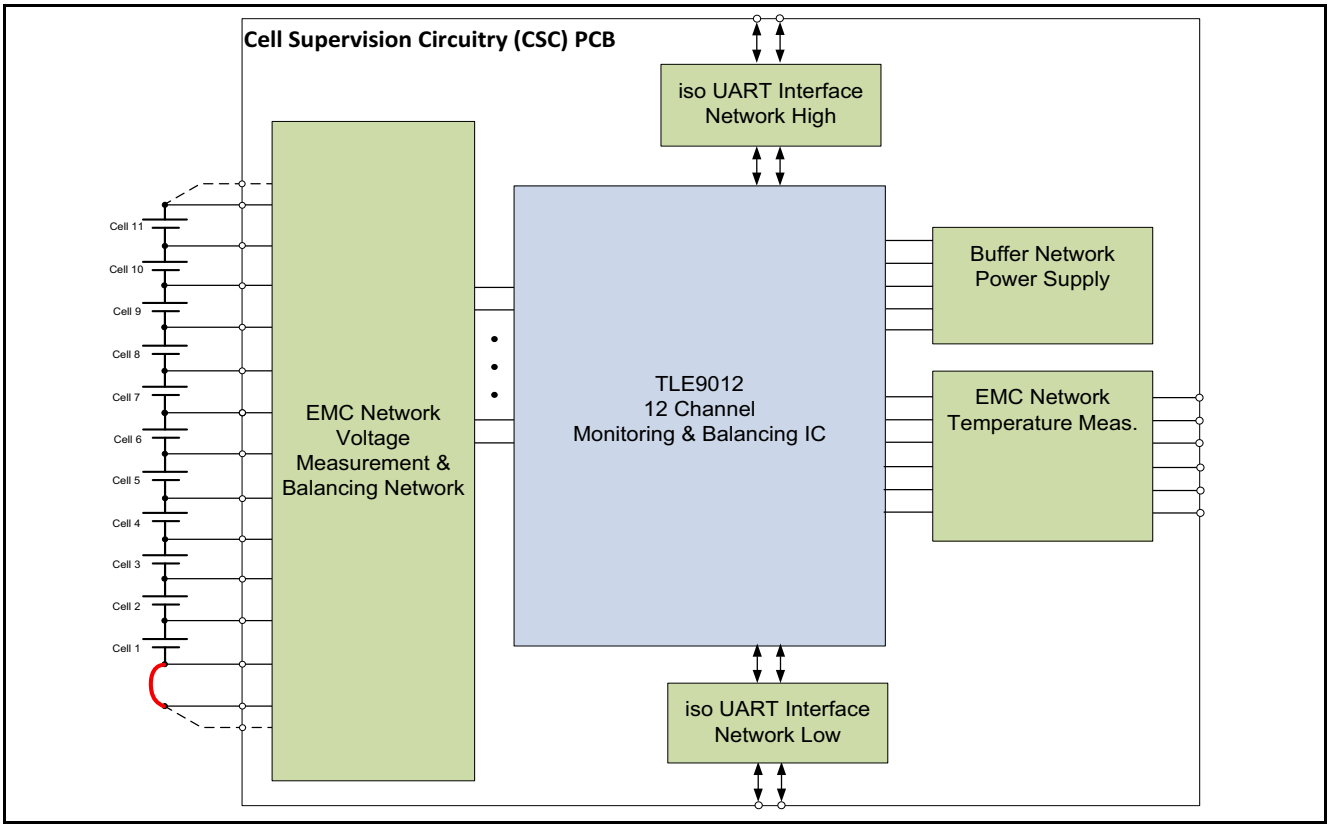

Figure 5 TLE9012AQU (12 Channel) CSCs connected to 11 cells (Connector)

2 Application schematic transceiver circuit

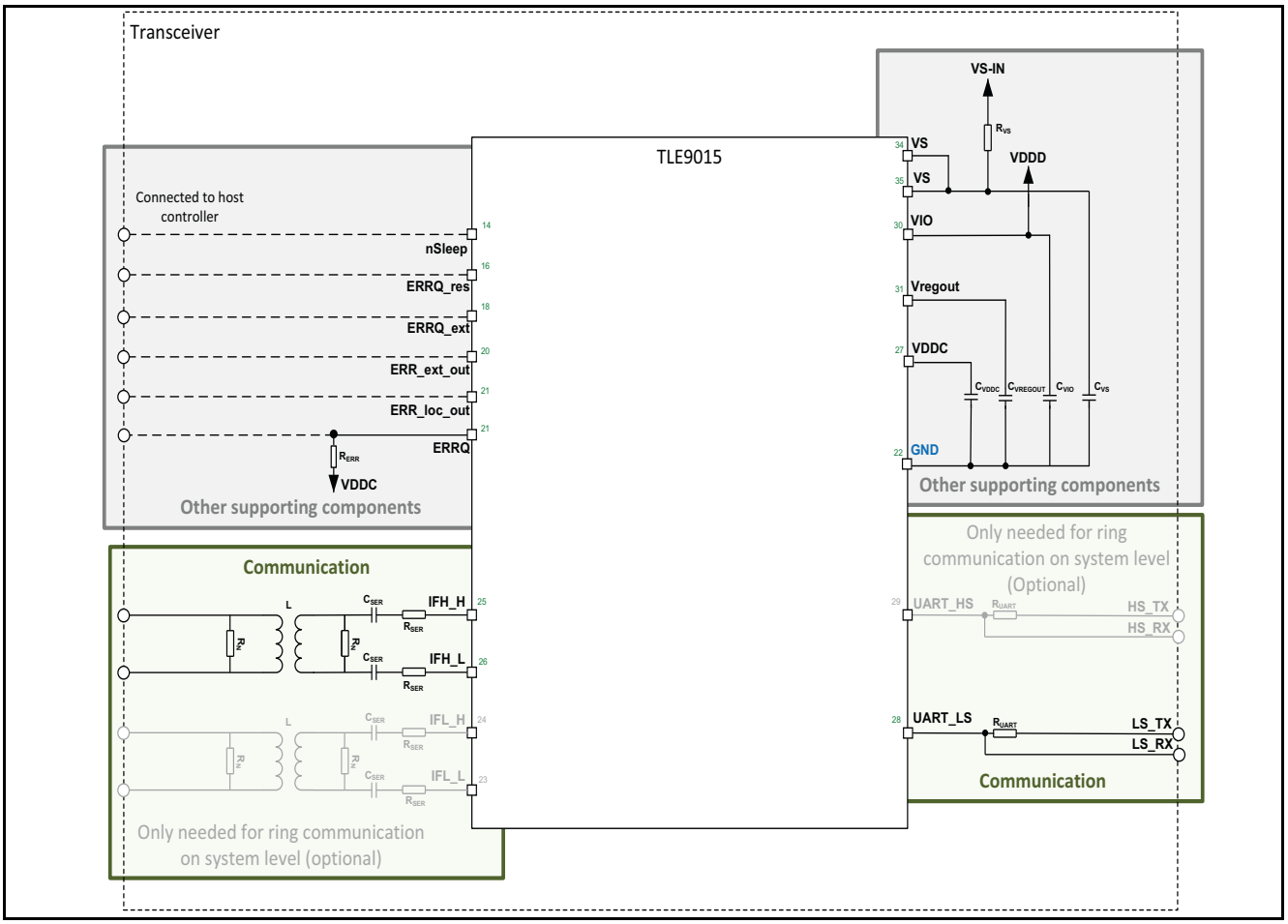

Figure 6 Schematic of the transceiver

2.1 BOM communication circuit

Table 4 BOM communication circuit

		Status as is on Evaluation-Board			Possible optimization for series development	Layout hints and general comments
	Pin function	**Value**	**Package**	**Characteristics**		
R_{SER}	iso UART network	39 Ω	SM0805			
C_{SER}	iso UART network	1 nF	SM1206	500 V	100 V can be used since transformer is making the galvanic isolation; 0805 package can be used.	
R_N	iso UART network	510 Ω	SM0805			

Application schematic transceiver circuit

Table 4 BOM communication circuit

		Status as is on Evaluation-Board			Possible optimization for series development	Layout hints and general comments
	Pin function	**Value**	**Package**	**Characteristics**		
L	Transformer			Sumida CEP99P, Pulse HM2106ZNL		
R_{UART}	UART network	1 kΩ	SM0603			

2.2 BOM of other supporting components

Table 5 BOM communication circuit

		Status as is on Evaluation-Board			Possible optimization for series development	Layout hints and general comments
	Pin function	**Value**	**Package**	**Characteristics**		
$C_{VREGOUT}$	Buffer capacitor	100 nF	SM0603	50 V	Can be reduced to e.g. 0402.	Should be placed as close as possible to the VREGOUT pin.
C_{VDDC}	Buffer capacitor	330 nF	SM0805	25 V	Can be reduced to e.g. 10 V and can be reduced to e.g. 0402.	Should be placed as close as possible to the VDDC pin.
C_{VIO}	Buffer capacitor	100 nF	SM0805	50 V	Can be reduced to e.g. 10 V and can be reduced to e.g. 0603.	Should be placed as close as possible to the VIO pin.
C_{VS}	Buffer capacitor	100 nF	SM0805	50 V		Should be placed as close as possible to the VS pin.
R_{VS}	Buffer resistor	5.1 Ω	SM1206			
R_{ERR}	Error output	1.5 kΩ	SM0402			

3 CSC Infineon evaluation board

Physical dimensions: (9.2 x 9.0) cm

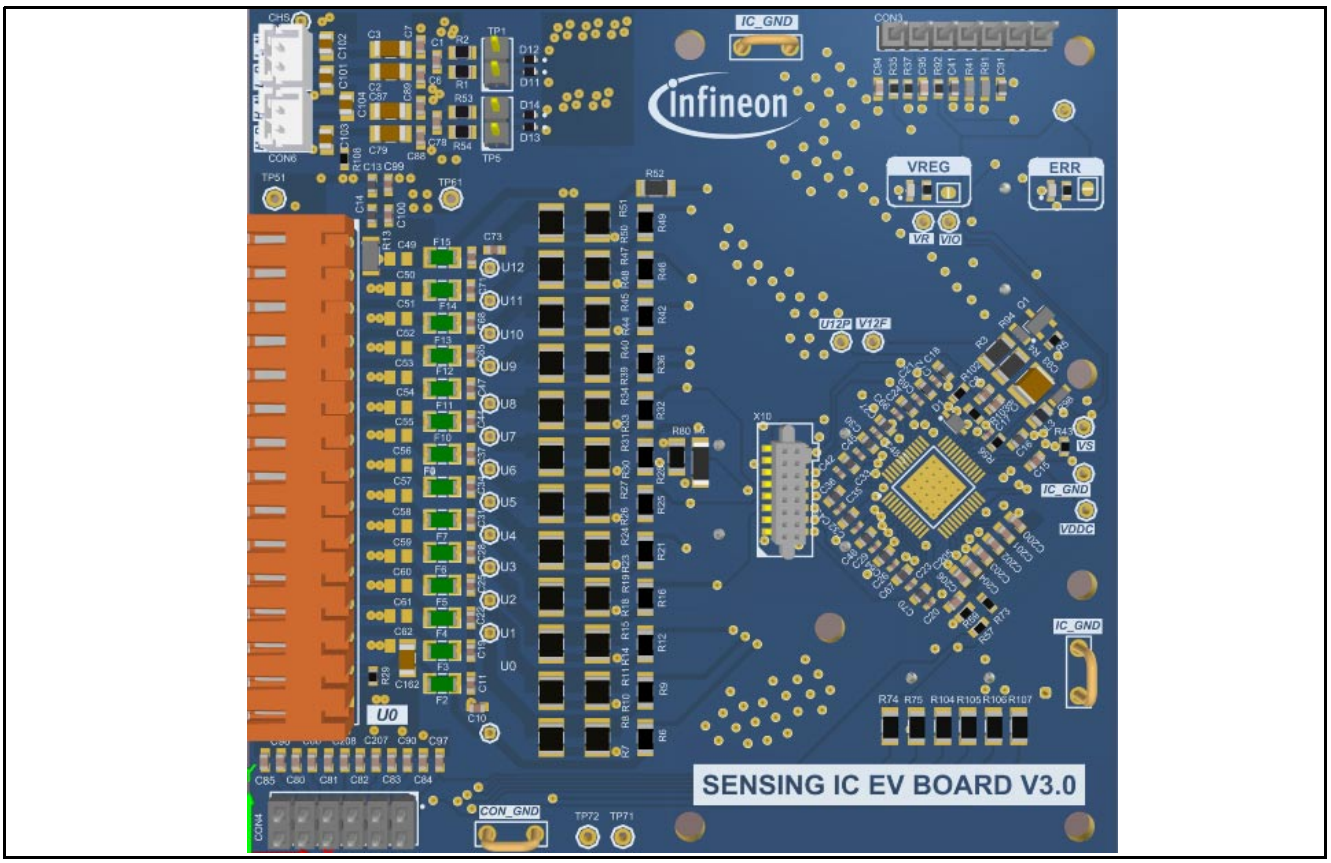

Figure 7 3D Image of CSC evaluation board

4 Transceiver Infineon evaluation board

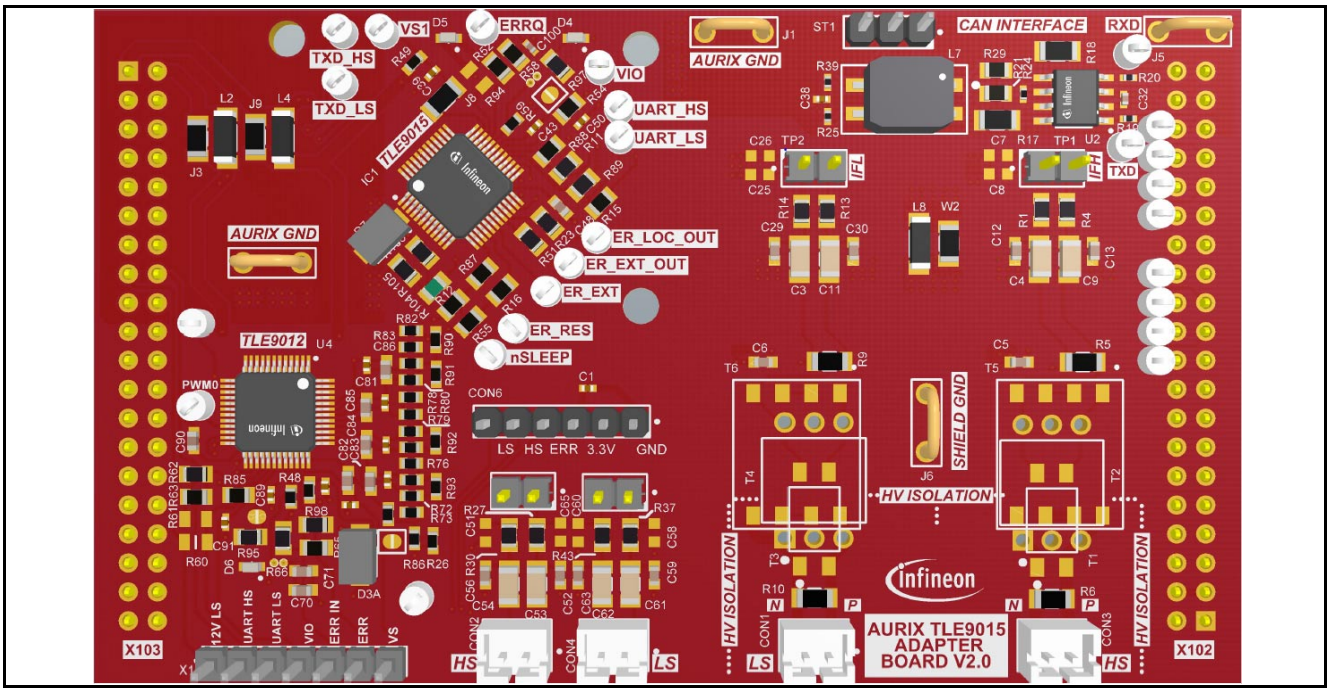

Figure 8 3D Image of transceiver evaluation board

5 Typical chip performance

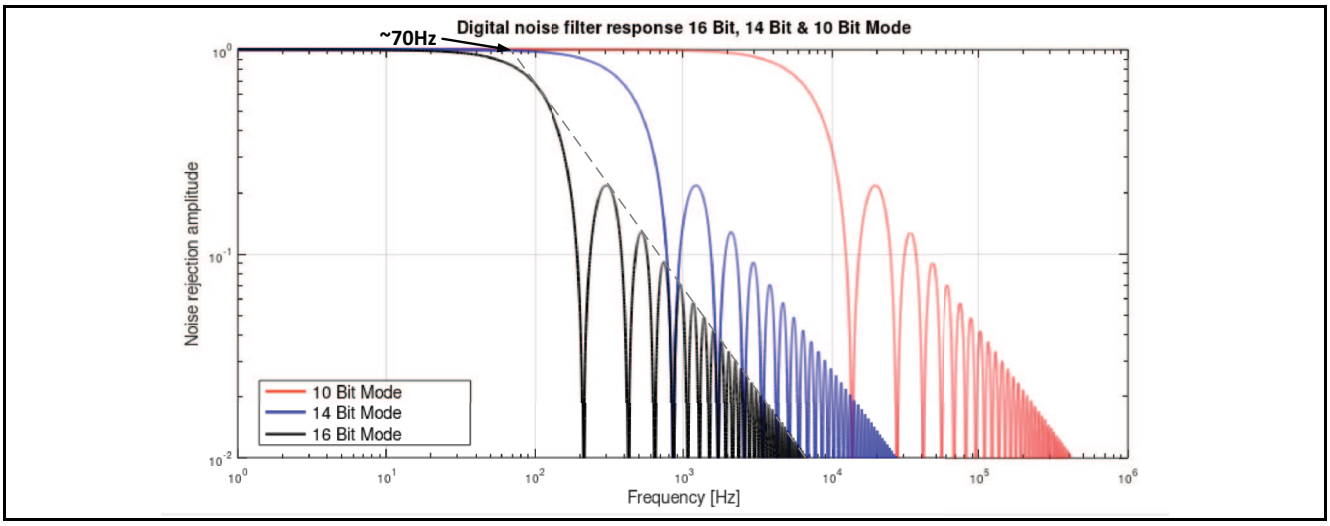

Figure 9 Digital noise filter response

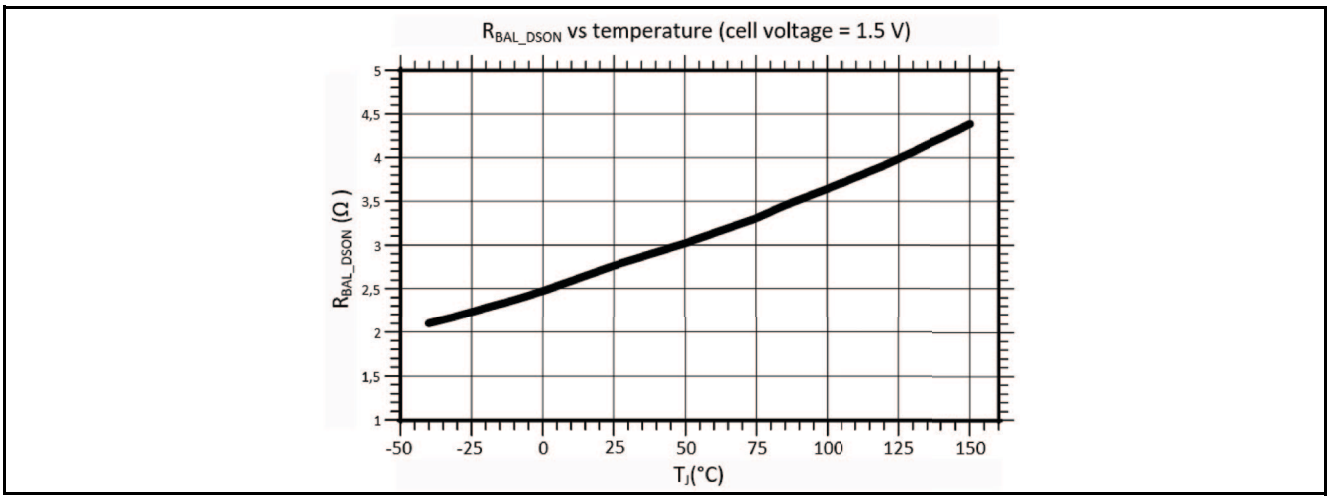

Figure 10 Typical R_{BAL_DSON} vs temperature

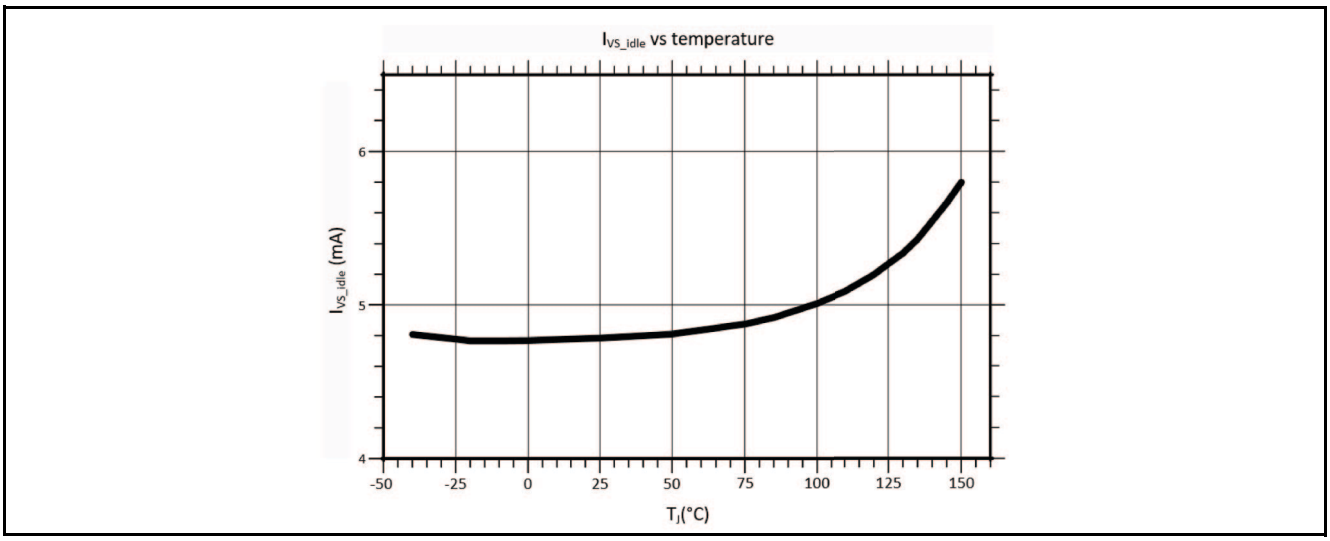

Figure 11 Typical I_{VS_idle} vs temperature

6 EEPROM

If additional memory is required, an EEPROM can be connected to the TLE9012AQU. The two GPIO pins of the TLE9012AQU can be used for the communication with the memory using bit banging to emulate I2C.

Memory requirements:

- I2C interface
- Max. operating current: I_{VIO_comm} [1)]
- Supply voltage: $V_{Vregout}$ [1)]
- The minimum clock frequency must be taken into account when choosing the memory. Since the emulation of I2C using bit banging is slow, the minimum clock frequency of the memory should be small.

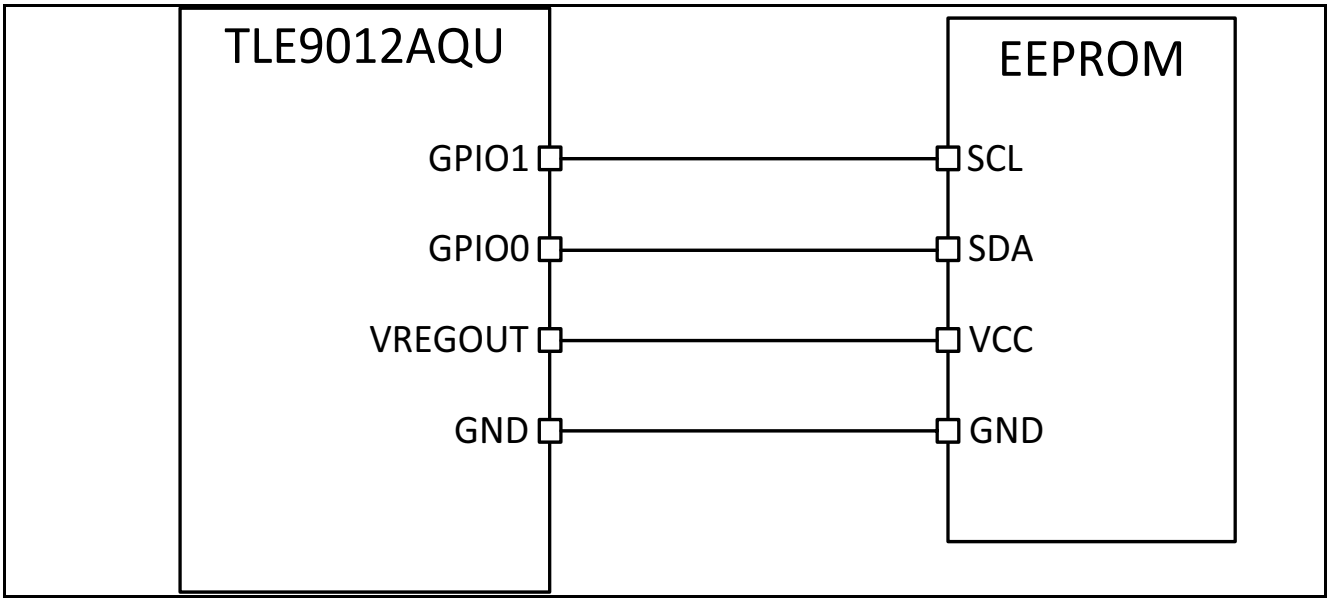

Figure 12 TLE9012AQU connected to EEPROM

Note: Instead of using the VREGOUT pin to supply the EEPROM, a thrid GPIO pin (e.g. PWM0) can be used to supply the memory. If the pin is set to HIGH, the memory is supplied. In case of the pin is set to LOW, the memory is removed from the supply. This is beneficial to reduce the supply current.

Depending on the EEPROM used, a defined bit sequence as well as the memory address and the data to be stored must be sent. An example sequence for a write is shown in **Figure 13**.

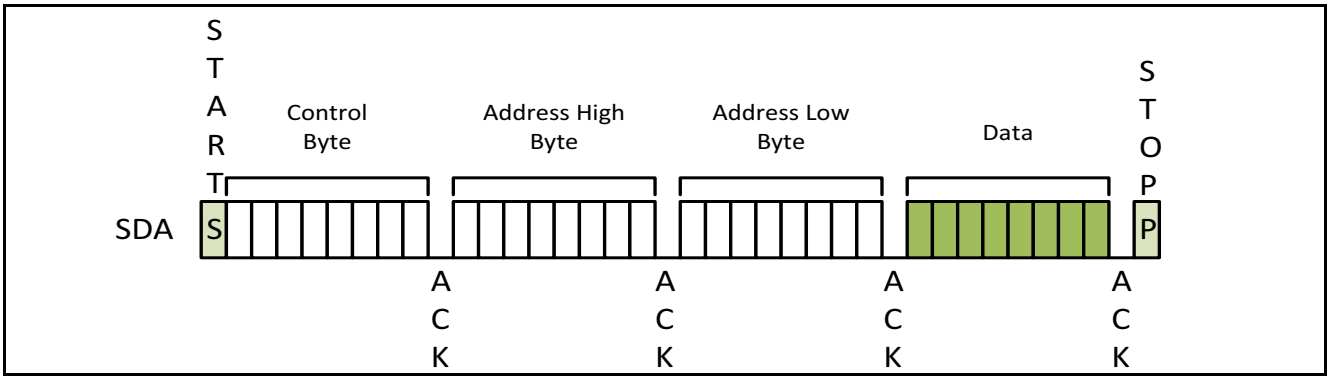

Figure 13 SDA sequence to write one byte

1) Defined in the TLE9012AQU DS

EEPROM

The control byte and the address bytes depend on the used memory. With the shown sequence, it takes ~ 15 ms to write one byte.

The bit sequence to read one byte is similar to the write sequence. After the memory specific control byte and address bytes, the memory responds with the control byte and the requested data.

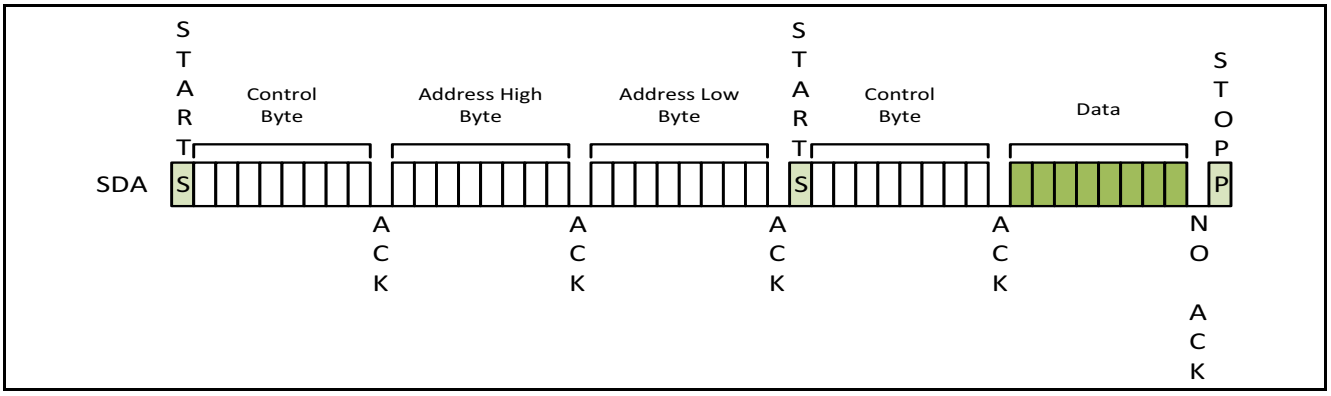

Figure 14 SDA sequence to read one byte

With the shown sequence, it takes ~ 18 ms to read one byte.

7 13 wire setup

The TLE9012AQU can be also used in a 13 wire setup (the 15 wire setup is shown in **Figure 1**). This means supply and sensing current share one wire for the top and bottom cell.

The 13 wire setup influences the CVM accuracy of the top and bottom cell due to the additional voltage drop forced by the supply current over these wires. A real 15 wire setup (sensing and supply current have separate wires) is used as a reference measurement to have a reference setpoint for CVM accuracy.

For the voltage stability required (dynamic & static), real Li-Ion cells (LFP R_i < 10 mΩ) are used. The intrinsic setup accuracy is 0.5 mV.

Figure 15 show the difference between the 13 wire and the 15 wire setup for the CVM accuracy. The cable length from the Li-Ion cells to the BMS Demo Board is 20 cm (3 BMS Demo Board were tested).

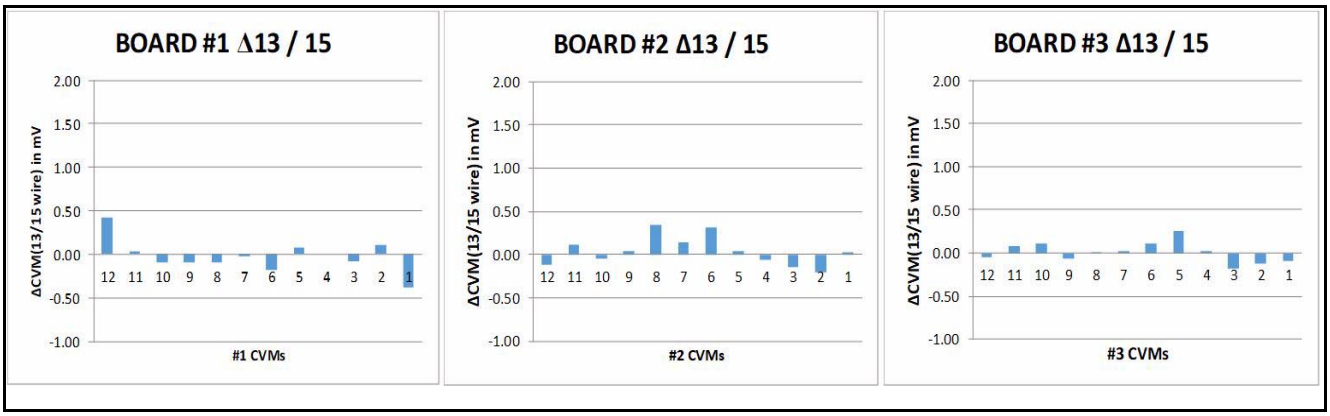

Figure 15 CVM accuracy Δ 13/15 wire setup with 20 cm cable length

Due to the setup, the differences for a 13 and 15 wire setup are practically negligible (difference in the range of setup accuracy). As the path from cell to Demo Board is very low ohmic, the supply current has practically no influence.

Figure 16 shows the CVM results for the Demo Board #2 with an increased cable length (cell-to-board) of 1.5 m.

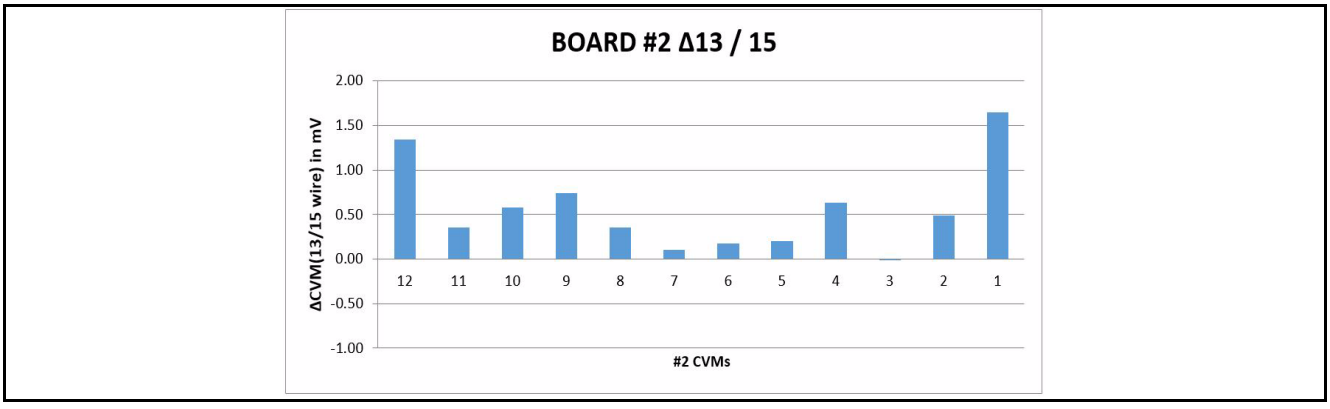

Figure 16 CVM accuracy Δ 13/15 wire setup with 1.5 m cable length

The comparison of **Figure 15** and **Figure 16** is showing the corner channel effect clearly on channel 1 and channel 12.

The effect due to the 13 wire setup (voltage drop over cable) is measureable and equal for the top and bottom channels. The strenght of the effect depends on the setup (cable length, connectors, fuses, voltage stability of source, etc.) and needs to be verified in the real application (in a real car battery).

If the offset at the top and bottom cells in the real car battery is too large to accept, it could also be compensated at the microcontroller as the offset is fixed by system characteristics.

8 iso UART communication interface

8.1 Introduction

The iso UART protocol is based on a two wire, differential, half duplex physical layer, which the Infineon Battery Management ICs use to communicate between slaves. A more detailed description can be found in the device datasheet.

The following section discusses the datasheet specs and how to interpret the iso UART waveforms at different points on the iso UART circuitry for robust communication between the slaves.

8.2 Physical layer overview

The datasheet specification states the threshold level for the iso UART analog receiver interface to convert the analog physical signals to useful digital signals for the bus timing protocol.

iso UART current threshold HIGH indicates the positive edge level to trigger a digital “1” signal.

iso UART current threshold LOW indicates the negative edge level to trigger a digital “0” signal.

Figure 17 shows how the iso UART interfaces are configured in the Master on Bottom (MOB) topology. In this topology, the low side interface is configured as receiver mode (RX) which receives the iso UART physical signals and translates them to digital signals for further interpretation. The high side interface is then configured as transmitter mode (TX) which drives the digital signal out into the physical link.

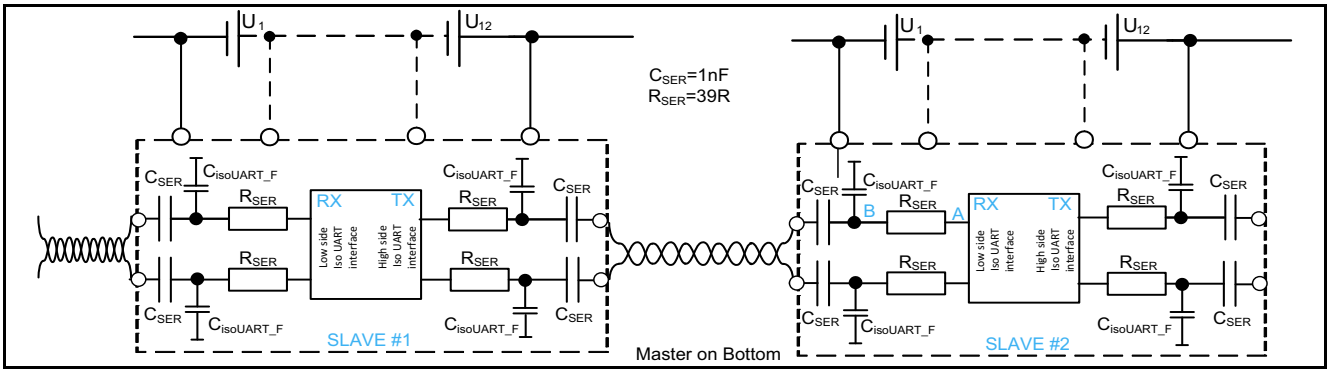

Figure 17 Master on Bottom communication

The physical and digital signals are illustrated as an example in **Figure 18**.

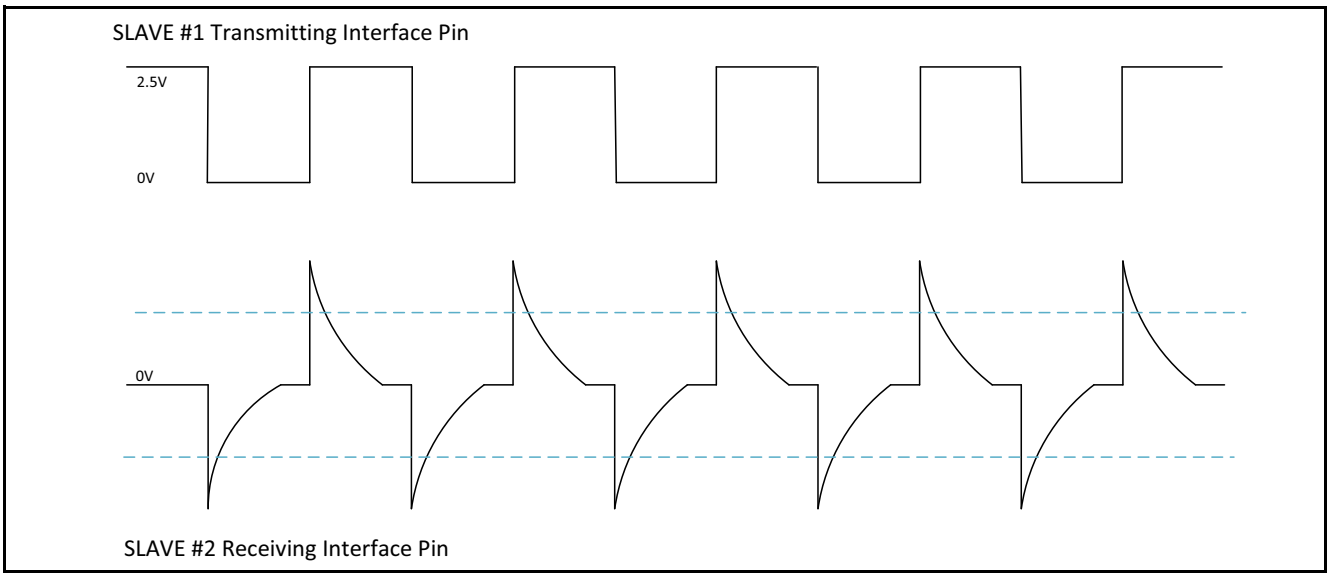

Figure 18 iso UART digital and analog signals

8.3 iso UART measurement point

In order to enable slave # 2 to propagate the correct digital signals at its iso UART TX interface, the analog signals at its RX pins must meet the threshold requirements (blue dash line). Measured at point B with respect to ground as shown in **Figure 19**, the negative signal must cross the blue line $I_{isoUART\_th\_LOW}$ max.*(R_{on}+R_{SER}) to trigger a digital “0”. For a digital “1” to be successfully triggered, the positive edge signal must cross the blue line $I_{isoUART\_th\_HIGH}$ max.*(R_{on}+ R_{SER}).

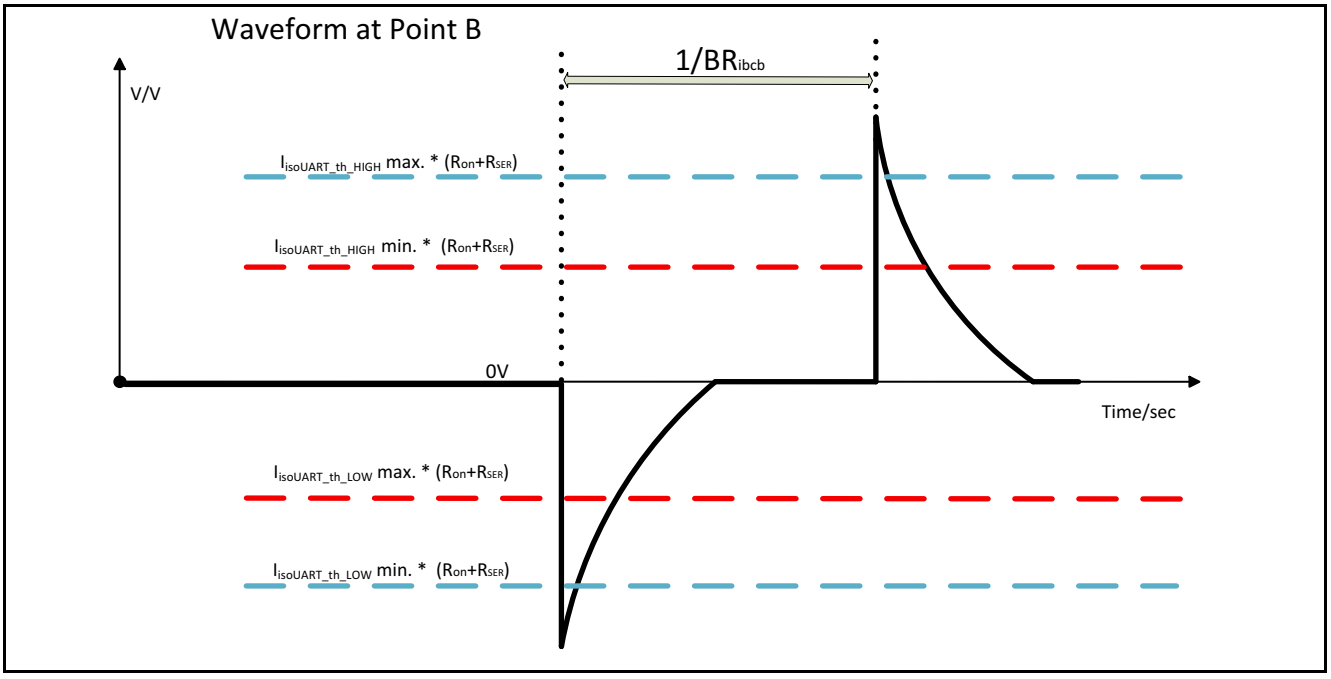

Figure 19 iso UART signal threshold level interpretation at Point B

If the signal is measured at Point A (directly at IC pin) with respect to ground, the threshold level should be reduced by the value R_{SER}. See **Figure 20**.

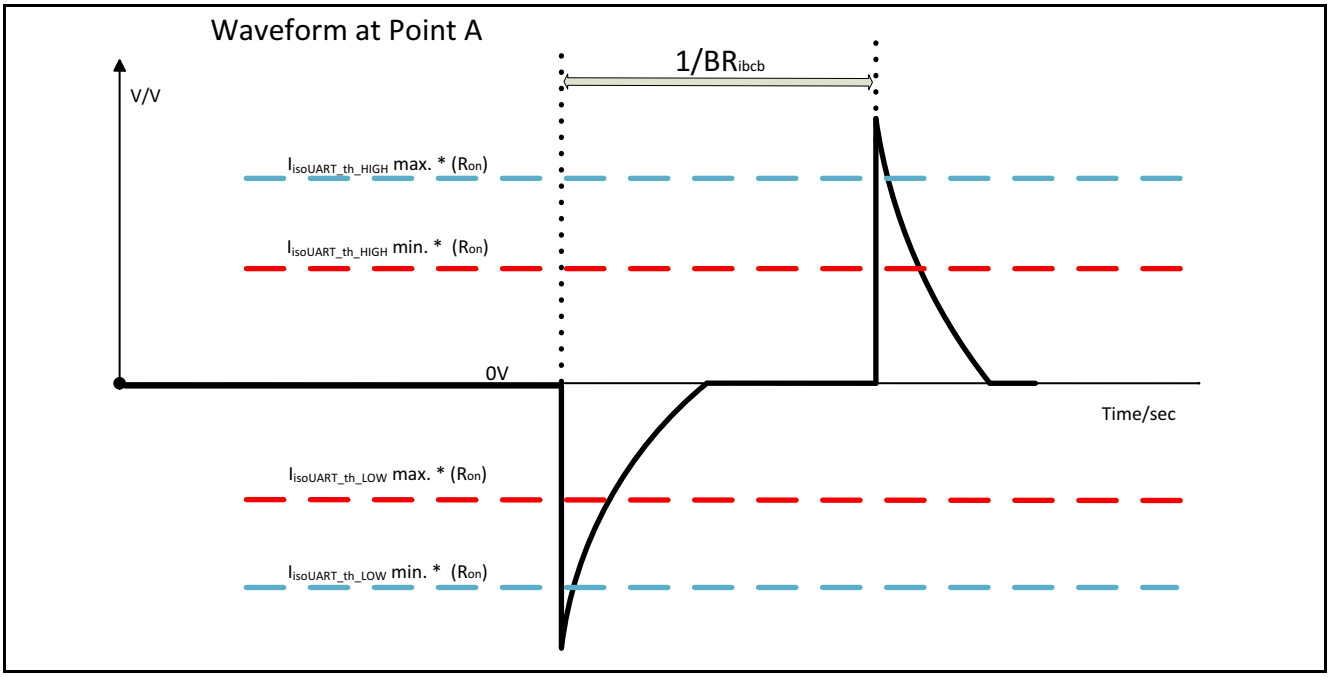

Figure 20 iso UART signal threshold level interpretation at Point A

8.4 Capacitive coupled signals

For capacitive signals, the guideline is to follow the requirements illustrated in **Figure 19** or **Figure 20** depending on the measurement point.

Figure 21 gives an example of the typical application use case in Infineon Sensing IC evaluation board. The C_{SER} and R_{SER} used is 1 nF and 39 Ω respectively. R_{SER} is preferred to be fixed at 39 Ω and the user can tune the C_{SER} to meet the threshold requirement. This tuning may have an impact on the EMC performance, therefore it should be evaluated to fulfill the EMC system level requirements by the user in the final system.

In this figure, we can see that the green signals at the slave iso UART receiver input meet the threshold requirements and the slave is able to transmit the correct red digital signals at its corresponding iso UART TX interface.

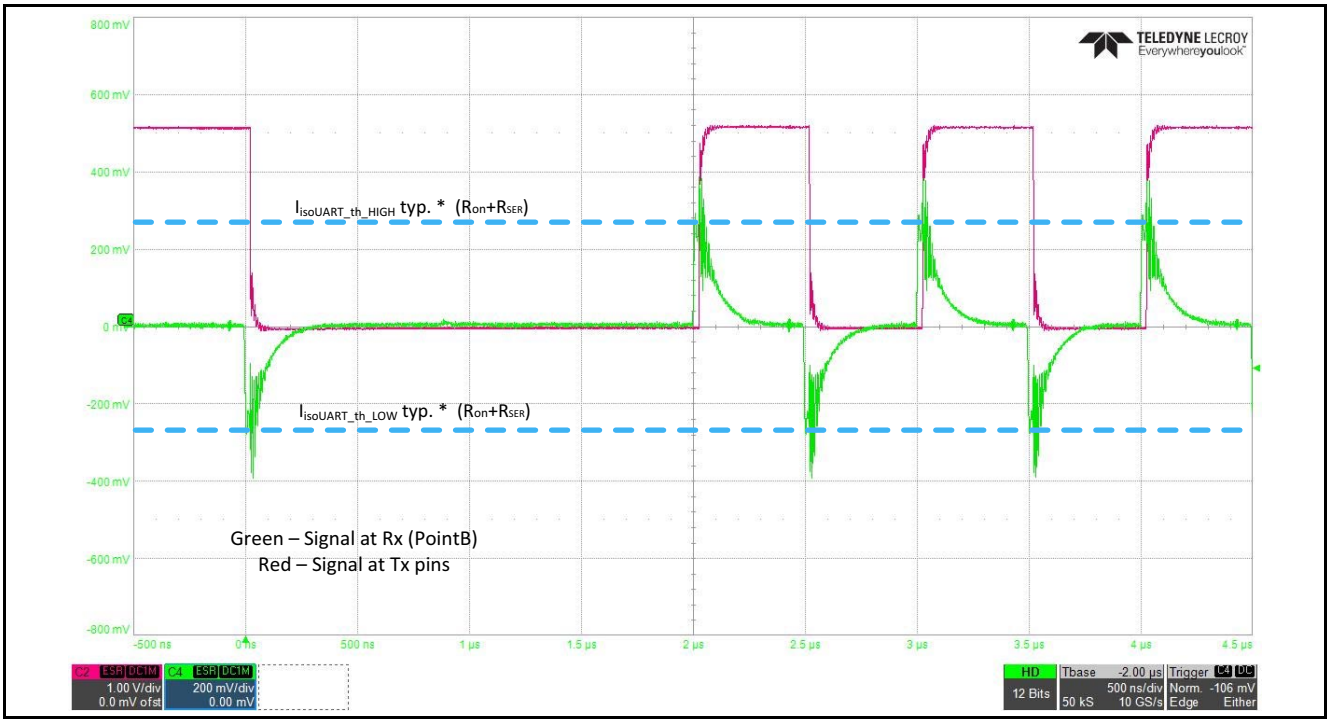

Figure 21 Capacitive coupled iso UART signals between 2 slaves

8.5 Transformer coupled signals

Due to the isolation requirement, it may be necessary to implement a transformer between the low voltage and high voltage domain boards (see **Figure 22**). In such an application scenario, the iso UART signals have a high tendency to oscillate due to the introduction of high inductance in the communication link.

Note: The information given is as a hint for the implementation of the Infineon Technologies components only and shall not be regarded as any description or warranty of a certain functionality, conditions or quality of the Infineon Technologies component(s). Infineon recommends verifying the transformer selection and tuning also under system level EMC requirements within the real application environment.

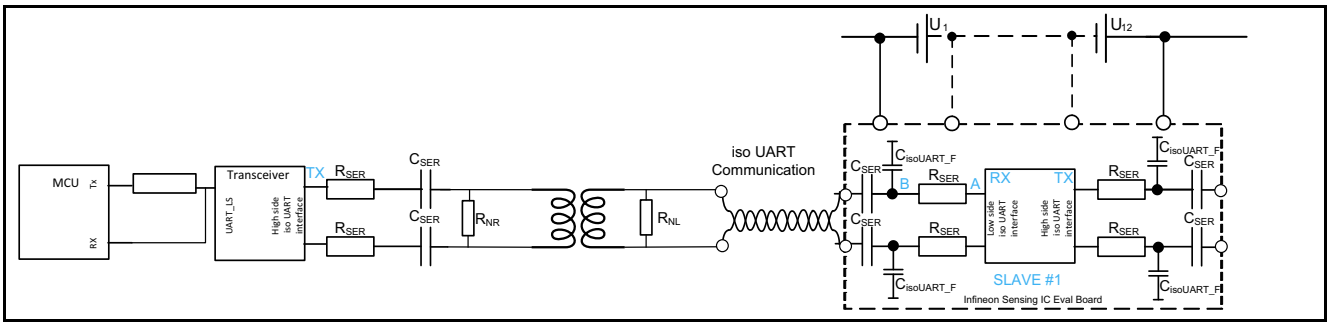

Figure 22 Transformer based circuitry at transceiver

Within a bit duration ($1/BR_{isoUART}$), the oscillating iso UART signal should not cross the prohibited threshold $I_{isoUART\_th\_HIGH}$ min.*(R_{on}+ R_{SER}) or $I_{isoUART\_th\_LOW}$ min.*(R_{on}+ R_{SER}) to avoid false triggering of the digital signal. The oscillation can be damped by adding damping resistors R_{NX} as shown in **Figure 22**.

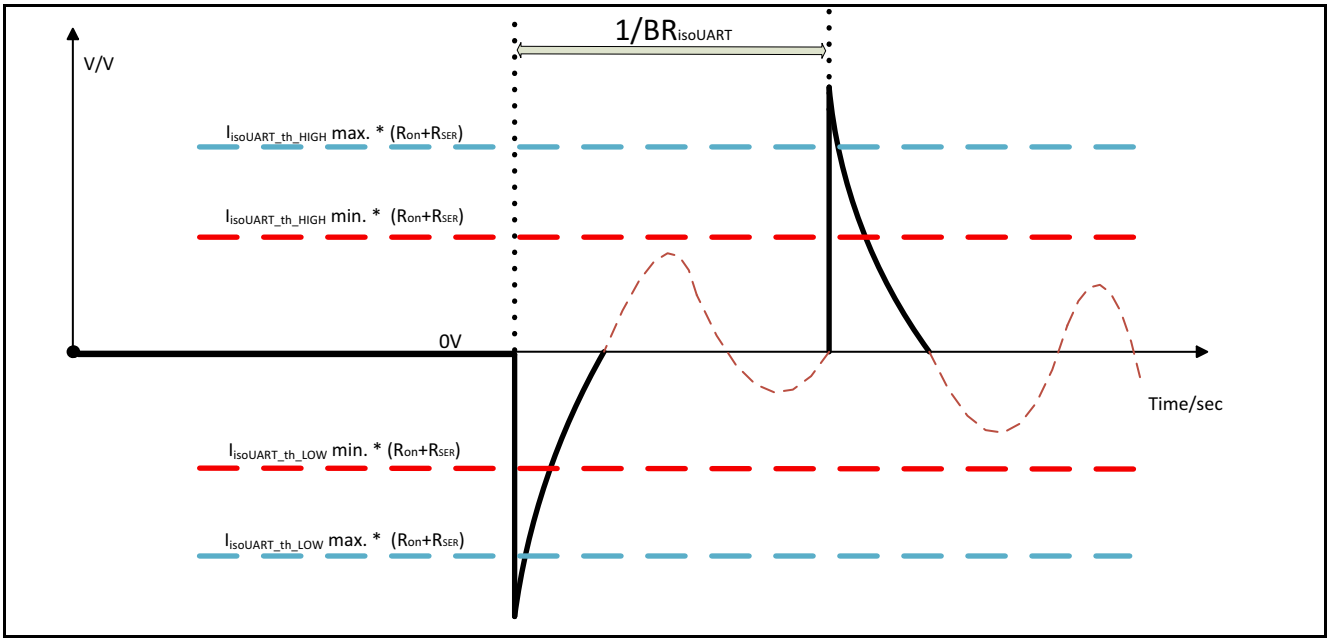

Figure 23 Transformer coupled signal at Point B

Figure 24 shows how the damping resistor affects the oscillation waveform. A smaller resistor is able to damp the oscillation better but is also making the first spike narrower.

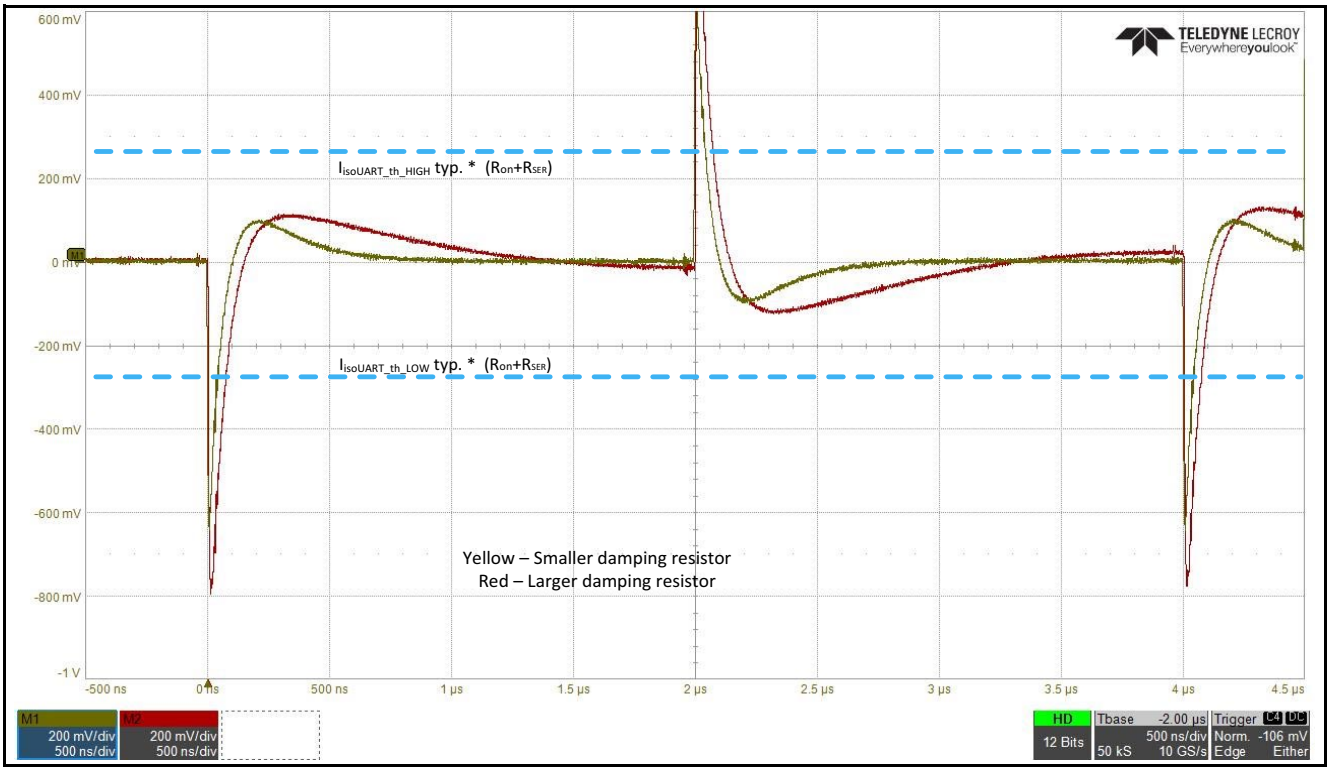

Figure 24 iso UART waveforms with different damping resistors

The iso UART physical layer thresholds ($I_{isoUART\_th\_HIGH}$ min., $I_{isoUART\_th\_HIGH}$ max., $I_{isoUART\_th\_LOW}$ min., $I_{isoUART\_th\_LOW}$ max.) are defined in the datasheet. A high sensitivity current probe can be used to measure the iso UART current in one of the iso UART communication wires (see **Figure 25**). In cases where an iso UART current measurement is not possible, the iso UART voltage measurement can be realized with normal oscilloscope probes.

Note: A differential voltage measurement at the R_{SER} (39R) resistor (the differential voltage needs to be divided by 39 Ω) is a very good way to measure the current which passes the receiver. If a current probe is used (which is better than just measure the single ended voltage at the iso UART pin), a higher current will be measured (because a part of this current is shorted by EMC caps $C_{isoUART\_F}$ and does not pass the receiver).

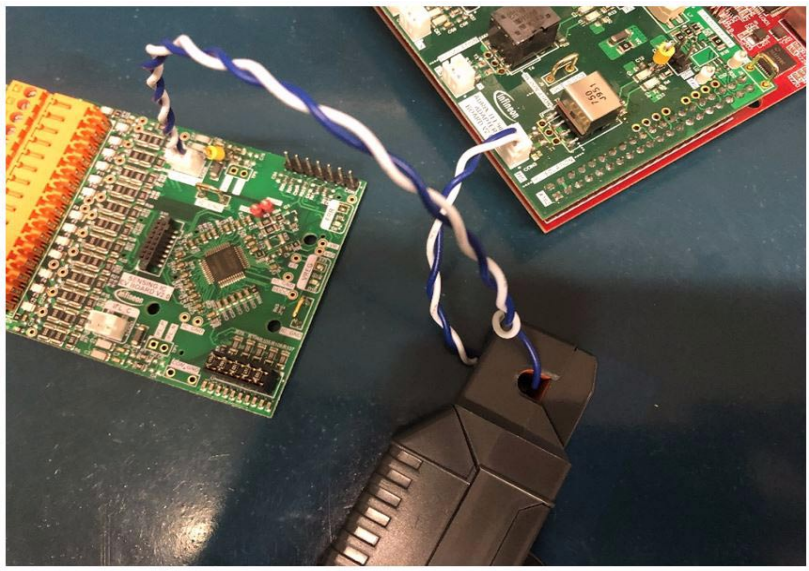

Figure 25 Current probe measurement$_B$

The iso UART current waveform can be used to determine the overdrive current I_{od} and the pulse duration t_{pulse} (see **Figure 26**).

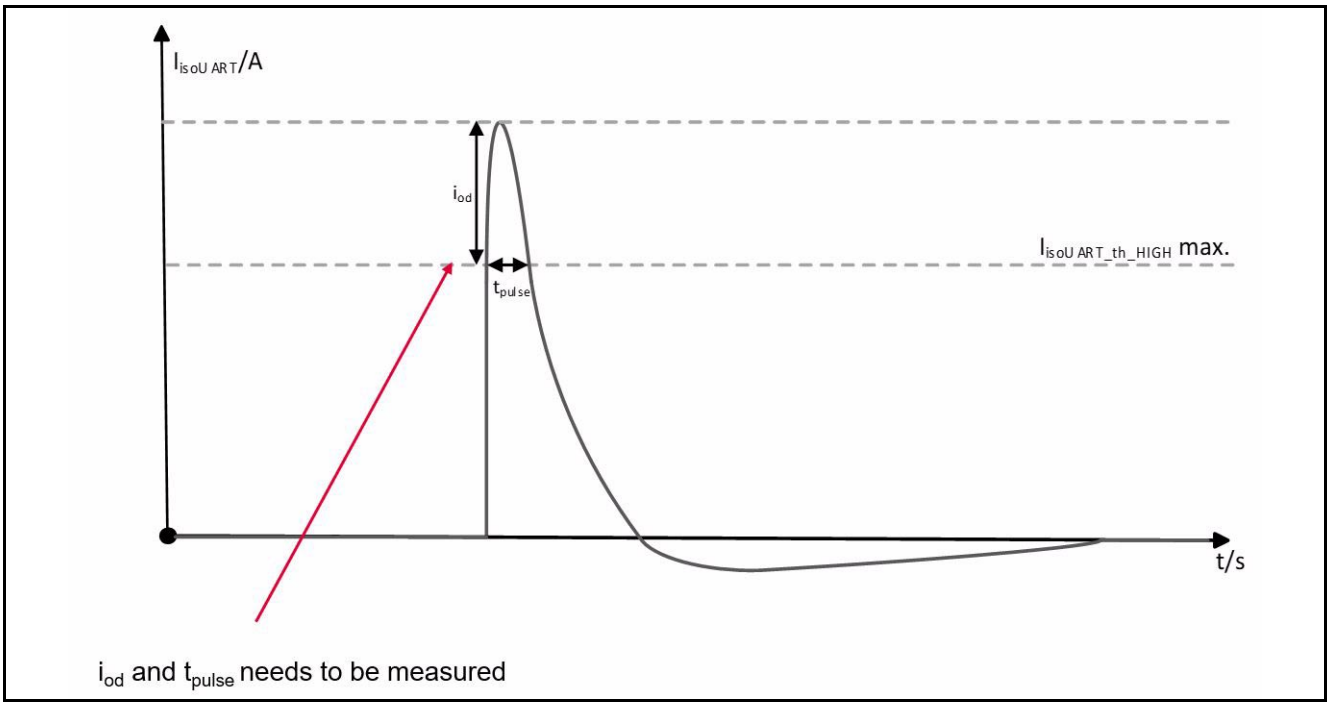

Figure 26 iso UART waveform

The resulting I_{od} should fall on the upper right part of the graph in **Figure 27** to ensure that bits are correctly detected.

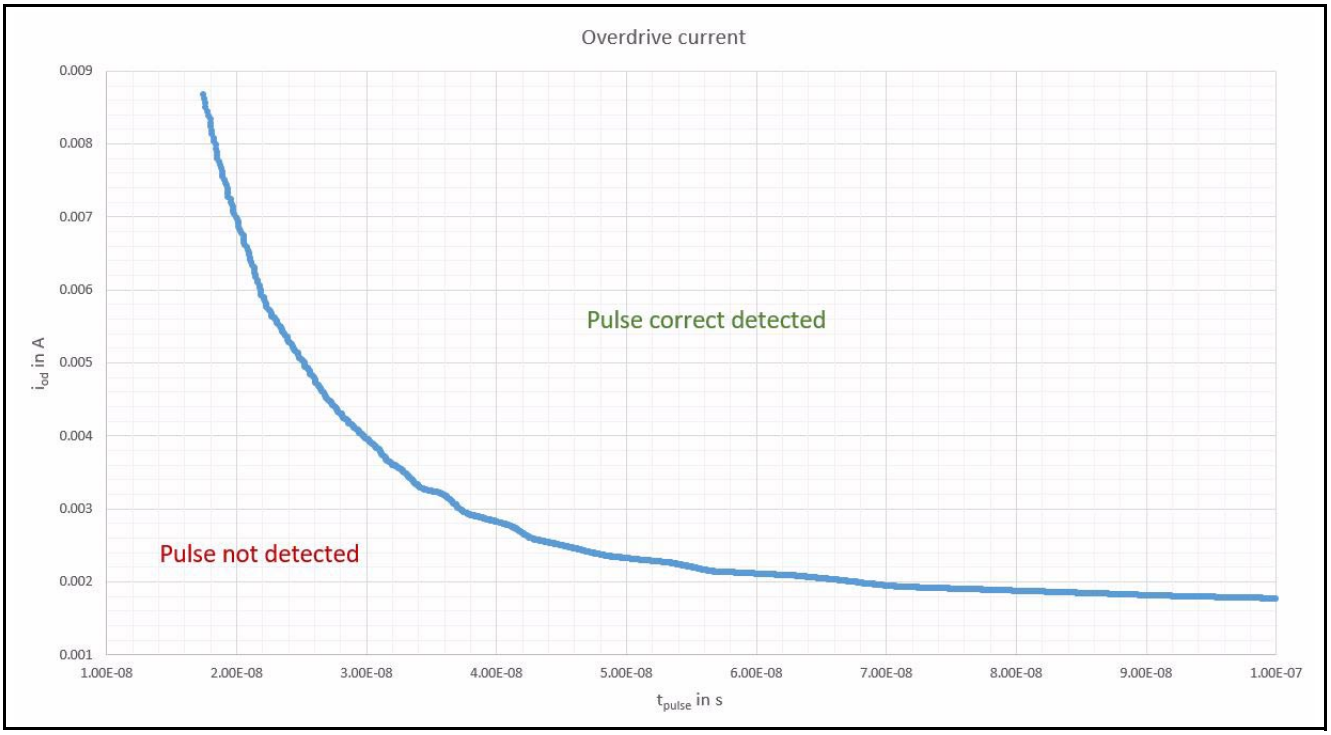

Figure 27 Overdrive current

For example in **Figure 29**, a peak voltage of 17 mA is measured. It leads to a i_{od} of (17 - 6.25) mA = 10.75 mA and a pulse duration t_{pulse} of 50 ns. This value is on the upper right side of the graph and the bit will be correctly detected.

*Note: The iso UART propagation delay increases the closer the overdrive current i_{od} is to the pulse detection curve (**Figure 27**). Therefore, the max. $t_{isoUART\_prop\_del}$ for the smallest i_{od} is shown in **Figure 28**.*

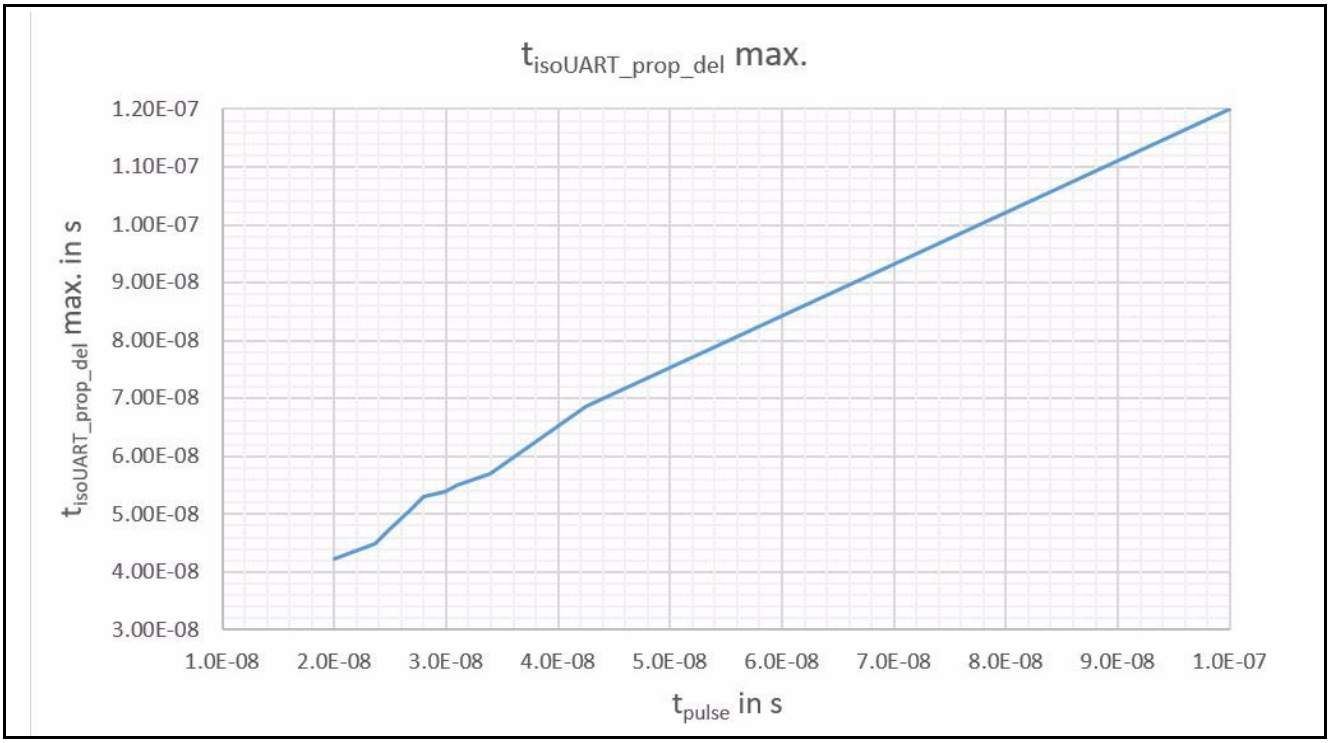

Figure 28 iso UART propagation delay $t_{isoUART\_prop\_del}$ max.

iso UART communication interface

Figure 29 and **Figure 30** show the current waveform of the iso UART communication with two different transformers (Sumida CEP99P, Pulse HM2116ANL) and R_{NL}/R_{NR} set to 510 Ω (2x510R damping resistor).

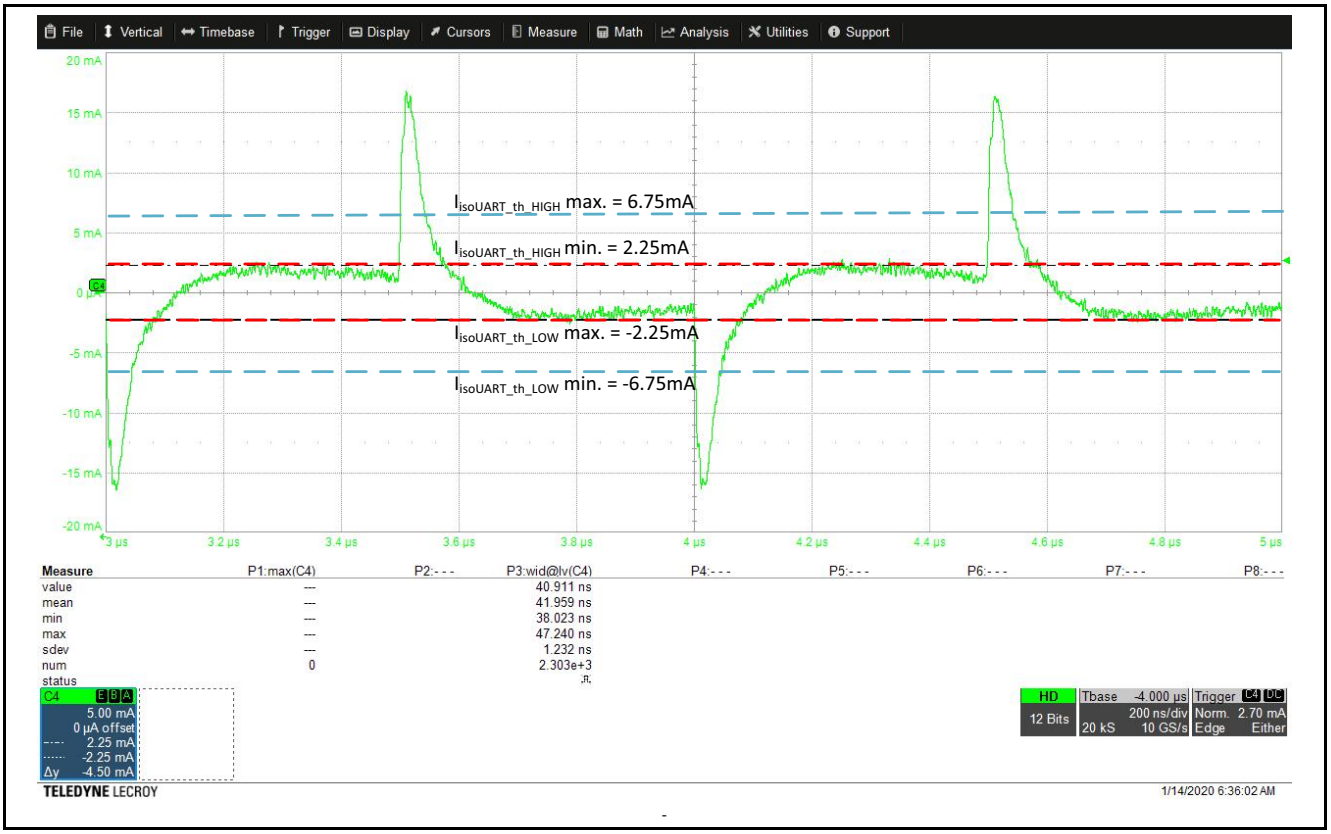

Figure 29 iso UART current probe measurement - CEP99P (2x510R)

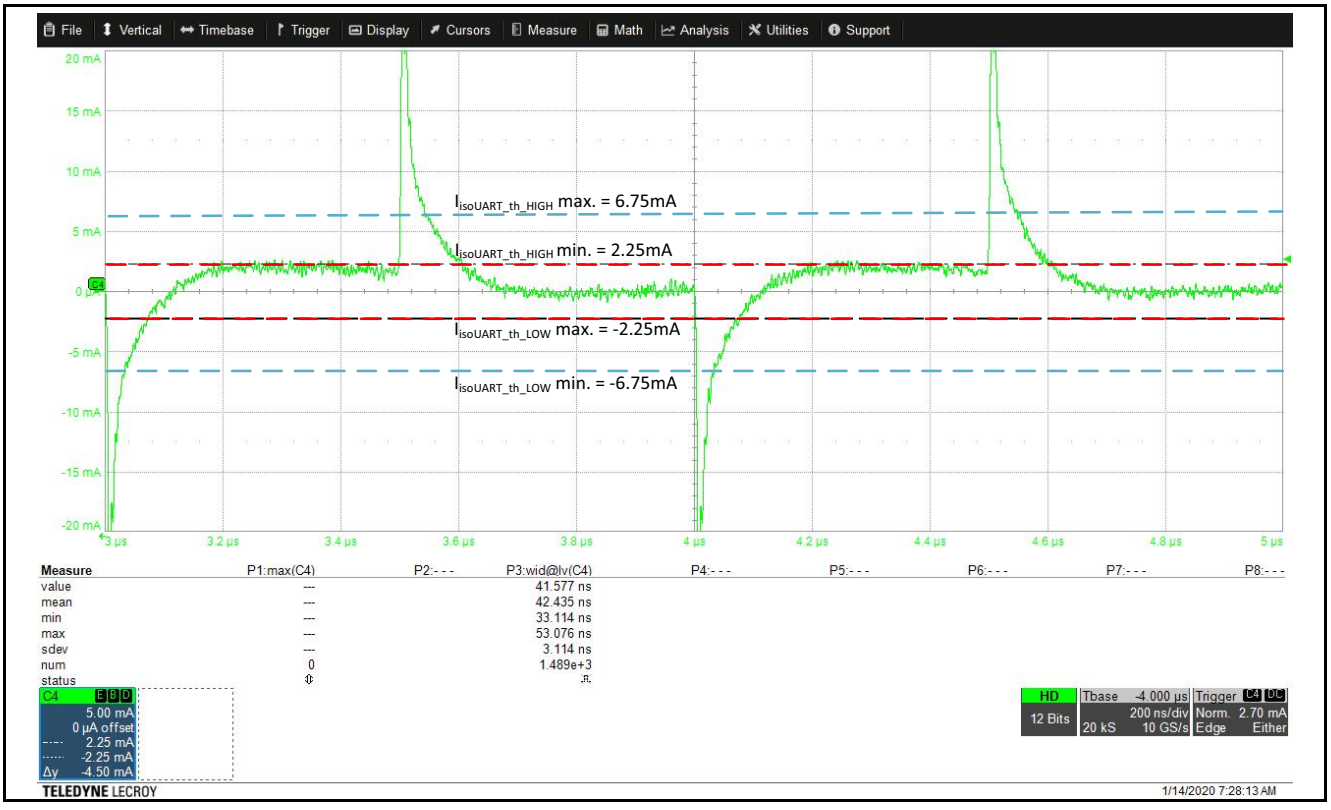

Figure 30 iso UART current probe measurement - HM2116ANL (2x510R)

iso UART communication interface

The waveform in **Figure 31** for the transformer CEP99P from Sumida with 2x510R damping resistor shows the reference waveform which has been tested with corner samples.

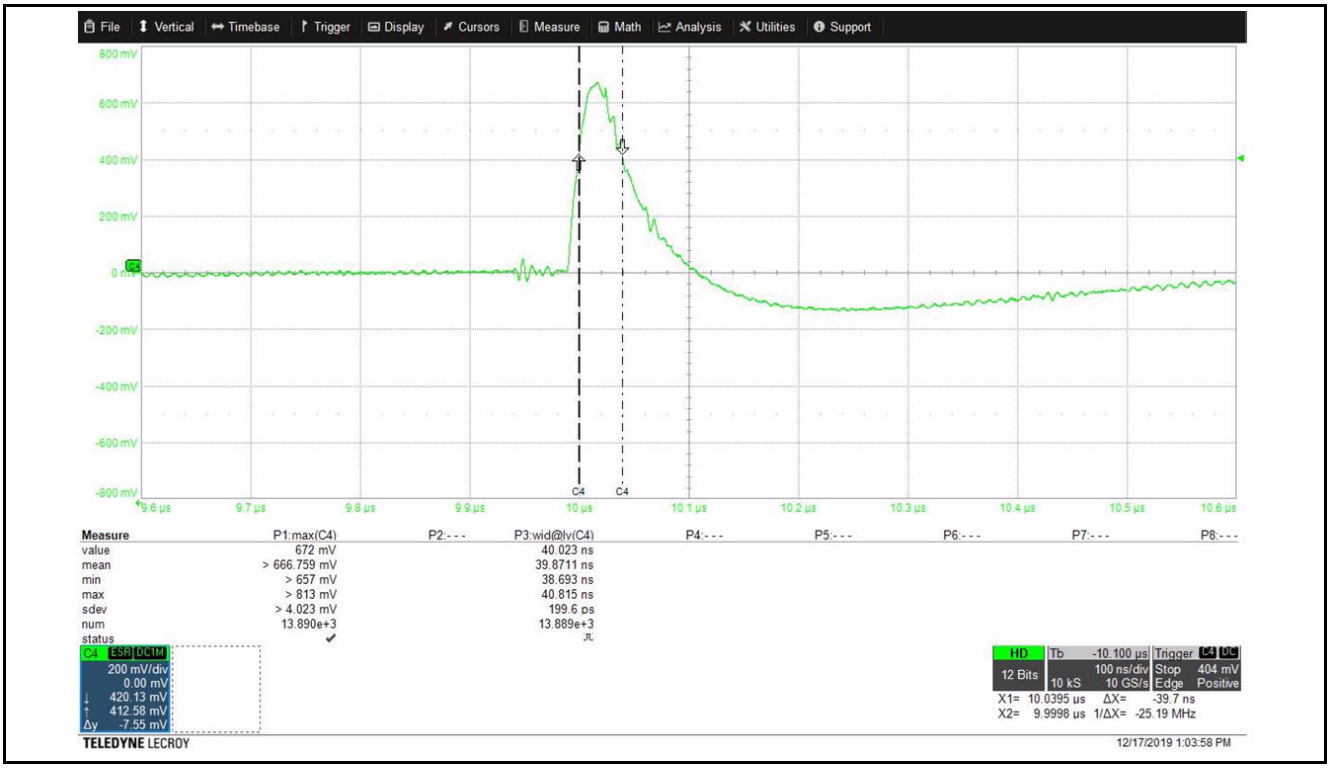

Figure 31 Transformer CEP99P with 2x510R damping resistor

Figure 32 shows the positive pulse with a Pulse HM2116ANL transformer with 2x510R.

As a guideline, a pulse duration of 40 ns over the temperature range of the application is recommended.

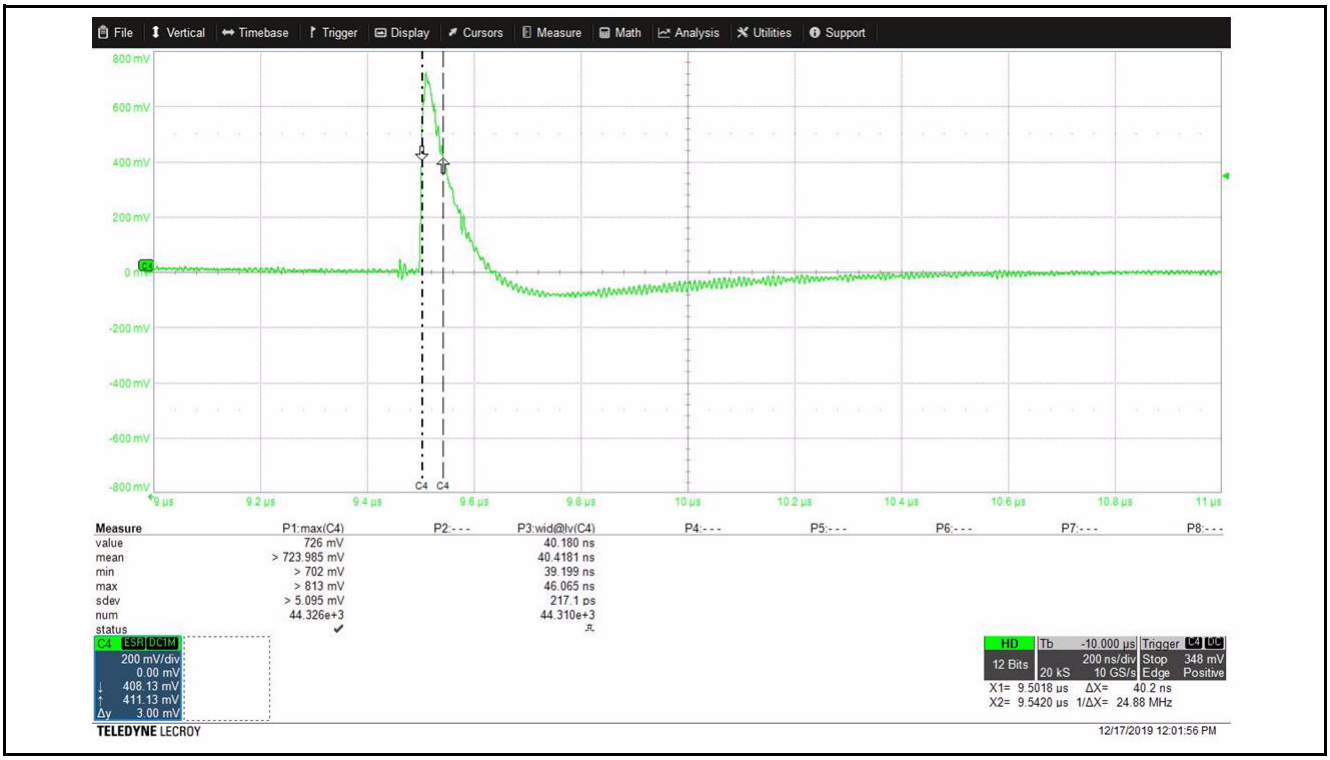

Figure 32 Transformer HM2116ANL with 2x510R damping resistor

iso UART communication interface

Figure 33 shows the iso UART waveform measurement at Point B from two different transformer evaluations. The yellow waveform shows the waveform from Pulse HM2116ANL while the green waveform shows the transformer from Sumida CEP99P. Both transformers have 2x510R damping resistor mounted.

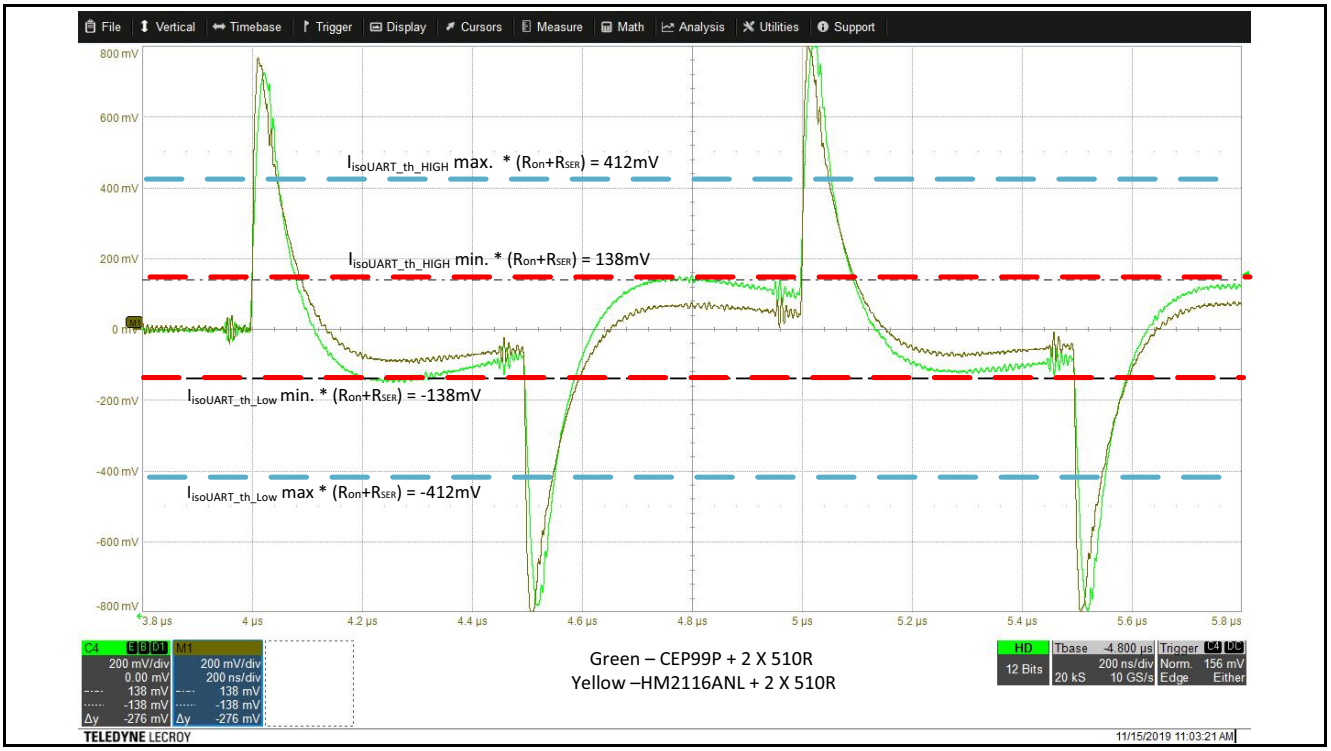

Figure 33 Transformer iso UART waveforms comparison

9 Revision History

Revision	Date	Changes
1.3	2020-04-03	Editorial changes **Chapter 5** Typical chip performance added **Chapter 6** EEPROM added **Chapter 7** 13 wire setup added **Chapter 8.5** Transformer coupled signals added
1.2	2019-10-23	Minor fixes
1.1	2018-12-17	Added chapter unused pins, added chapter use less than 12 cells, added layout hints, small fixes
1.0	2018-10-31	Initial Draft

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