



Let's consider an example of Cypress SRAM which has 5 address inputs and interfaced with FPGA. In case 1, if you would like to write a word on address A0, A1, A2, A3, A4 = 11001 then FPGA will send these address bits to SRAM and SRAM will store that word internally on the same address 11001.

Now consider cases 2, in this case the address mapping are different than case 1 and you would like to write a same word on the same address; so FPGA will send the address 11001 (A0-A4) but internally the SRAM will store that word on the address 01110 (SRAM A0-A4). When FPGA wants to read the same word then it will send an address 11001 but SRAM will provide the data to FPGA from 01110 address.

As a result, the FPGA will always receive the expected data for a given address regardless of address labeling.

There is a special case where A0 and A1 must be in the same location on both SRAMs. This case occurs when the application is using the internal Burst Counters.