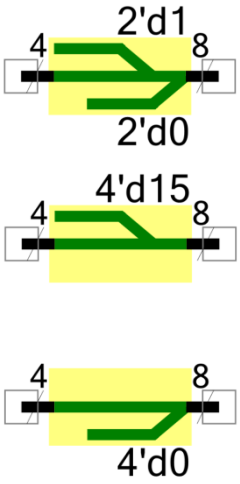
BusConnect
0.0

Features

- Connects narrow digital bus to a wide digital input bus.
- Unconnected bits are hardcoded to digital constants.
- Virtual component.
- Simplifies and saves space on a schematic.



General description

The BusConnect component is a virtual component facilitating connection of narrow digital bus to wider input bus at the design time[*]. When a narrow bus is connected to wide input, there is an ambiguity in bits correspondence and some bits are left unconnected, which leads to compilation errors. In a result, tedious manual routing is required to assign input-to-output bits correspondence and to terminate unused bits. The BusConnect component assigns input-to output bits order and sets hardcoded values to unconnected pins. Using BusConnect component saves space on a schematics and simplifies signal routing. BusConnect works only for digital bus types and can't be used with analog signals.

When to use DDS24 component

Component was developed for connecting 23-bit wide input bus of DDS24 custom component to digital sources, but it can be used with any other PSoC component which has digital input or output bus. Demo project is provided.

[*] The opposite case of connecting wide output bus to a narrow input bus is trivial.

Functional Description

Many PSoC components have digital input or output buses which can be used for interfacing. Consider an example (Figure 1) when a digital output bus of width 4 from the BasicCounter has to be connected to VDAC8, which has digital input bus of fixed width 8. Such schematics arrangement shall not compile because of two types of errors: (i) the number of input and output bits do not match and (ii) some bits are having multiple drivers.

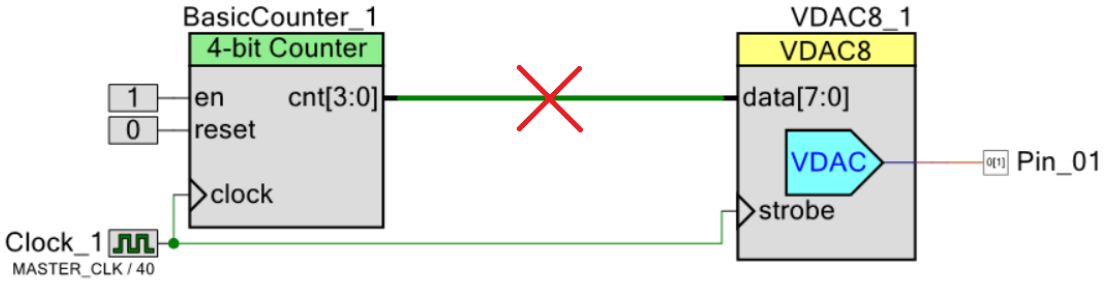


Figure 1. Failed attempt to connect output bus of width 4 to input bus with fixed width 8.

Since there are more input bits than available sources, it has to be explicitly stipulated which input bits are being connected to data source and which are being terminated(*). Let's decide that in this application bits [5:2] are connected to the source (4-bit BasicCounter), the least significant bits [1:0] are terminated with digital "1" each, and the remaining most significant bits [7:6] are terminated with digital "0" each (Figure 2). Such connection will produce a 15-step voltage ramp with offset of 3.

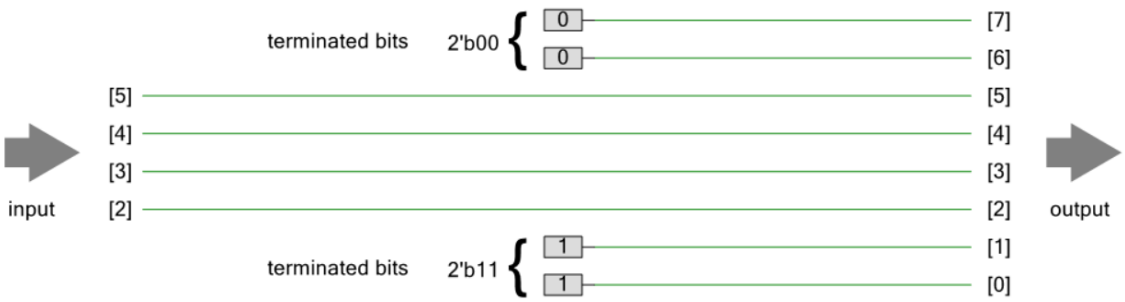


Figure 2. Example of bits [5:2] being connected to the data source, while unconnected LSB's and MSB's are being terminated with hardcoded values.

* In partially connected input bus, the unconnected bits can't be left free-hanging.

In Cypress Creator IDE such assignment can be accomplished by using regular bus indexing tools and digital constants (Figure 3).

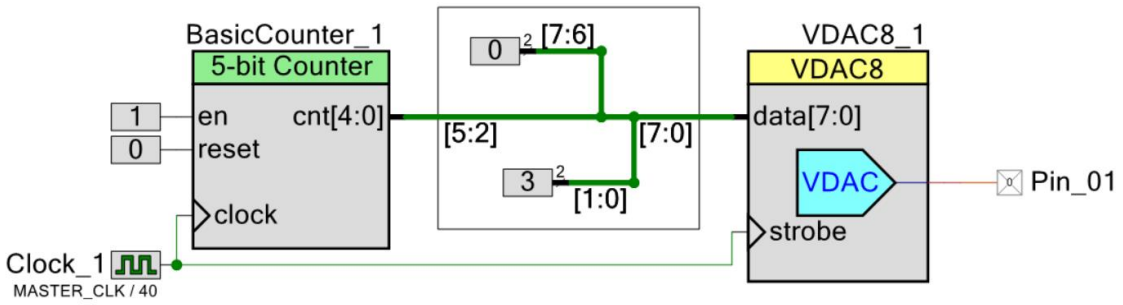


Figure 3. Bus connection accomplished using regular bus indexing tools and digital constants.

In this example, the LSBs bus [1:0] of width 2, is being terminated with digital constant value 3 (decimal representation 2'd3, or binary 2'b00); input bits [2:5] are being connected to the source, and MSBs bus [7:6] of remaining 2 bits is terminated with digital constant value of 0 (decimal representation 2'd0, or binary 2'00).

Using the BusConnect component the schematic can be cleaned up and simplified, while preserving all visual information (Figure 4).

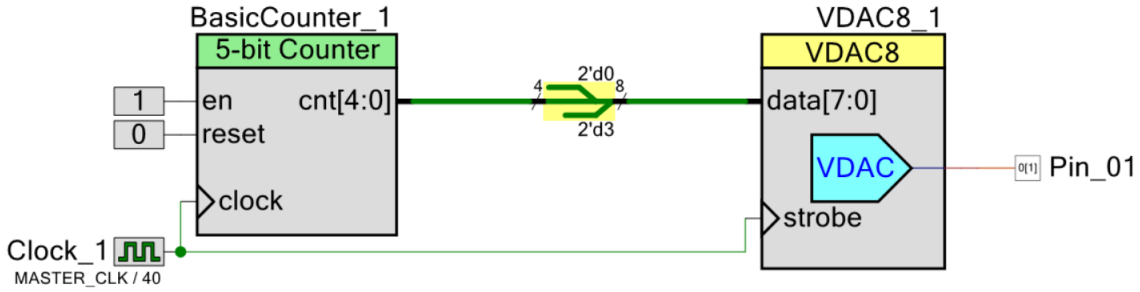


Figure 4. Final arrangement using BusConnect component.

All tree representation of bus connection on Figures 2, 3 and 4 are equivalent and summarized on Figure 5. The BusConnect symbol displays the input and output buses width, and the width and termination constant value for the MSBs and LSBs using standard decimal notation {width}'d{value}.

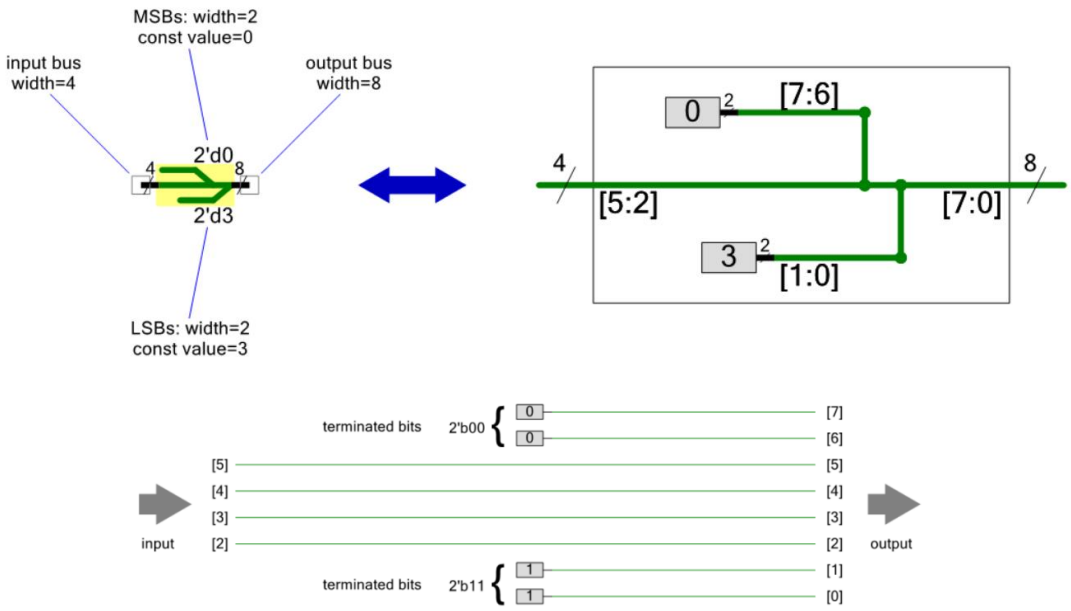


Figure 5. Equivalent representations of the BusConnect component.

Using BusConnect component saves space and simplifies schematic.

Input-output connections

inp[N-1: 0] – input bus

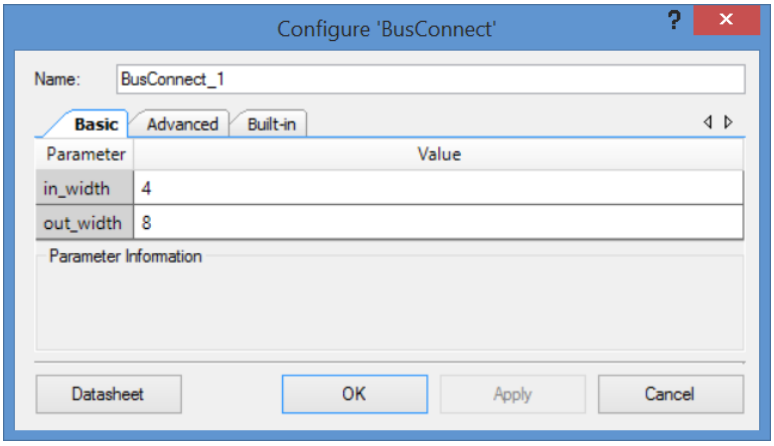
This pin is digital input bus. The bus width is user-selectable, highest is 32. Input width should always be less or equal output width (N≤M). The pin is always visible, and must be connected to valid digital source.

out[M-1: 0] – output bus

This pin is digital output bus. The bus width is user-selectable, highest is 32. Output width can't be smaller than input width (M≥N). This pin is always visible. The pin doesn't have to be connected.

Parameters and Settings

Basic dialog provides following parameters:



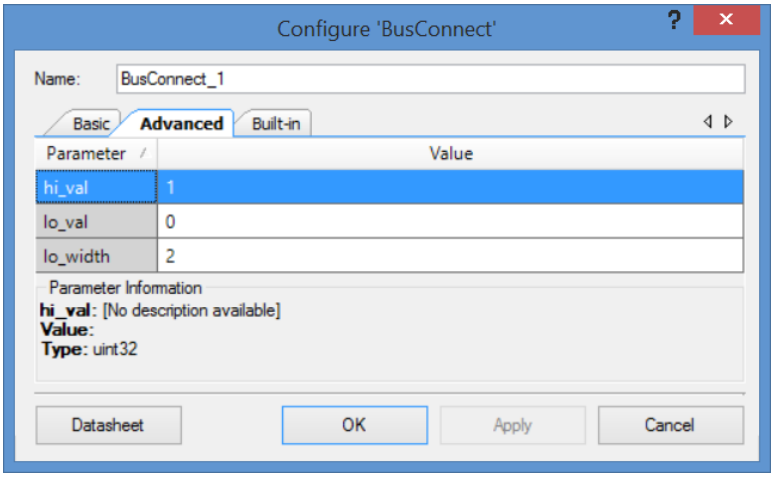
inp_width [1…32]

Input bus width. Valid range is from 1 to out_width.

out_width [1…32]

Output bus width. Valid range is from inp_width to 32.

Advanced dialog provides following parameters:



MSBs_val (uint32)

Hardcoded constant assigned to the MSBs group of unconnected pins. Default value is 0. The value assigned can't exceed the maximum allowed by the number of available bits. The MSBs' width is automatically calculated from the values of the input, output and LSBs width as: (out_width – inp_width – LSBs_width).

LSBs_val (uint32)

Hardcoded constant assigned to the LSBs group of unconnected pins. Default value is 0. The value assigned can't exceed the maximum allowed by the number of available bits.

LSBs_width [0...31]

Width of the LSBs group of unconnected pins. Valid range is from 0 to (32 – inp_width). If no LSBs are required, set this value to "0". The component symbol will update to indicate that the LSBs or MSBs bus is absent.

Application Programming Interface

The component does not have associated API.

Resources

The BusConnect doesn't consume extra UDB resources (as compared to manual routing). The component is not device-specific and works with any of PSoC4 or PSoC5. Component does not use any clocks.

Performance

The component is written in Verilog and does not consume CPU resources. The component is virtual, that is all configuration parameters are set at design time and can't be altered during run-time.

Sample Firmware Source Code

Basic application example shown on Figure 6. Here the BusConnect joins 4-bit output bus from the BasicCounter and 8-bit control bus of the VDAC8 to generate a 15-step ramp wave with offset defined by the MSBs constant (from 64 to 124). Demo project provided.

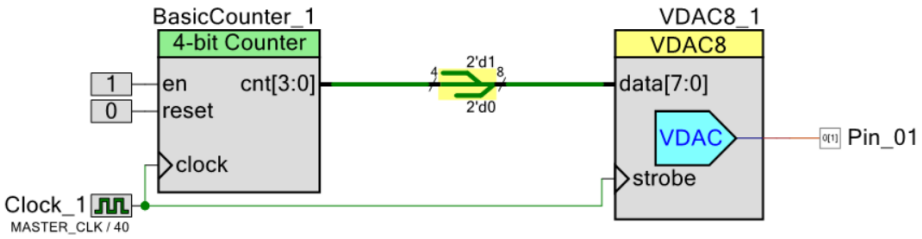


Figure 6. Basic application example.

Component Changes

Version	Description of changes	Reason for changes/impact
0.0	Version 0.0 is the first beta release of the BusConnect component	