Full Wave Signal Rectifier with LPF using PSoC 1

Project Name: Example_FullWave_Rectifier_with_LPF
Programming Language: C
Software Version: PSoC Designer 5.2
Associated Part Families: CY8C27x43,CY8C29x66,CY8C24x94
Related Hardware: CY3210
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Project Objective

The project implements a Full Wave Signal Rectifier along with a Low Pass Filter to get the filtered output using PSoC® analog resources.

Overview

The analog signal is fed to a comparator. The output is used to modulate the sign of a SC Block to convert the AC input signal to a full wave rectified output. The rectified output is fed to a 2-pole low pass filter that gives a filtered DC voltage as output.

User Module List and Placement

The following table lists user modules used in this project and the hardware resources occupied by each user module.

User Module	Placement
PGA_1	ACB00
CMPPRG_1	ACB01
RefMux_1	ACB02
SCBLOCK_1	ASC10
LPF2_1	ASC21, ASD11

User Module Parameter Settings

The following tables show the user module parameter settings for each of the user modules used in the project.

PGA		
Parameter	**Value**	**Comments**
Gain	1.000	The PGA is configured as unity gain amplifier.
Input	AnalogColumn_InputMUX_0	Input from P0[1] is connected from AnalogColumn_InputMux0
Reference	AGND	The PGA is referenced to Analog Ground
AnalogBus	Disable	The analog output is not used. The output of the PGA is internally connected to the SC Block

SCBLOCK		
Parameter	**Value**	**Comments**
FCap	16	Feedback capacitor
ClockPhase	Norm	The clock phase is chosen as normal
ASign	Neg	This value is XORed with the hardware modulator signal from the CMPPRG to decide the sign of the SC Block
ACap	16	Gain is FCap/ACap = 1
ACMux	ACB00	Output of PGA (Buffer) is routed to SCBLOCK's I/P
BCap	0	Not used

SCBLOCK		
Parameter	**Value**	**Comments**
AnalogBus	AnalogOutBus_0	SCBLOCK (Rectifier) output is routed to P0.3
CompBus	Disable	Not used
AutoZero	On	The Auto Zero compensation of the SC block is enabled
CCap	0	Not used
ARefMux	AGND	The input is referenced to AGND
FSW1	On	Phase-2 switch in Fcap is enabled
FSW0	On	Phase-1 switch in Fcap is enabled
BMux	–	Bmux is not used
Power	High	SCBLOCK set for full power

Note The column clock decides the over sampling ratio of the SC block. The data clock to the SC Block is one quarter of the column clock. For a column clock of 4 MHz, the data clock is 1 MHz. For a 20 KHz input signal and 1 MHz of data clock, the over sampling ratio is 50. When the input frequency increases, the over sampling ratio reduces. This can be seen as discreet steps on the output. The general rule of thumb is that for a smoother output, a higher oversampling ratio should be used.

RefMux		
Parameter	**Value**	**Comments**
Reference Selection	AGND	Used to route AGND to P0[4]

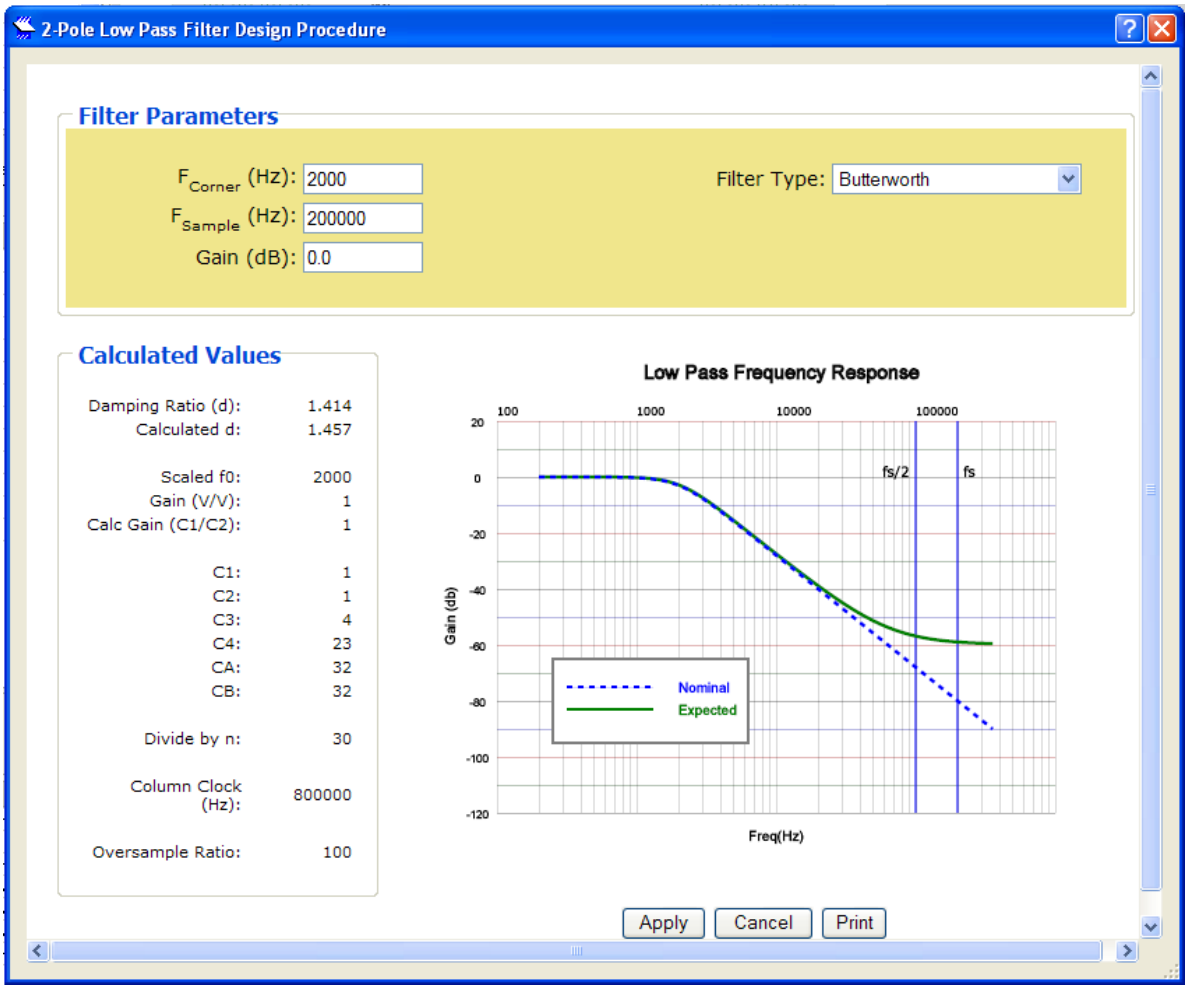
CMPPRG		
Parameter	**Value**	**Comments**
AnalogBus	Disable	Not used
CompBus	ComparatorBus_1	The output of comparator is routed to Comparator Bus so that it can be used as a modulating source for the SC Block
Input	ACB00	Input to the Comparator comes from the PGA
LowLimit	VSS	The lower limit is chosen as Vss
RefValue	0.500	The Low Limit and RefValue set the threshold of CMPPRG to VDD/2

LPF2		
Parameter	**Value**	**Comments**
C1	1	See note
C2	1	See note
C3	4	See note
C4	23	See note
CA	32	See note
CB	32	See note
Input	ASC10	Rectifier output is routed to the LPF input
AnalogBus	AnalogOutBus_1	LPF output is routed to P0.5
CompBus	Disable	Not Used
Polarity	Non-Inverting	The polarity is set as non-inverting.

Note C1, C2, C3, C4, CA, and CB are the parameters set automatically by the LPF Design Wizard. Right click on the LPF User Module and select the LPF Design Wizard. Select the parameters as shown in the following figure:

The cut off frequency of the filter is selected as 2 KHz.

Figure 1. LPF Design Wizard

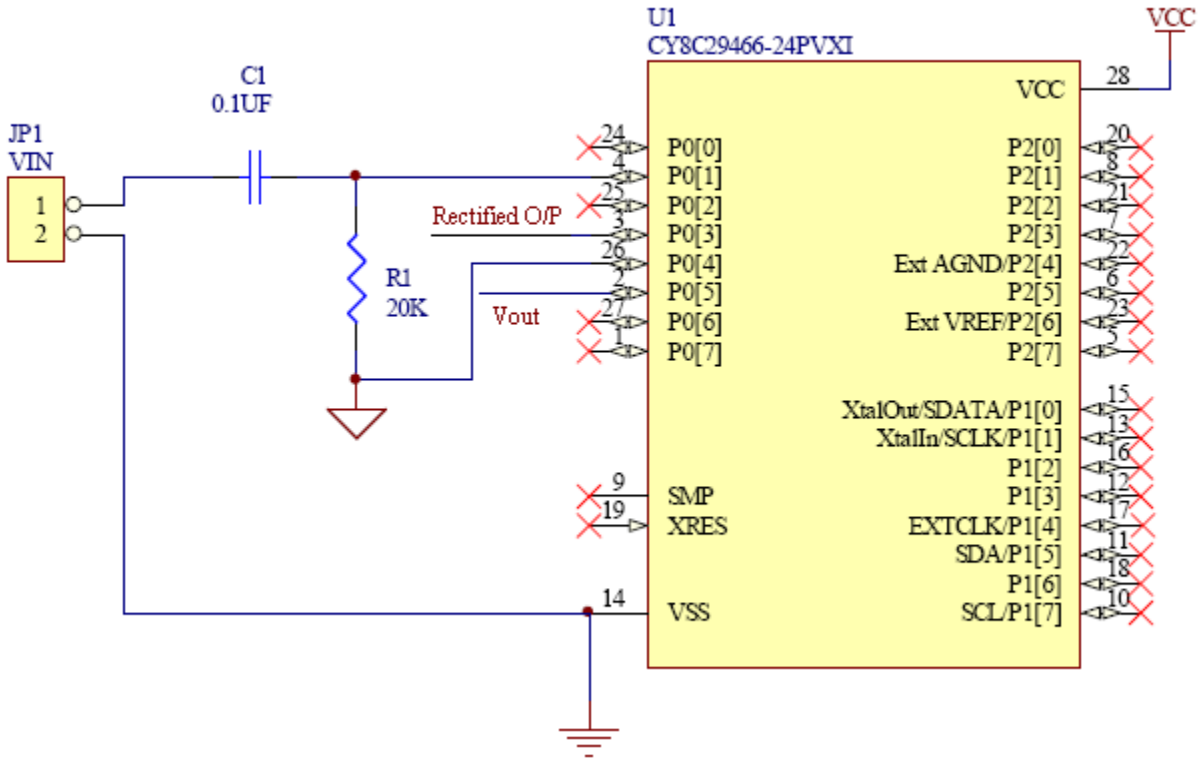


Global Resources

Important Global Resources		
Parameter	**Value**	**Comments**
Analog Power	SC On / Ref High	Switched Capacitor blocks On, Reference at High Power
VC1	6	VC1 generates 4 MHz column clock to the SC Block
VC2	5	VC2 generates 1 MHz column clock to the SC Block

Hardware Connection

Figure 2. Project Schematic Diagram



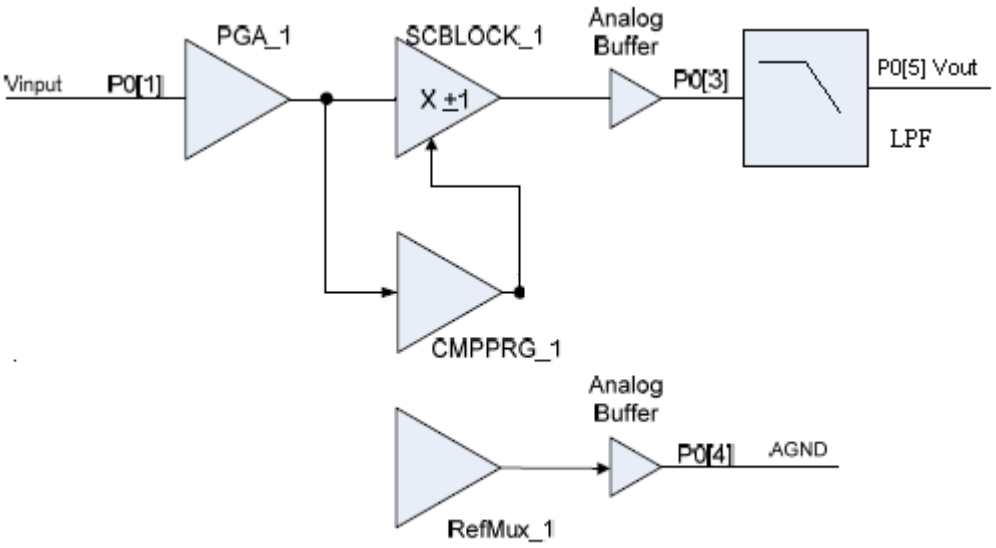
The Analog Ground (AGND) is brought out on P0[4] and the input signal of 20 kHz (referenced to VSS) is biased to AGND using C1-R1. The rectified output signal is available on P0[3]. This is routed to the Low Pass Filter having a cut off frequency of 2 kHz. This does not allow the rectified signal to pass through and thus gives a filtered DC voltage as output available on P0[5].

The project can be tested using the CY3210 – PsoC Eval1 board. The following connections may be made on the CY3210 board:

- Use the bread board area of the CY3210 to assemble R1 and C1.
- Connect the input signal of 20 kHz after the RC network to P0[1] on J6.
- The rectified output is available on P0[3] on J6.
- The filtered output is available on P0[5] on J6.
- The AGND is available on P0[4] on J6.

Operation

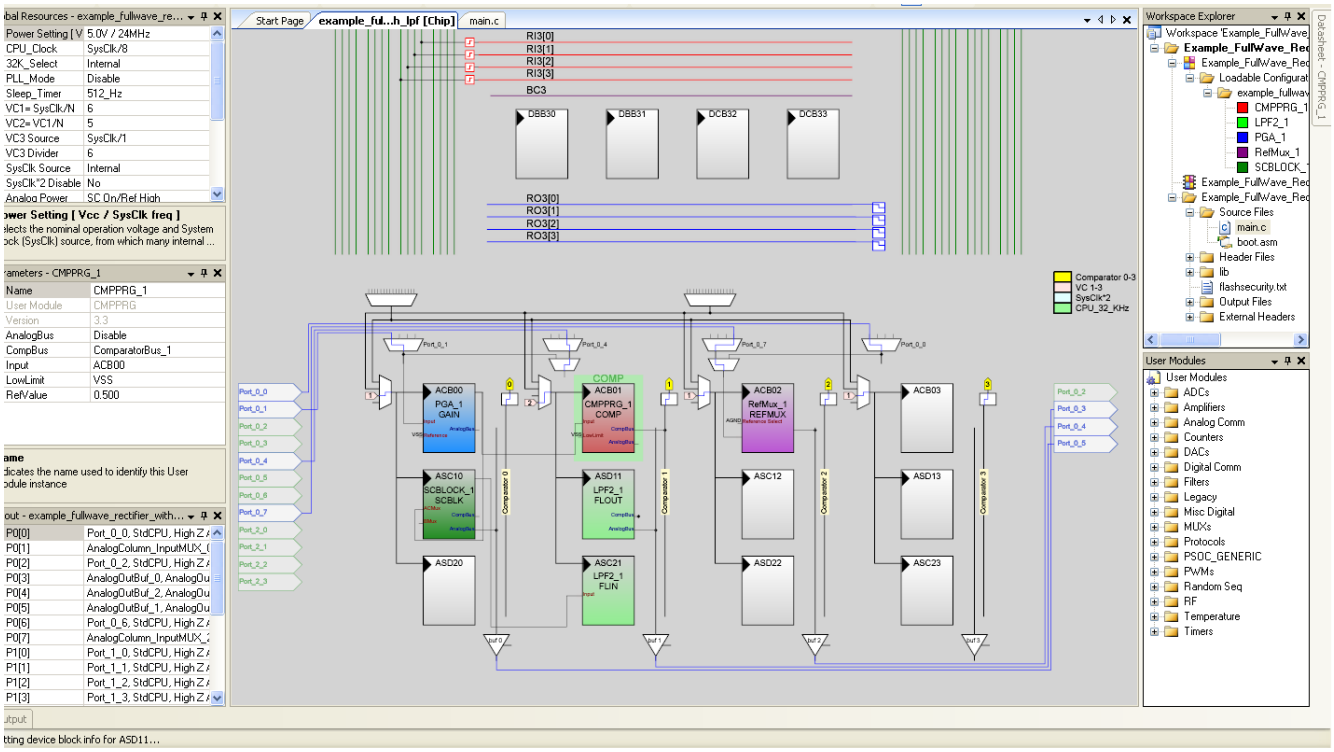
Figure 3. Block Diagram



The project works in the following manner:

- A RefMux user module placed in ACB02 is used to bring the AGND to P0[4].
- The input signal referenced to AGND is fed to a PGA placed in ACB00, configured as a unity gain amplifier.
- The output of the PGA feeds a CMPPRG placed in ACB01 and an SCBLOCK placed in ASC10.
- The CMPPRG is configured as a zero crossing detector with its threshold set at 0.5 * Vss, which is 2.5 V. The output of the CMPPRG is high when the input signal is positive and low when the input signal is negative.
- The SCBLOCK is configured as a unity gain amplifier by selecting Fcap = Acap = 16.
- The modulation source of the Rectifier is set to Comparator_Bus_1.
- The “Sign” parameter of the SCBLOCK and the Comparator Bus output are XORed and the result sets the sign of the SCBLOCK. As the “Sign” parameter of the SC Block is set to “Negative”, a HIGH from the CMPPRG results in a positive sign and LOW results in a negative sign.
- When the input signal is positive, the output of CMPPRG is HIGH; the sign is positive and, therefore, the output is also positive.
- When the input signal goes negative, the output of the CMPPRG is LOW; the sign is negative and the negative signal multiplied by negative sign results in a positive output.
- Therefore, the sign modulation of the SCBLOCK produces a full wave rectified output that is available at P0[3].
- This rectified output is passed through a low pass filter having a cut off frequency lower than the frequency of the rectified output.
- Therefore, the output available on the P0[5] is the filtered DC signal.

Figure 4. PSoC Designer Device Editor View



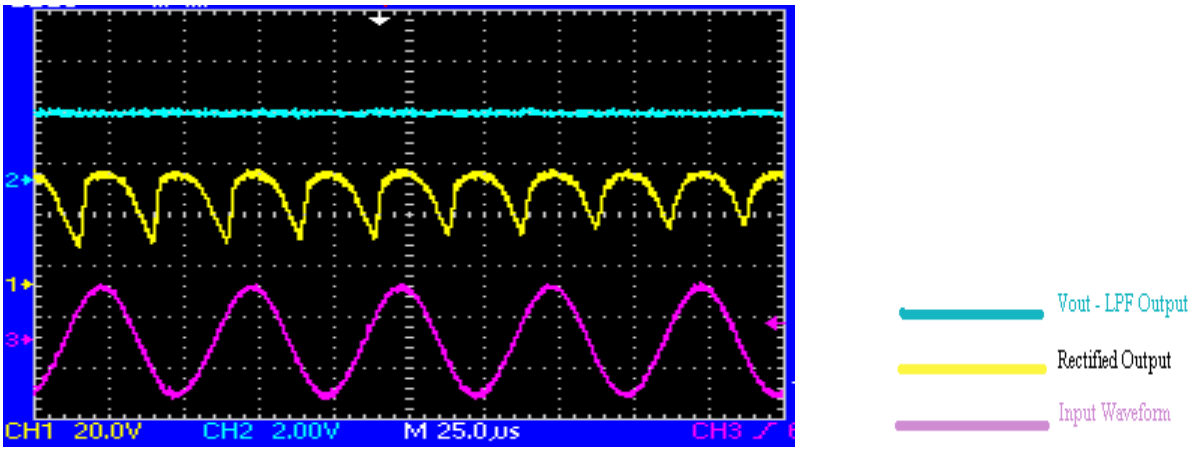
Firmware

The firmware of the project is simple. The following operations are done in *main.c*:

- Start all user modules in high power.
- The modulation source of SCBLOCK is set to Comp_Bus_1 by writing to the AMD_CR register.

Testing

Figure 5: Output Waveforms



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