1. SCH

FPGA part, HyperRam pins (HR\_\*) connect to different banks.







HyperRam:



2. All below waveforms are from Reveal logic analyzer in Lattice Radiant software.

Writing 8x64bits data, starting from address 0:



reading 1x64bits data from address0:



Read ID0:



1. Please note all those signals are before FPGA IO buffers, I am not able to probe HyperRan pins except DQ6 and DQ7.
2. I confirmed the waveform from DQ7 matches the waveform of merged signal from i\_hr\_dq\_i[15] and i\_hr\_dq\_i[7] ( i\_hr\_dq\_i is the 16bist bus after iddr from physical HR\_DQ bus of HyperRam, similar for i\_hr\_rwds\_i). So that means HyperRAM does respond.
3. If I hold reset at low, I will read all 0 values which is reasonable