Part No: 1ED3122MU12HXUMA1

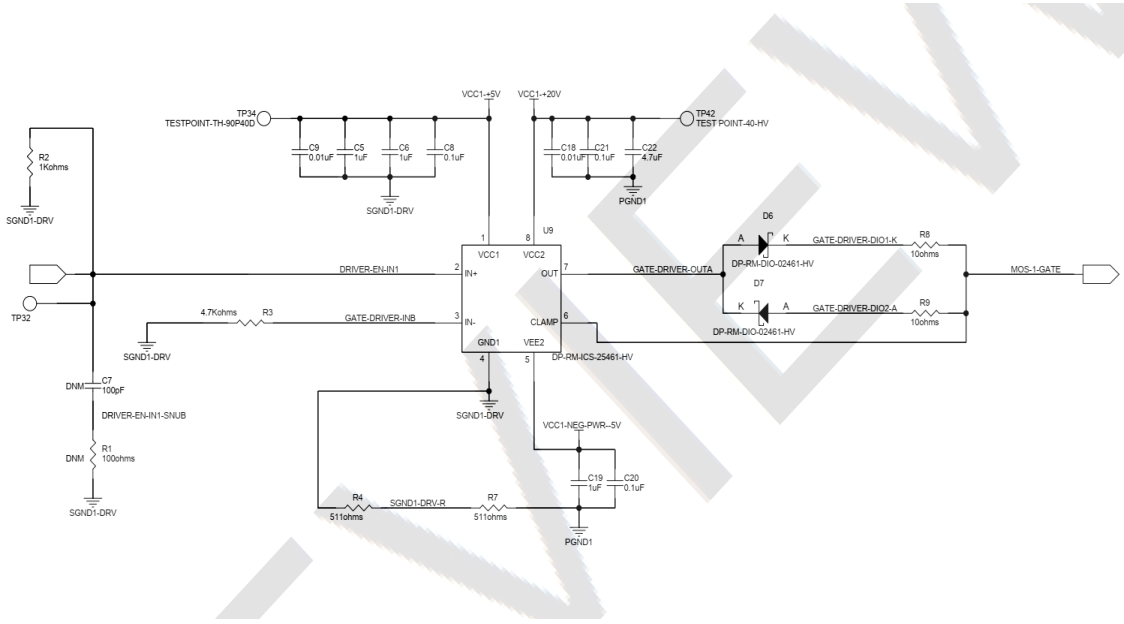

Figure 1 : Gate driver IC 1ED3122MU12HXUMA1 circuit

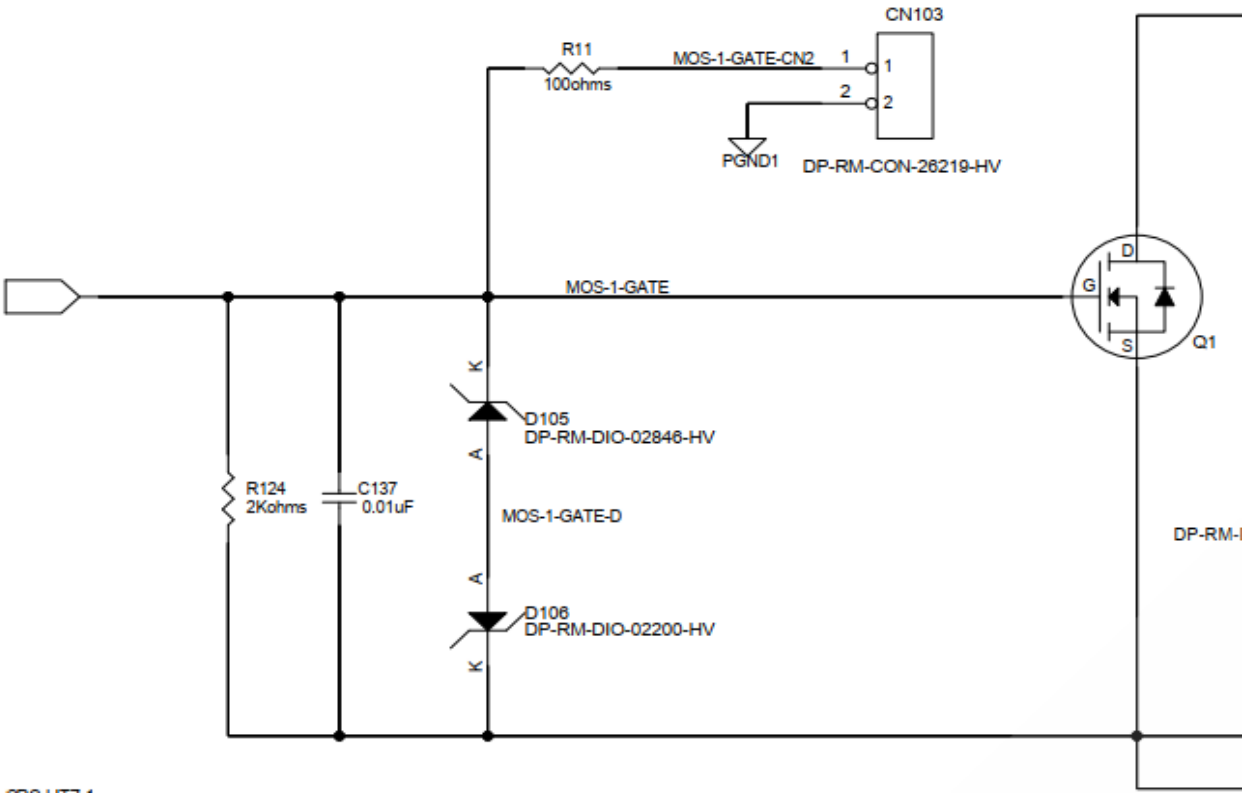

Figure 2 : MOSFET gate to source circuit.

Part No: 1ED3122MU12HXUMA1

In our application, -40kV is switched using 40 Nos of MOSFETs which are connected in series connection (Refer Fig). 40KV isolation is provided between each 1kV switching module and the controller module using isolation transformers. Each MOSFET's gate will be driven by the gate driver IC **1ED3122MU12HXUMA1**. VCC1 (+5V) and VCC2 (+20V) supplies of Gate driver IC are isolated supplies. The gate driver and MOSFET are connected as shown in the Figure 1 & Figure 2.

While switching the -40kV with 1us pulse width at 1Hz, the 39th MOSFET was observed as a false turn OFF at the driver output. In this scenario, input of the gate driver was normal with 1us pulse width, but the gate driver output was abnormal which means it was turned off approximately 300ns instead of 1us as shown in Figure 9 & Figure 10.

The bias supply for the switching module is isolated with 60KV isolation transformer as shown in the Block diagram Refer figure . The gate driver input is also 60KV Optically isolated.

Below mentioned the detailed analysis,

- **IN+** was measured and found OK as mentioned above.
- **IN-** pin is shorted to ground using 0 Ohm resistor.
- **VCC1** and **VCC2** were measured and found OK.
- **CLAMP** pin was measured at the time of false turn OFF, as it was directly short with the MOSFET gate terminal, the same wave form observed in the clamp pin.
- 2x 512 Ohms connected across **SGND1** & **PGND1** to limit the voltage built up between primary and secondary of gate driver IC. The voltage across the 2x 512 Ohms was measured as 700V during MOSFET switching.
- **OUT** pin was measured and found that it was turned OFF approximately 300ns instead of 1us.

There is no abnormalities such as UVLO, over current. dV/dt built up across SGND and PGND is within limit as mentioned in data sheet. So that, we could not come to a conclusion on this issue. Please help us to find out the issue.

Figure 3 : Gate to source Voltage(CH1 - Yellow) with respect to the IN+(CH2 - Blue) during normal condition

Figure 4 : Gate to source Voltage(CH1) with respect to the IN+(CH2) during false turn off condition

Figure 5 : Gate to source Voltage(CH1) with respect to the VCC2(CH2) during normal condition

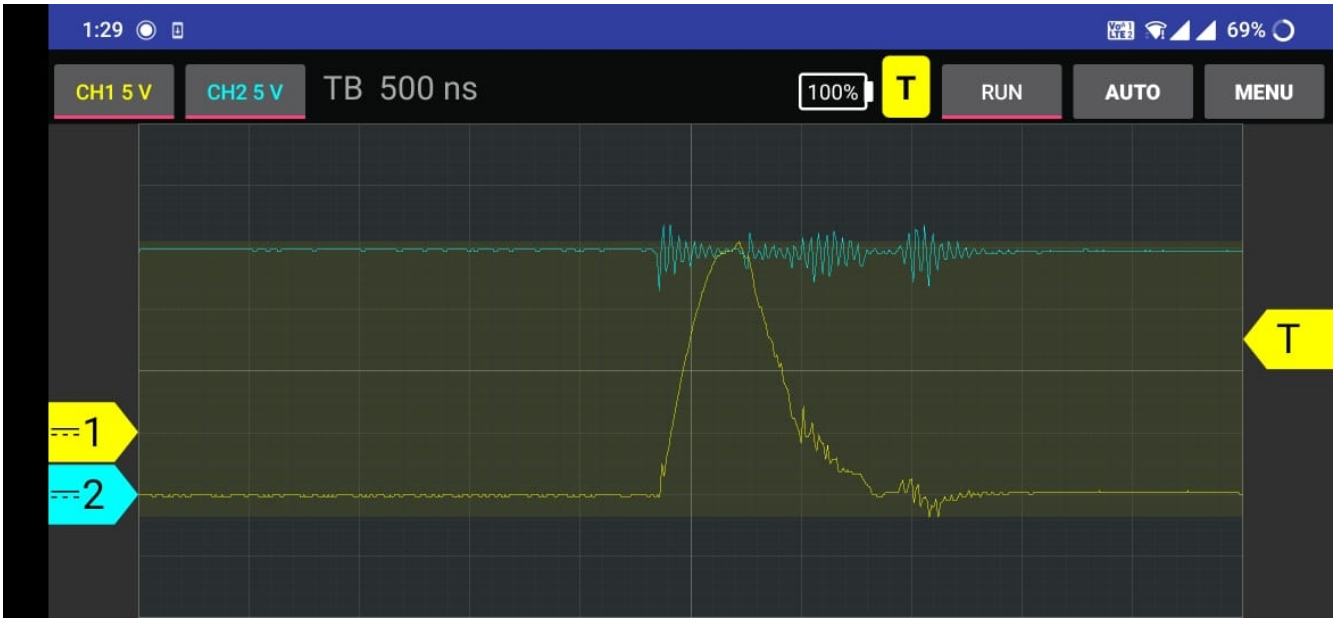

Figure 6 : Gate to source Voltage(CH1) with respect to the VCC2 (CH2) during false turn OFF condition

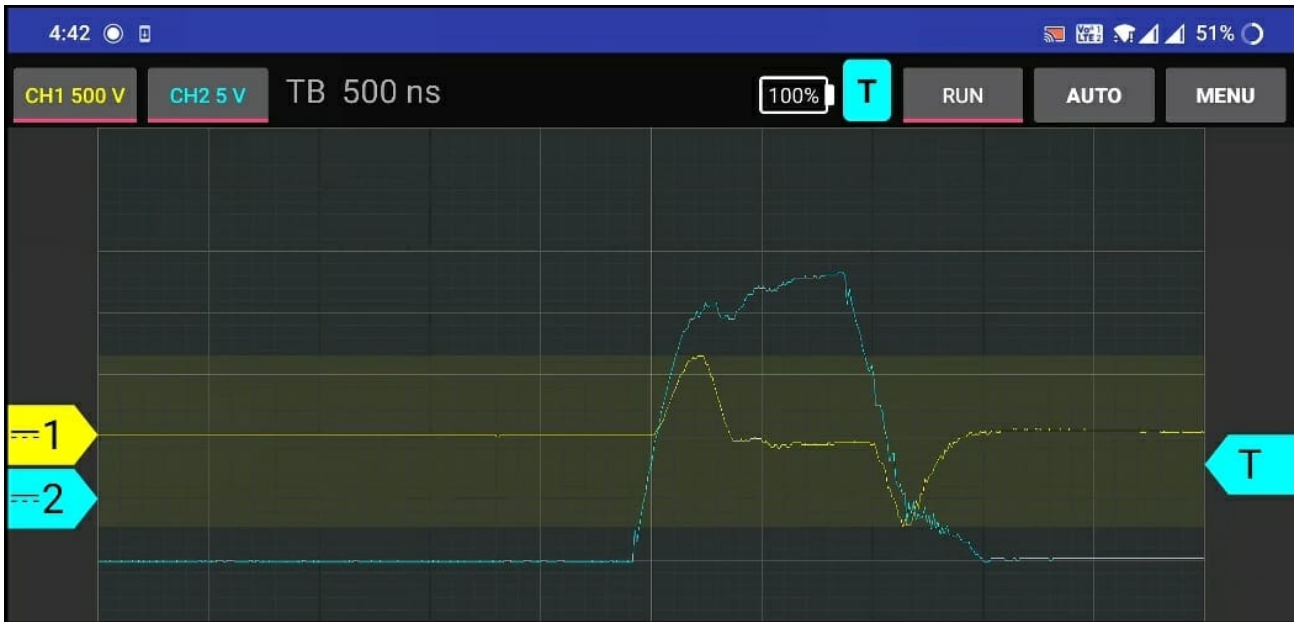

Figure 7 : Gate to source Voltage(CH2) & Voltage across GND1 & VEE2 capacitor ground(CH2) at normal condition

Figure 8 : Gate to source Voltage(CH2) & Voltage across GND1 & VEE2 capacitor ground(CH2) at false turn off condition

Figure 9 : Gate to source Voltage(CH2) with respect to the gate driver output(CH1) at normal condition

Figure 10 : Gate to source Voltage(CH2) with respect to the gate driver output(CH1) at false turn off condition

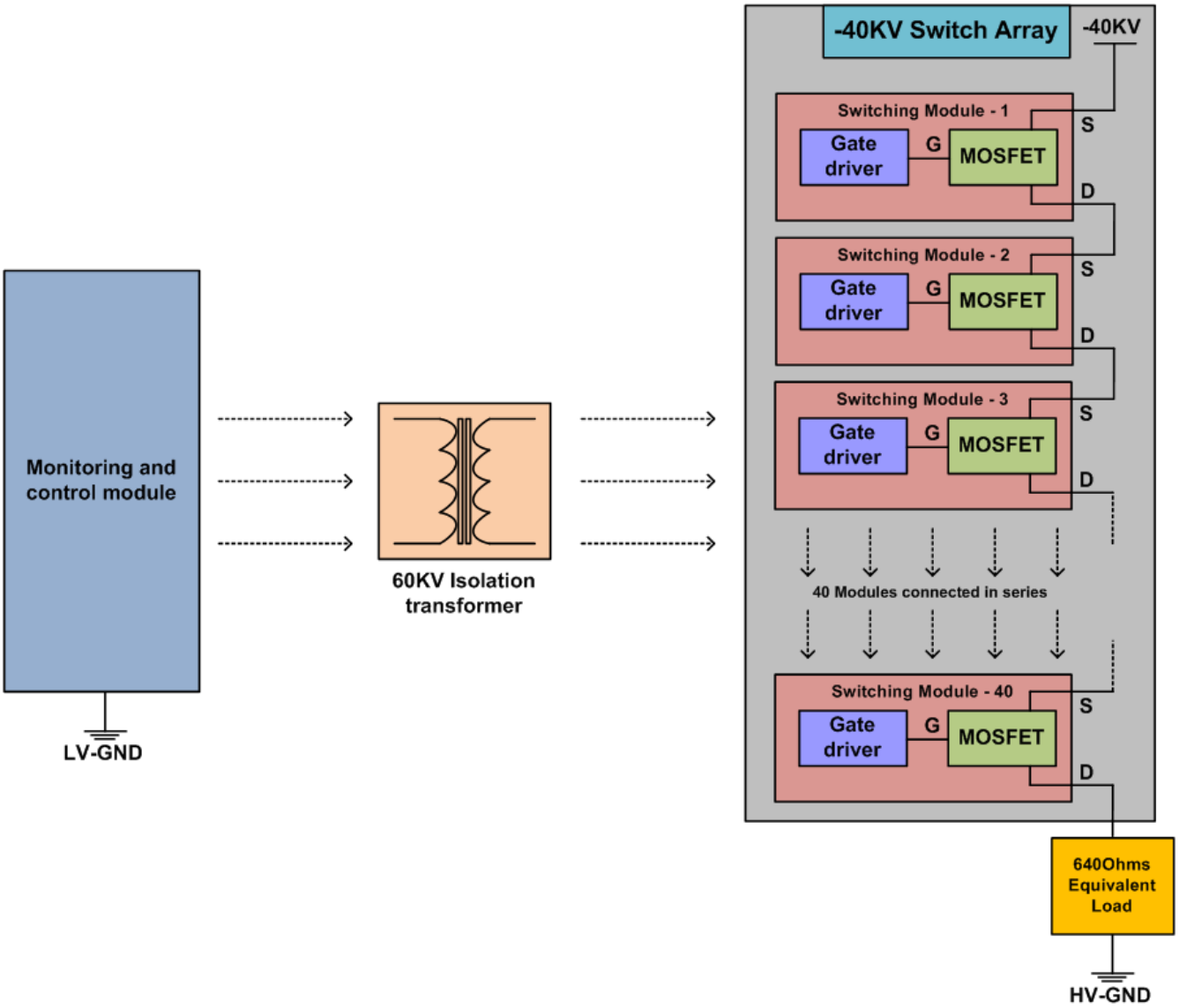

Figure 11 : Overall Block Diagram