AN2014-06 1EDC/1EDI Compact family technical description

Technical description

About this document

The Infineon EiceDRIVER™ 1EDC/1EDI Compact products are single channel high voltage gate driver ICs with integrated Coreless Transformer (CLT) technology and a maximum offset voltage of 1200 V. The undervoltage lockout levels of these family members are mainly designed for IGBT operation.

Scope and purpose

The scope of this application note includes an explanation of general gate driver input and output features, and a description of how to use them in an application.

Intended audience

This document is intended for application circuit designers and concept engineers in power electronics.

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1 Introduction

The Infineon EiceDRIVER™ 1EDC/1EDI Compact products are available in a UL1577 certified 300 mil package and in addition in 150 mil and 300 mil packages without certification.

Table 1 1EDC Compact 300 mil UL1577 certified device types

The wide body PG-DSO-8-59 (300 mil) package provides either separated source sink outputs or a single output with an additional clamping function. The undervoltage lockout levels of these devices are designed for IGBT operation. The variants are recognized under UL1577 for an insulation withstand voltage of 2500 V for 1 minute and an insulation test voltage of 3000 V for 1 second.

Product Name	Min. peak output current	Output configuration	Propagation delay	Undervoltage lockout Vcc2
	(source / sink) A		(tpy) ns	(off / on) V
1EDC05I12AH	0.5 / 0.5	Source / Sink	300	11.1 / 12.1
1EDC20I12AH	2.0 / 2.0	Source / Sink	300	11.1 / 12.1
1EDC20H12AH	2.0 / 2.0	Source / Sink	125	11.1 / 12.1
1EDC40I12AH	4.0 / 4.0	Source / Sink	300	11.1 / 12.1
1EDC60I12AH	6.0 / 6.0	Source / Sink	300	11.1 / 12.1
1EDC60H12AH	6.0 / 6.0	Source / Sink	125	11.1 / 12.1
1EDC10I12MH	1.0 / 1.0	Out / Clamp	300	11.1 / 12.1
1EDC20I12MH	2.0 / 2.0	Out / Clamp	300	11.1 / 12.1
1EDC30I12MH	3.0 / 3.0	Out / Clamp	300	11.1 / 12.1

Table 2 1EDI Compact 150 mil device types

The compact PG-DSO-8-51 (150 mil) package provides either separated source sink outputs or a single output with an additional clamping function. There are two optimized products available with undervoltage lockout levels for power MOSFETs.

Product Name	Min. peak output current	Output configuration	Propagation delay	Undervoltage lockout Vcc2
	(source / sink) A		(tpy) ns	(off / on) V
1EDI05I12AF	0.5 / 0.5	Source / Sink	300	11.1 / 12.1
1EDI20I12AF	2.0 / 2.0	Source / Sink	300	11.1 / 12.1
1EDI20N12AF	2.0 / 2.0	Source / Sink	125	8.6 / 9.4
1EDI40I12AF	4.0 / 4.0	Source / Sink	300	11.1 / 12.1
1EDI60I12AF	6.0 / 6.0	Source / Sink	300	11.1 / 12.1
1EDI60N12AF	6.0 / 6.0	Source / Sink	125	8.6 / 9.4
1EDI10I12MF	1.0 / 1.0	Out / Clamp	300	11.1 / 12.1
1EDI20I12MF	2.0 / 2.0	Out / Clamp	300	11.1 / 12.1
1EDI30I12MF	3.0 / 3.0	Out / Clamp	300	11.1 / 12.1

1 Introduction

Table 3 1EDI Compact 300 mil device types

The wide body PG-DSO-8-59 (300 mil) package provides either separated source sink outputs or a single output with an additional clamping function. The undervoltage lockout levels of these devices are designed for IGBT operation.

Product Name	Min. peak output current	Output configuration	Propagation delay	Undervoltage lockout Vcc2
	(source / sink) A		(tpy) ns	(off / on) V
1EDI05I12AH	0.5 / 0.5	Source / Sink	300	11.1 / 12.1
1EDI20I12AH	2.0 / 2.0	Source / Sink	300	11.1 / 12.1
1EDI20H12AH	2.0 / 2.0	Source / Sink	125	11.1 / 12.1
1EDI40I12AH	4.0 / 4.0	Source / Sink	300	11.1 / 12.1
1EDI60I12AH	6.0 / 6.0	Source / Sink	300	11.1 / 12.1
1EDI60H12AH	6.0 / 6.0	Source / Sink	125	11.1 / 12.1
1EDI10I12MH	1.0 / 1.0	Out / Clamp	300	11.1 / 12.1
1EDI20I12MH	2.0 / 2.0	Out / Clamp	300	11.1 / 12.1
1EDI30I12MH	3.0 / 3.0	Out / Clamp	300	11.1 / 12.1

Nomenclature

1EDiccs12fp: Lower case letters in the product name are placeholder for a single digit of the original product name.

- Type of insulation (i): C = certified insulation, I = galvanic insulation
- Gate driver output current (c): two digit number, scale 0.1 A
- Switch type optimization (s): H = high-speed IGBT, I = IGBT, N = n-channel MOSFET
- Output function (f): A = alternate source/sink output, M = active Miller clamp
- Package (p): F = 150 mil, H = 300 mil

2 Input Features

The input features of the gate driver IC include undervoltage lockout of input supply, pull-up and pull-down resistors of logic inputs and signal filtering.

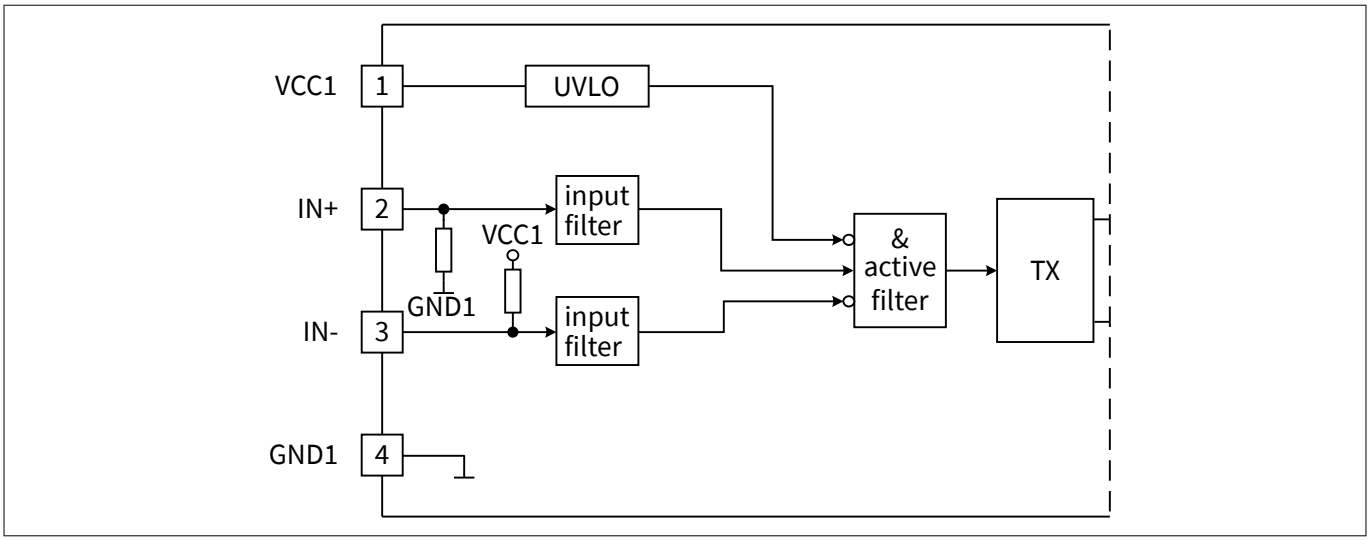

Figure 1 Block diagram of input section

The gate driver IC input section consists of the following functional blocks

- input undervoltage lockout circuit
- signal filtering
- pull-up resistor for inverting-input
- pull-down resistor for non-inverting-input
- signal transmission to isolated output section

2.1 Input supply and undervoltage lockout (UVLO)

The input supply range has absolute maximum ratings of -0.3 V to 18 V. Static operation beyond the absolute maximum voltage (abs max) damage internal structures and is therefore considered a forbidden area.

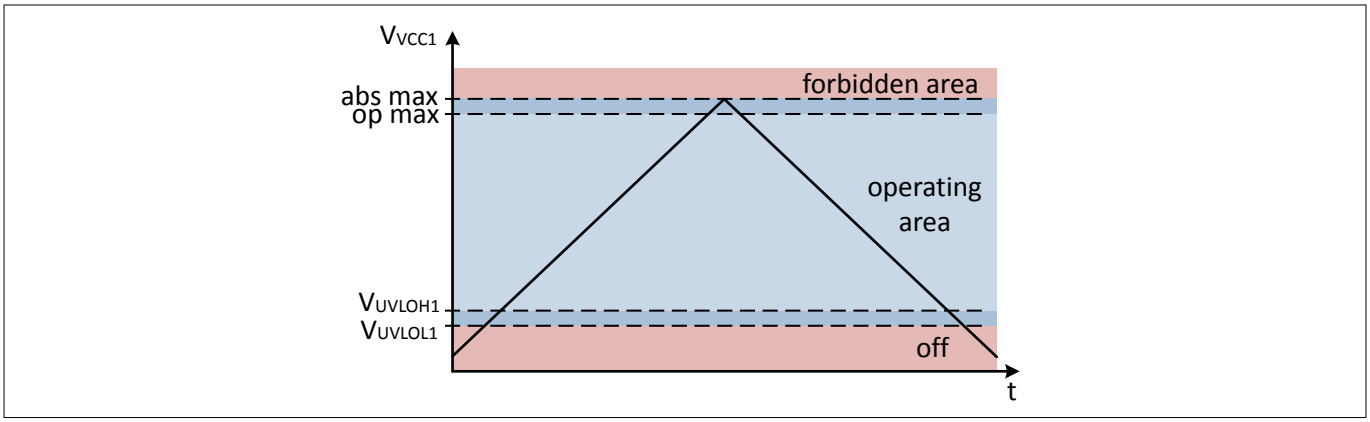

Figure 2 Input supply areas and UVLO threshold

At a crossing of the turn on undervoltage lockout threshold(V_{UVLOH1}) during a positive ramp at VCC1 pin the input section starts to operate. It is evaluating the input signals IN+ and IN- and transmits their current state to the output section. During V_{VCC1} ramp down and crossing of the turn off undervoltage lockout threshold (V_{UVLOL1}) the input section will send a final off signal regardless of the IN+ or IN- state. V_{UVLOL1} and V_{UVLOH1} form a hysteresis which offers stable operation even at low levels.

Any voltage overshoot above the absolute maximum voltage (abs max) rating can damage the driver circuits. In this area, the current consumption increases dramatically and therefore results in a violation of the maximum allowed input power loss. The operating area is defined between the turn on undervoltage lockout threshold (V_{UVLOH1}) and the maximum operating voltage (op max).

2.2 Pull-up and pull-down resistor for input signals

The input pull-up or pull-down resistors ensure an off state in case the corresponding input is not connected. These resistors have a minimum value of 25 kΩ. Even with the maximum allowed voltage at VCC1 pin the input current due to these resistors stays below 1 mA.

The pull-up and pull-down resistors are designed to be connected to an external supply or ground potential for permanent activation of the individual driver input.

2.3 Input signal filtering (active filter)

The input section of the driver IC filters both input signals to suppress short pulses triggered by external influences.

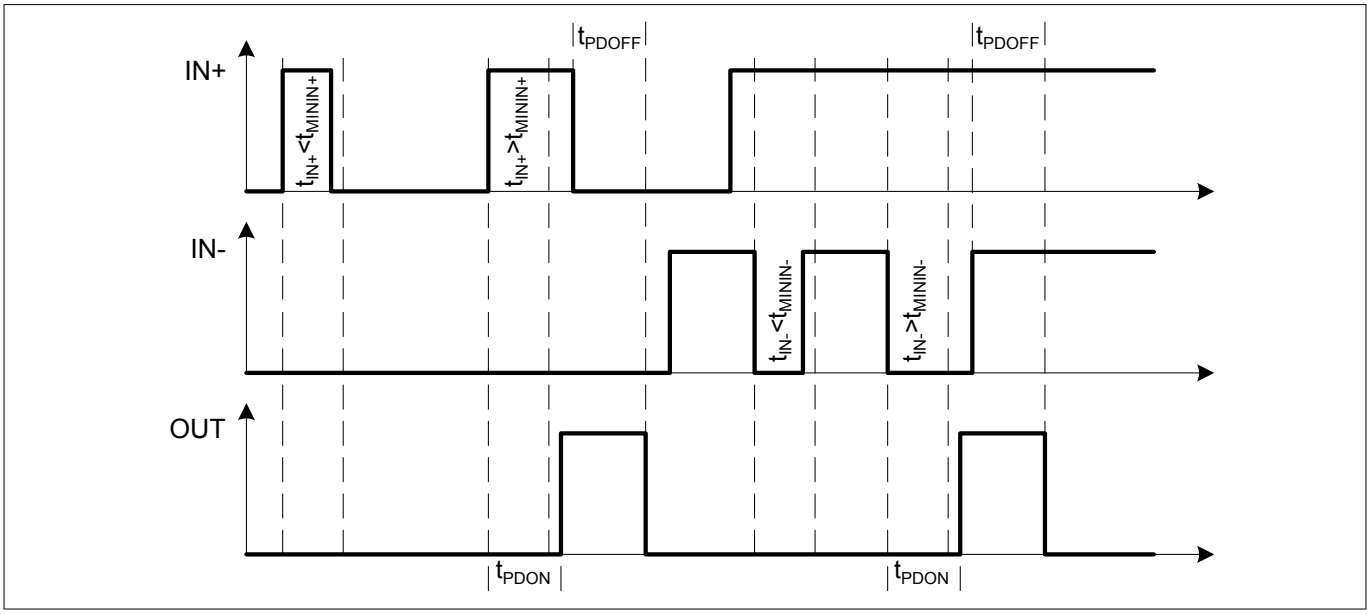

Figure 3 Input pulse suppression and turn-on / turn-off propagation delay

Every pulse at IN+ shorter than the input pulse suppression time for pin IN+ (t_{MININ+}) will be filtered and is not transmitted to the output chip. Longer pulses will be sent to the output with the shown propagation delay t_{PDON} and t_{PDOFF}. The same behavior is implemented at IN-. Every pulse shorter than the input pulse suppression time for IN- (t_{MININ-}) will be omitted and longer pulses transmitted with the same propagation delay.

Table 4 Typical filter and propagation delay times

The 1EDI Compact family offers two dedicated input filter times resulting also in two different propagation delay times. Lower case letters in the product name are placeholder for a single digit of the original product name.

- Type of insulation (i): C = certified insulation, I = galvanic insulation
- Gate driver output current (c): two digit number, scale 0.1 A
- Output function (f): A = alternate source/sink output, M = active Miller clamp
- Package (p): F = 150 mil, H = 300 mil

Product name	Input pulse suppression time (typ)	Propagation delay time (typ)
1EDiccI12fp variants	240 ns	300 ns
1EDIccN12AF variants, 1EDiccH12Ap variants	45 ns	125 ns

2.4 VCC1 scaled input threshold voltage

The threshold voltages of both input pins IN+ and IN- are scaled with the voltage level of V_{VCC1} within the operating range of 3 V to 17 V.

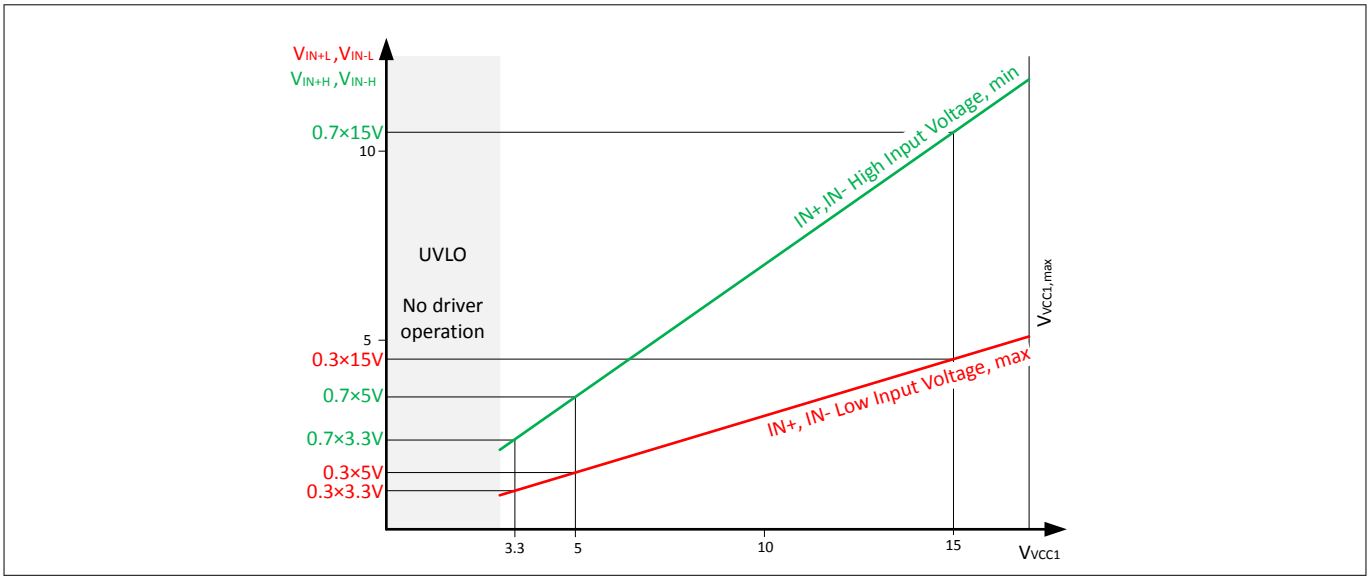

Figure 4 VCC1 scaled input threshold voltage of IN+ and IN-

Beginning from the input undervoltage lockout level, threshold levels for IN+ and IN- are scaled to V_{VCC1}. The high input threshold is 70% of V_{VCC1} and the low input threshold is at 30% of V_{VCC1}.

The inputs IN+ and IN- are rated up to 17V. The voltage level at the input pin can therefore be higher than the supply voltage level at VCC1. This higher input voltage compared to VCC1 results in an internal current from IN+ or IN- to VCC1. The total input current can therefore increase to a maximum value of 260 µA.

2.5 Application usage of IN+ and IN-

The inverting (IN-) and non-inverting (IN+) input pins offer multiple possibilities to connect PWM input and logic signals for various control and protection uses.

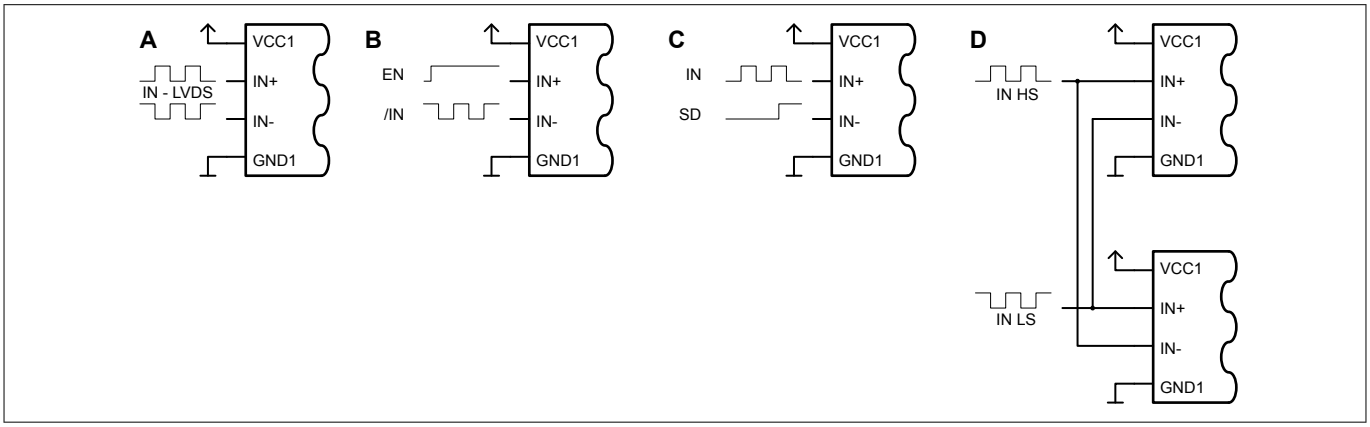

Figure 5 Input IN+ and IN- usage

Apart from using both inputs with a differential signal (A) (*VCC1* and *GND1* levels) using only one input signal for actual switch control leaves the second input available for functions like Enable (B), Shutdown (C) or Interlock (D).

A) Differential signal

Applying a logic level differential signal on both *IN+* and *IN-* with the positive level of *VCC1* pin and the negative level of *GND1* pin improves common mode noise rejection.

B) Enable

Using the *IN+* pin as enable signal leaves the *IN-* to control the output PWM with an inverted logic input signal. The enable signal can then be shared between gate driver ICs of a complete inverter to start operation with a single control signal.

C) Shutdown

Using the *IN-* pin as shutdown signal leaves the *IN+* to control the output PWM with a non-inverted logic input signal. The shutdown signal can then be shared between gate driver ICs of a complete inverter to interrupt operation with a single control signal.

D) Interlock

Interlocking is often used in half bridge configurations to avoid a shot through current from the high voltage DC bus supply. Connecting the following input signal pins of the top and bottom driver IC together inhibits a static turn on for both channels at the same time

- top driver non-inverting input (*IN+*) with the bottom driver inverting input (*IN-*)
- bottom driver non-inverting input (*IN+*) with the top driver inverting input (*IN-*)

Dynamic turn on and off characteristics of gate drivers and power switches can still lead to short term shot though. A proper deadtime setting at the PWM generation to avoid overlapping turn on times at the power switches is recommended.

3 Output Features

This section describes the gate driver output section of the variants with separate source/sink outputs and variants with single output and active miller clamp functionality.

3.1 Output supply and undervoltage lockout (UVLO)

The output supply range has a positive absolute maximum rating of 35 V for separate output variants and 20 V for variants with active miller clamp function. Separate output variants are therefore capable of providing a bipolar gate voltage to a connected power switch.

Table 5 Output undervoltage lockout voltage threshold levels

The undervoltage lockout thresholds of the different gate driver variants are optimized to be used with either IGBT or MOS based switches. Nevertheless, all variants provide unlimited functionality for use with both, IGBT as well as MOSFET.

Parameter	Symbol	Value	Unit
IGBT variant maximum turn on level	$V_{UVLOH2,IGBT}$	12.7	V
IGBT variant minimum turn off level	$V_{UVLOL2,IGBT}$	10.5	V
MOS/GaN variant maximum turn on level	$V_{UVLOH2,MOS}$	10.0	V
MOS/GaN variant minimum turn off level	$V_{UVLOL2,MOS}$	8.0	V

3.2 Active shutdown

The active shutdown function is a protection feature of the driver. It is designed to avoid a free floating gate of a connected power switch to trigger a turn on.

An external R_{GE} usually provides this protection. The active shutdown function is implemented in all variants and renders the use of this external resistor unnecessary.

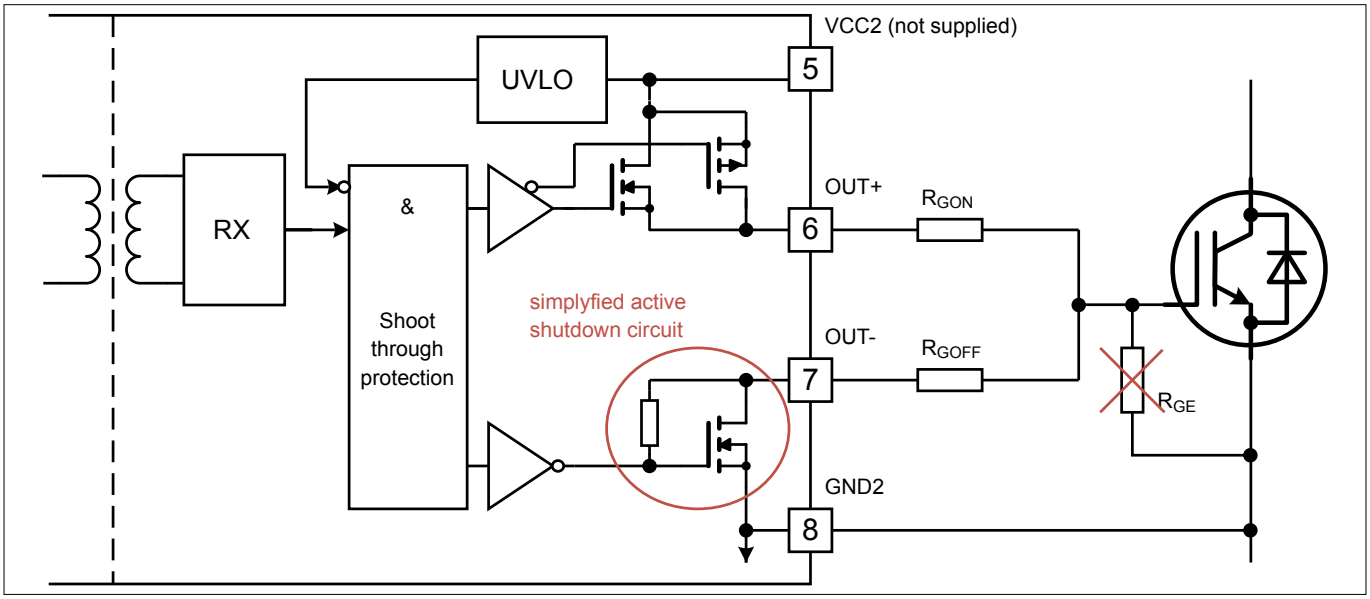

Figure 6 Block diagram of separate output variant showing active shutdown

In case of supply voltage failure at the VCC2 pin, the output section of the driver operates in the active shutdown mode. In this case the driver uses the floating voltage of the connected gate to supply this internal circuit. The maximum pull down current in this mode is approx. 10% of the rated output current of the individual driver variant. This solution is by far stronger than an otherwise used R_{GE}.

3.3 Separate Source / Sink Output Variants

With separated outputs for current sourcing and sinking in a gate driver IC individual gate resistors can be used for turning a power switch on and off.

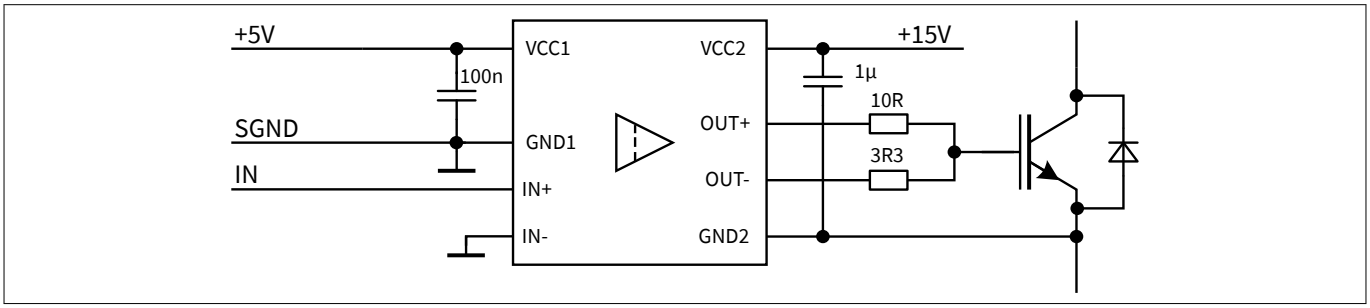

Figure 7 Circuit example for separate output variants

This optimization for a dedicated application saves a bypass diode for each power switch used.

It also helps reducing the gate loop by minimizing the number of components between the gate driver and the power switch. It minimizes as well the required PCB space. An additional benefit of two separated gate resistors is the power loss distribution. Because each of the two resistors are only active during turn on or turn off the power loss in each individual resistor is also only halved compared to a single gate resistor solution.

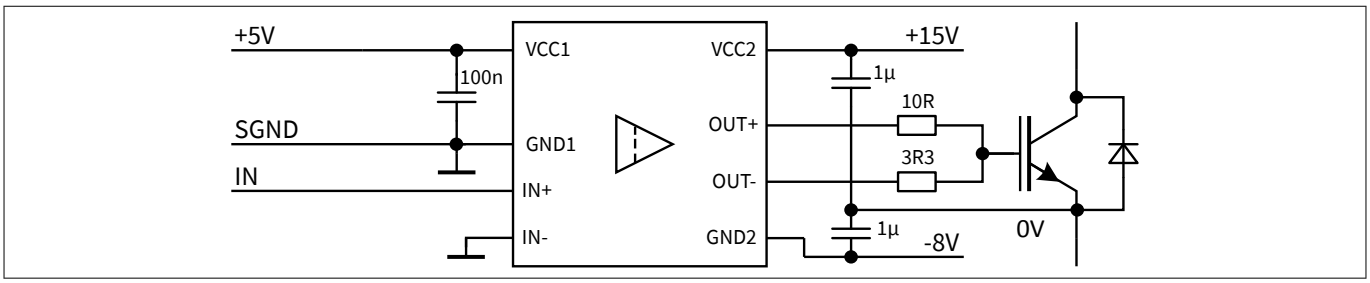

Figure 8 Circuit example for separate output variants for bipolar supply

The variants with separate outputs are also able to operate up to 35 V between VCC2 and GND2 pins. This allows a gate switching with for example 0 V to +15 V, -8 V to +15 V or -15 V to +15 V.

The connection of any voltage supply needs to connect the positive voltage to VCC2 pin, the negative voltage to GND2 pin and the reference supply pin to the emitter of an IGBT. This common ground level is then unknown to the driver IC and therefore the UVLO protection is referenced to the negative supply.

3.4 Out / Clamp Variants

In these variants a common output for turn-on and turn-off is combined with a separate pin for active miller clamping. They are also optimized for single supply voltage of up to 20 V between VCC2 and GND2 pins.

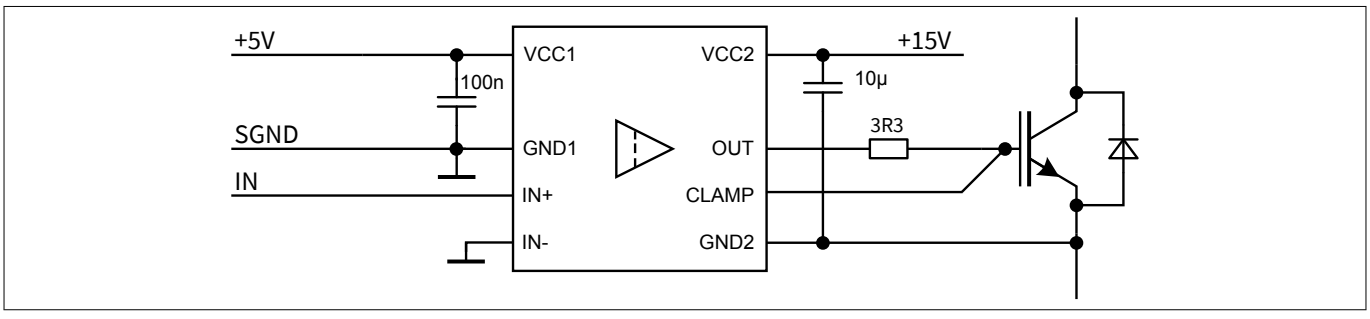

Figure 9 Circuit example for clamp variants

The active miller clamping function reduces the risk of a parasitic turn on during a high dv_{CE}/dt transition at the connected IGBT. Displacement currents through the intrinsic gate-collector (C_{GC}) and gate-emitter (C_{GE}) capacitances can lead to an increase at v_{GATE}. If the voltage reaches the IGBT threshold a dynamic turn on of the power switch occurs. It stays on until the regular discharge path through R_G can reduce the gate voltage again.

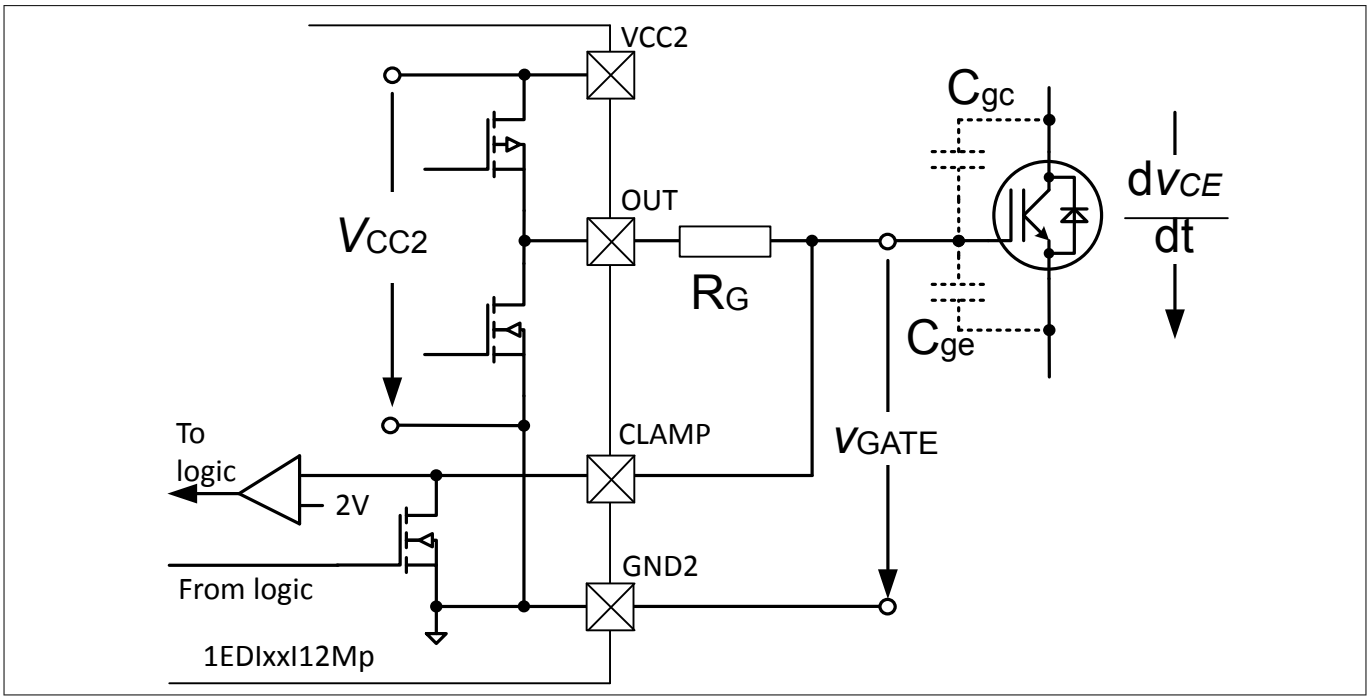

Figure 10 Output block diagram for clamp variants

The implemented clamp function of the 1EDI Compact monitors the gate voltage during driver off state. It activates the additional discharge path between CLAMP and GND2 as soon as the gate voltage sinks below 2 V. The clamping circuit stays active until the driver is turned on again. To achieve the most effective clamping results, the circuit layout between gate and CLAMP pin must be optimized for lowest possible inductance.

4 Design Aspects

The design aspects describe gate resistor and output supply capacitor selection as well as the power dissipation estimation for a selected design.

4.1 Output supply capacitor selection

A general design rule for the location of the driver output supply capacitor is always as close to the IC's supply pins VCC2 and GND2 as possible.

Additionally the value of the capacitor needs to be big enough to limit the voltage drop during the power switch turn on. The following equation helps to calculate a first approximation for this capacitor.

$$C_2 = \frac{I_{Q2} \cdot t_p + Q_G}{\Delta V_{CC}} \cdot 1.2$$

Equation 1

I_{Q2} is the gate driver supply current, t_P the period of the switching frequency, Q_G the total gate charge at the selected operating condition and ΔV_{CC} the maximum allowable voltage variation. The additional margin of 20% covers typical tolerances of capacitor and gate charge parameters.

Calculating this for the 100 A Module FP100R12KT4 with Q_G = 800 nC, a switching frequency of f_{sw} = 15 kHz and an acceptable voltage variation of ΔV_{CC} = 0.2 V results in

$$C_2 = \frac{2mA \cdot 67\mu s + 800nC}{500mV} \cdot 1.2$$

$$C_2 = 2.24\mu F$$

Equation 2

4.2 Gate resistor selection

To optimize the gate resistor it is recommended to have the appropriate gate charge diagram of the used IGBT and the output characteristic of the gate driver ready. Both diagrams are depending on operation conditions such as DC-link voltage (VDC), collector current (IC) and operating temperature.

The following representative diagrams show typical behaviors of an IGBT and the 1EDI Compact driver output without scale.

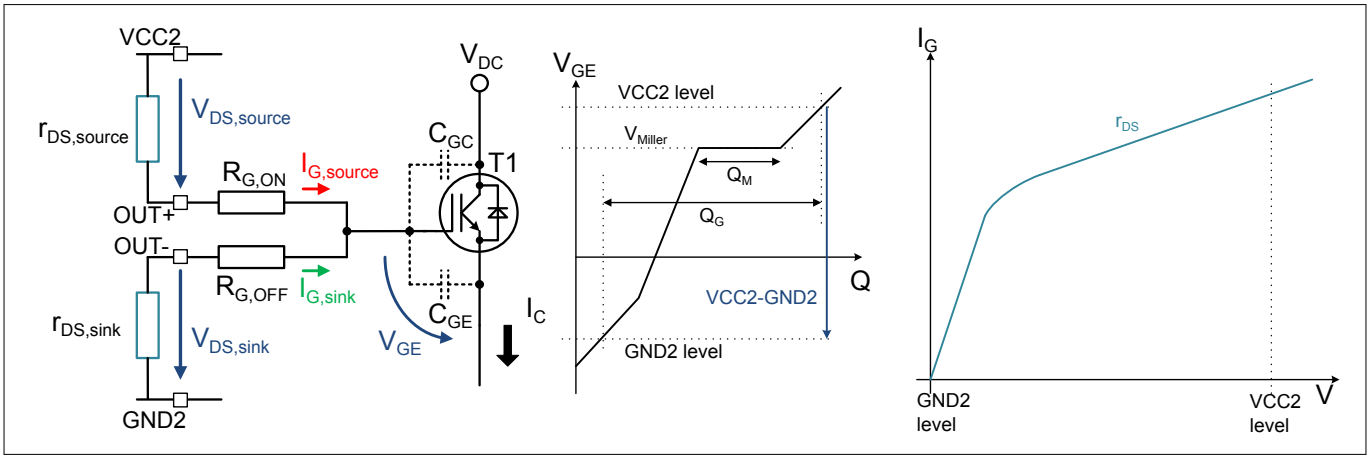

Figure 11 Simplified gate circuit, IGBT gate charge diagram and driver output characteristic

The MOSFET based gate driver outputs can be simplified as dynamic resistors ($r_{DS,source}$; $r_{DS,sink}$) with a voltage drop ($V_{DS,source}$; $V_{DS,sink}$) during switching. The total gate charge (Q_G) and the Miller charge (Q_M) can be extracted from the gate charge diagram using the given gate driver supply $V_{(VCC2-GND2)}$ and DC-link voltage.

4 Design Aspects

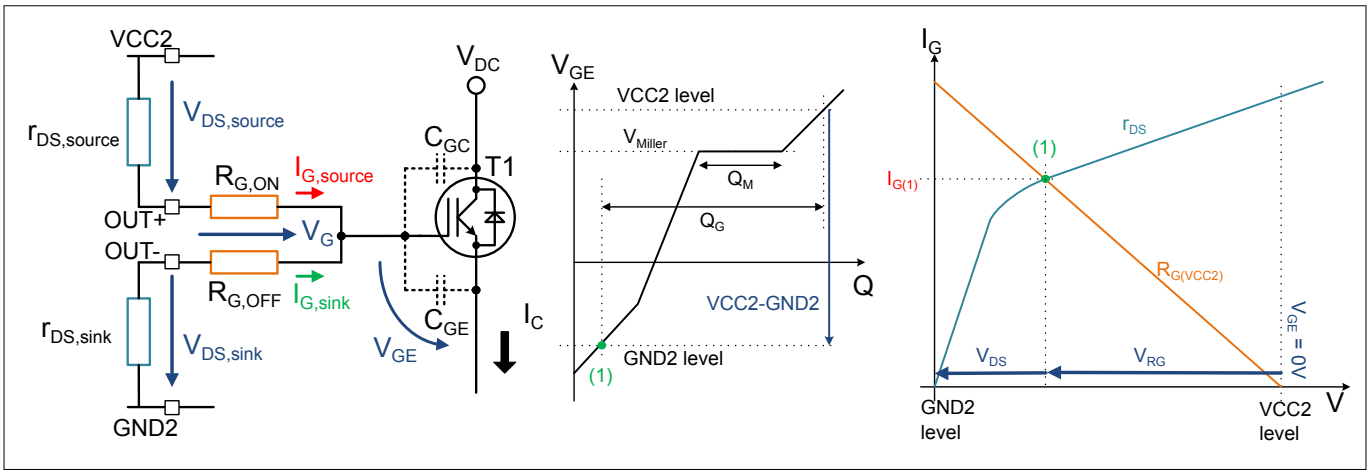

Figure 12 Simplified gate circuit turn on event: Initial phase

In the initial phase of an IGBT turn on event the gate is discharged and at the level of the GND2 pin. In the diagram this is marked with (1). Therefore the total gate supply voltage is split between the inner gate driver resistance ($r_{DS,source}$) and the turn on gate resistor ($R_{G,ON}$). The graphical solution shows the initial gate current ($I_{G(1)}$). This maximum current can also be used to select the appropriate pulse current class for the gate resistor.

Immediately after the initial phase the gate current starts to fall, following the crossing point of the output characteristic curve and the parallel translated gate resistor line while the gate-emitter voltage (V_{GE}) charges up.

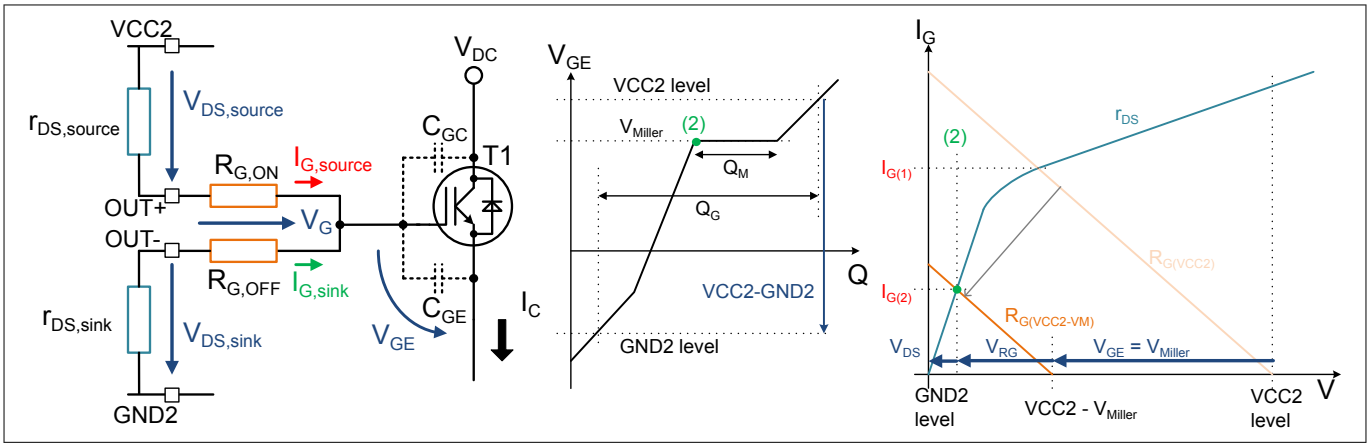

Figure 13 Simplified gate circuit turn on event: at Miller plateau

Beginning with the Miller plateau, marked with (2) above, the gate-emitter voltage remains nearly constant while the transistor is reducing the collector-emitter voltage to its saturation level.

Given the condition at that phase the resulting gate current is constant, allowing a collector-emitter voltage transition time (tON) calculation with the following formula:

$$t_{ON} = \frac{\left(R_{G,ON} + r_{DS,source(2)}\right)}{\left(V_{CC2} - V_M\right)} \cdot Q_M$$

$$t_{ON} = \frac{1}{I_{G(2)}} \cdot Q_M$$

Equation 3

Tuning the value of a gate resistor requires extensive knowledge of all the parasitics in the gate circuit. It is therefore an iterative process of adjusting between switching losses and EMI.

4.3 Power dissipation estimation

Apart from the power losses in the gate resistor during switching of any power switch, there is also considerable power loss inside the driver IC.

Every package can achieve a maximum power dissipation at a certain operating condition without violating the maximum junction temperature. The internal power loss of the output section (P_{OUT}) of the 1EDI Compact driver can be estimated as follows:

$$P_{OUT} = P_Q + P_{source} + P_{sink}$$

Equation 4

P_Q is the operating power loss of the driver output stage. It is easily calculated by the operating supply current (I_{Q2}) and the supply voltage between VCC2 and GND2 pins:

$$P_Q = I_{Q2} \cdot (VCC2 - GND2)$$

Equation 5

The turn-on (P_{source}) and turn-off (P_{sink}) losses can be estimated using the resistive voltage divider between inner gate driver resistance (R_{DS}) and outer gate resistor (R_G) with the total gate charge (Q_G) and switching frequency (f_{sw}):

$$P_{source} = \frac{1}{2} Q_G \cdot f_{sw} \cdot (VCC2 - GND2) \cdot \frac{R_{DS,source}}{R_{DS,source} + R_{G,ON}}$$

$$P_{sink} = \frac{1}{2} Q_G \cdot f_{sw} \cdot (VCC2 - GND2) \cdot \frac{R_{DS,sink}}{R_{DS,sink} + R_{G,OFF}}$$

Equation 6

Table 6 Gate driver output resistance

Lower case letters in the product name are placeholder for a single digit of the original product name.

- Type of insulation (i): C = certified insulation, I = galvanic insulation
- Switch type optimization (s): H = high-speed IGBT, I = IGBT, N = n-channel MOSFET
- Package (p): F = 150 mil, H = 300 mil

Driver type	$R_{DS,source}$ output resistance		$R_{DS,sink}$ output resistance	
	typ [Ω]	max [Ω]	typ [Ω]	max [Ω]
1EDi60s12Ap	0.75	1.4	0.75	1.7
1EDi40I12Ap	1.13	2.2	1.13	2.7
1EDi20s12Ap	2.25	4.3	2.25	5.0
1EDi05I12Ap	9.00	16	9.00	17
1EDi30I12Mp	1.50	2.8	1.50	3.4
1EDi20I12Mp	2.25	4.3	2.25	5.0
1EDi10I12Mp	4.50	8.6	4.50	10

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