Advanced Gate Drive Options for Silicon-Carbide (SiC) MOSFETs using EiceDRIVER™

About this document

Scope and purpose

This application note discusses the basic parameters of silicon-carbide (SiC) MOSFETs and derives gate drive requirements. The document considers the following EiceDRIVER™ products.

- 1EDI05I12Ax, 1EDI20I12Ax, 1EDI40I12Ax, 1EDI60I12Ax
- 1EDI20N12AF, 1EDI60N12AF
- 1EDI20H12AH. 1EDI60H12AH
- 1EDI10I12Mx, 1EDI20I12Mx. 1EDI30I12Mx
- 1ED020I12-F2, 1ED020I12-B2, 1ED020I12-FT, 1ED020I12-BT
- 1EDI20I12SV, 1EDS20I12SV
  ("x" = "F" or "H", depending on the package option)

These gate driver IC families provide galvanic isolation. Using isolated gate drivers for SiC MOSFET is not necessarily a mandatory requirement. However, ultra-fast switching 1200 V power transistors can be handled easier by means of isolated gate output sections. Therefore, this document concentrates on suitable galvanically-isolated EiceDRIVER™ ICs. The gate drive proposals are backed up with useful schematic or layout information.

It is also important to note that Infineon´s advanced CoolSiC™ Trench-MOSFET technology offers various benefits which allow simplified gate driving, which are mentioned in detail in this document. It is important to note that this document does not refer to SiC bipolar transistors or SiC JFETs.

Intended audience

This application notes give helpful information for power system hardware engineers and PCB layout engineers.

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1 Summary

For each gate driver IC, the availability of properties and supporting functions for driving SiC MOSFET is listed in Table 1. The most important parameters (shown with shaded rows at the beginning of the table) are tight propagation delay matching, precise input filters, wide output side supply range, negative gate voltage capability, and the extended CMTI capability.

Table 1 Gate driver IC functions and properties important for SiC MOSFET

Function / property	1EDI Compact Family "x" = package options ("F" or "H")											1ED-F2 Family			SRC Family	
	1EDI20H12AH	1EDI60H12AH	1EDI20N12AF	1EDI60N12AF	1EDI05I12Ax	1EDI20I12Ax	1EDI40I12Ax	1EDI60I12Ax	1EDI10I12Mx	1EDI20I12Mx	1EDI30I12Mx	1ED020I12-F2	1ED020I12-B2	2ED020I12-F2	1EDS20I12SV	1EDI20I12SV
Delay matching < 35 ns	✓	✓	✓	✓	—	—	—	—	—	—	—	—	—	—	✓	✓
Precise input filters < 150 ns	✓	✓	✓	✓	—	—	—	—	—	—	—	—	—	—	—	—
Wide output supply range	✓	✓	✓	✓	✓	✓	✓	✓	—	—	—	✓	✓	✓	✓	✓
Negative gate voltage	✓	✓	✓	✓	✓	✓	✓	✓	—	—	—	✓	✓	✓	✓	✓
Extended CMTI	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	—	—
Fast DESAT	—	—	—	—	—	—	—	—	—	—	—	✓	✓	✓	✓	✓
Two-level Turn-off	—	—	—	—	—	—	—	—	—	—	—	—	—	—	✓	✓
Closed-loop gate current control	—	—	—	—	—	—	—	—	—	—	—	—	—	—	✓	✓
UVLO ≈ 12 V	✓	✓	—	—	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
Act. Miller Clamp	—	—	—	—	—	—	—	—	✓	✓	✓	✓	✓	✓	—	—
Best use for	**Half-Bridge / Neg. Gate Voltage**				**Half-Bridge**				**Single transistor, Low d*V*/dt**			**Fast DESAT**				

The most suitable gate drivers without short circuit detection are 1EDI20H60AH and 1EDI60H60AH in a wide-body DSO8 package (300 mil) and 1EDI20N60AF and 1EDI60N60AF in a 150 mil DSO8 package. If a fast short circuit protection is required, the 1ED-F2 family fits best.

Single-transistor converter topologies such as boost, buck, forward, or flyback converters in combination with CoolSiC™ MOSFETs benefit most from 1EDI10I12MF, 1EDI20I12MF, and 1EDI30I12MF due to the integrated active-miller-clamp function. These three gate driver ICs may be also an option for applications with low dV_{DS}/dt and where a unipolar gate voltage is sufficient.

2 SiC MOSFET gate-drive requirements and options

This section derives necessary and optional requirements out of the SiC MOSFET general properties to drive the gates of SiC MOSFET properly.

2.1 Synchronous rectification

Half-bridge configurations, if they operate inductive loads such as motors in PWM mode, need a freewheeling path during the deadtime and during the off-state interval of the switch. The freewheeling path is automatically established by means of the SiC MOSFET´s body diode. It is good practice to support the body diode´s forward operation by turning on the transistor part of the MOSFET as well where the MOSFET´s channel operates in reverse direction. This kind of half-bridge control opens a path in parallel to the body diode through the channel of the MOSFET. This is called synchronous rectification.

The advantage of such an operation mode is that the channel usually generates a lower voltage drop compared to the forward voltage of the body diode. This operation mode is important for SiC MOSFET because the forward voltage of its body diode is relatively high according to Figure 1 showing the forward voltage at the lowest operating gate voltage. It is therefore mandatory for high system efficiency to avoid the mode with just the diode conduction as much as possible.

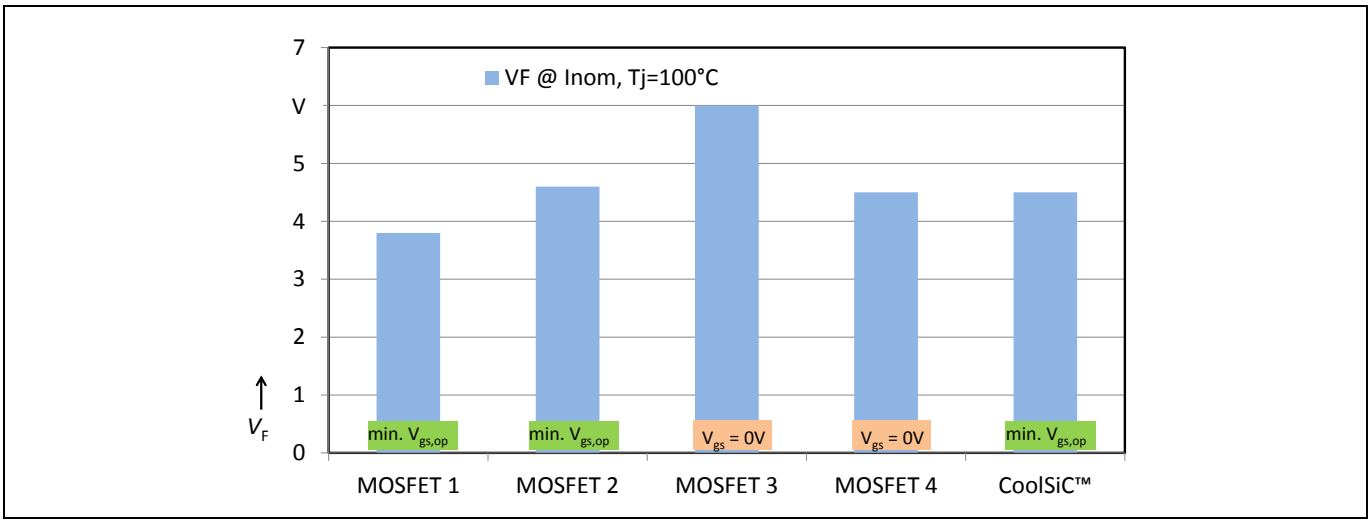

Figure 1 Forward voltage V_F of SiC MOSFET body diodes at lowest gate voltage conditions

2.2 Enable short deadtimes for high efficiency

Deadtimes inhibit a short shoot through current (cross conduction) in a half bridge. This is an important safety factor of any half-bridge application. On the other hand, having deadtime can lead to efficiency reduction or output power limitation, because no energy is converted into the load during the deadtime. Achieving as short a deadtime as possible without shoot-through is therefore essential in high performing power electronics. The most important aspects to this goal are a precise propagation delay matching and precise integrated filters, which are explained in the following sections.

2.2.1 Precise propagation delay matching

Important components of a gate driver IC's deadtime calculation are the propagation delay from input to the output, the rise, and the fall time. Since the rise and fall times are largely insignificant, sometimes even in a single digit nanoseconds range, it is not such an important parameter to look at. This is different for the control signal's propagation delay. The datasheet specification of galvanically isolated EiceDRIVER™ products includes usually the parameter variation over temperature, and the ICs lifetime. This often yields in a much larger single parameter tolerance in the datasheet compared to the real

tolerance of two parts being operated under the same conditions. Therefore, the difference of the propagation delay between any two components under the same conditions is considered by means of the propagation delay matching. The tight matching of propagation delays is mandatory to reduce that portion of the deadtime, which is necessary due to the gate driver´s tolerances. Examples for the tight propagation delay matching are shown in Table 2.

Table 2 Maximum propagation delay mismatching with and without temperature influence

IC sales code x = F or H (package options)	Max. delay matching	Max. delay matching incl. temperature variation
1EDI05I12Ax, 1EDI20I12Ax, 1EDI40I12Ax, 1EDI60I12Ax	40 ns	48 ns
1EDI20N12AF, 1EDI60N12AF	25 ns	29 ns
1EDI60H12AH. 1EDI60H12AH	25 ns	33 ns
1ED020I12-F2, 1ED020I12-B2 2ED020I12-F2	25 ns	45 ns
1EDI20I12SV, 1EDS20I12SV (with respect to slew rate control)	—	30 ns

It is important to know that the individual combination of SiC MOSFET and gate driver IC has to be evaluated carefully for dimensioning the deadtime properly. The turn-on and turn-off propagation delays of the power transistor very often differ much more over the operating conditions (such as the gate voltage range, drain-source voltage V_{ds}, junction temperature T_{vj}, or gate resistance) than propagation delays of the gate driver IC. Thus the parameters of SiC MOSFET can dominate the deadtime calculation.

2.2.2 Precise integrated filters

Filtering of input control signals is a state-of-the-art method to avoid wrong triggers caused by electrical noise. There are two ways of filtering often used in power electronics:

- RC-filters at control input terminals
- Combination of a RC-filter with short filter time and a precise integrated filter in the gate driver IC itself.

An external RC-filter substantially helps to stay inside the IC´s absolute maximum voltage ratings. These ratings usually specified for a negative voltage of only –0.3 V. There is a high risk that any coupling likely violates this rating when not using such a RC-filter. The capacitive portion of the filter helps to stay inside the operating range while the resistive portion limits coupled currents stressing any IC terminal. It is therefore the best choice to design a RC-filter with a short filter time constant in the range of a few nanoseconds and have a capacitor close to the ICs terminals. The IC itself should take over the effective filtering of larger disturbances.

The two filtering methods are investigated here in a case study. The first method suffers from the relatively flat branch of a RC charging curve as shown in the left graph in Figure 2. The component tolerances of the filter resistor and filter capacitor have big influence here regarding the filter time. The left graph shows the influence of component tolerances regarding the filter time tolerance. It can be seen that the minimum to maximum spread $t_{max} – t_{min}$ is not symmetrical with respect to the target value t_{trig}.

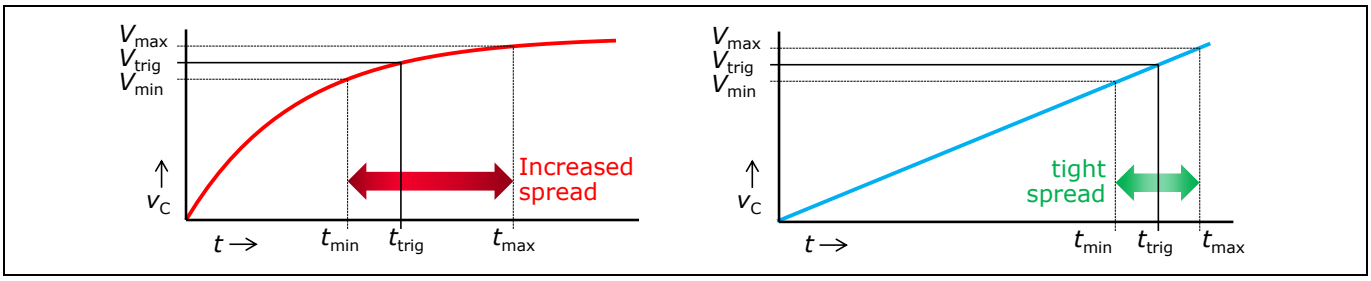

Figure 2 Different filter topologies (left: RC-filter, right: integrated filter with short time RC-filter)

The right graph in Figure 2 depicts the time behavior of a short filter time RC filter combined with a dominating integrated filter. The spread of filter time regarding the target value is rather symmetric here and tighter than with a single RC-filter only. Therefore, an integrated filter is superior to solutions having only an RC-filter as long as the maximum voltage specifications are no concern.

2.3 Negative gate voltage

Figure 3 shows an overview of selected SiC MOSFETs regarding their gate-source threshold voltage $V_{gs(th)}$. It can be seen that the Infineon´s CoolSiC™ technology provides the highest gate-source threshold voltage levels in the market. These high levels may allow even to operate the CoolSiC™ transistors with positive gate voltage only. Examples and conditions for such an operation mode are explained in section 4.

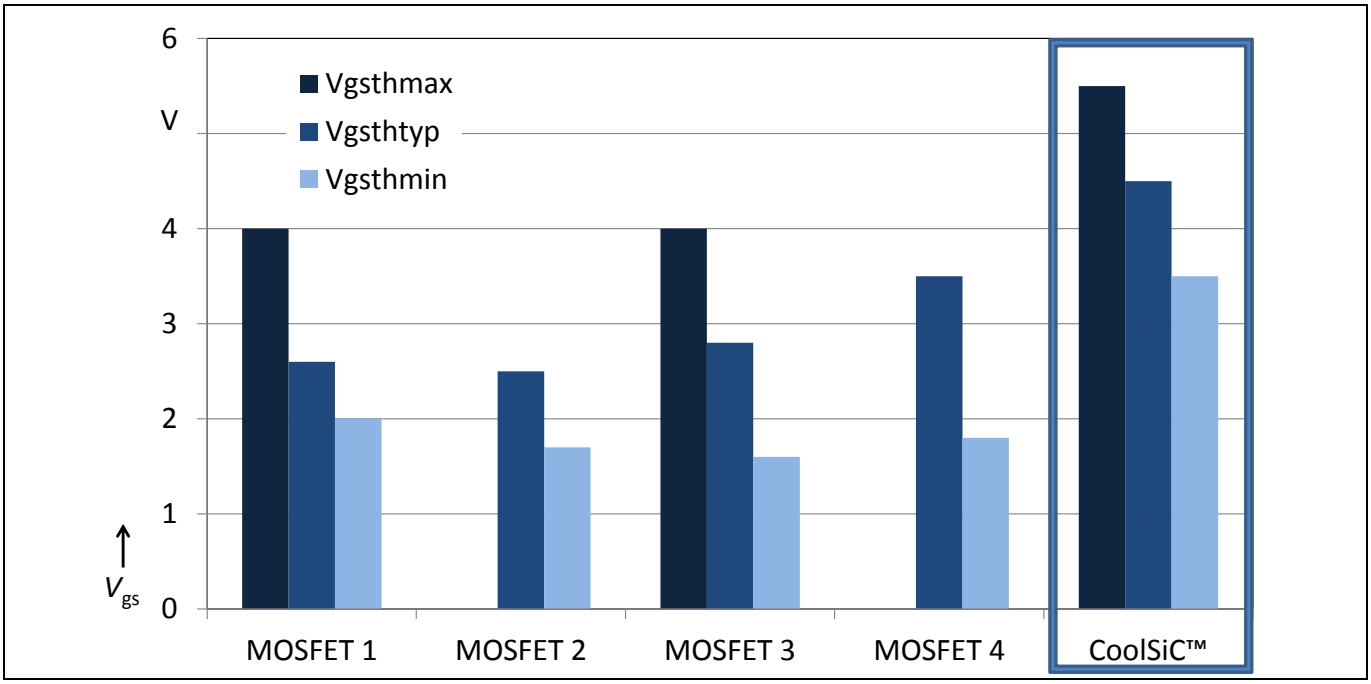

Figure 3 Gate-source threshold voltage range of SiC MOSFET

The minimum gate-source threshold voltage $V_{gs(th)}$ of other SiC MOSFET devices can be lower than 2 V at 25°C in some cases. Therefore, minor ground bouncing can lead to an uncontrolled turn-on of the MOSFET when using an off-state voltage of zero Volts. This situation could get more critical if one takes the temperature drift of the gate-source voltage threshold into account. A negative turn-off gate voltage can relax the situation and keeps the MOSFET in off-state even in noisy environments. On the other hand, it is known that too low negative gate voltages can limit the lifetime of such MOSFETs. The level of the negative gate voltage depends on the gate-source threshold voltage as well as on the required gate charge for turning on the MOSFET.

Thus, the driver ICs for SiC MOSFET should have the capability of managing a small negative gate voltage in order to provide a safe and stable off-state condition of SiC MOSFET.

As long as the absolute maximum ratings of the IC are not exceeded, any EiceDRIVER™ IC could be used to drive SiC MOSFETs. Nevertheless, it is recommended to use the driver ICs which provide the capability of working with negative gate voltages. Table 3 shows the maximum ratings of EiceDRIVER™ ICs for the maximum output supply voltage range V_{VCC2} - V_{VEE2} and V_{VCC2} - V_{GND2} respectively. The schematics for driving a negative gate voltage are depicted in Figure 4.

Figure 4 shows examples of gate drive circuits using negative gate-source voltages. The left schematic of Figure 4 represents the implementation if the EiceDRIVER™ IC does not provide specific terminals for negative gate-source voltage, such as the 1EDI05I12AF, 1EDI20N60AF, 1EDI60I12AH or 1EDI20H12AH. The right schematic of Figure 4 depicts a gate drive circuit of a driver IC with dedicated terminals for negative gate voltage, such as 1ED020I12-F2.

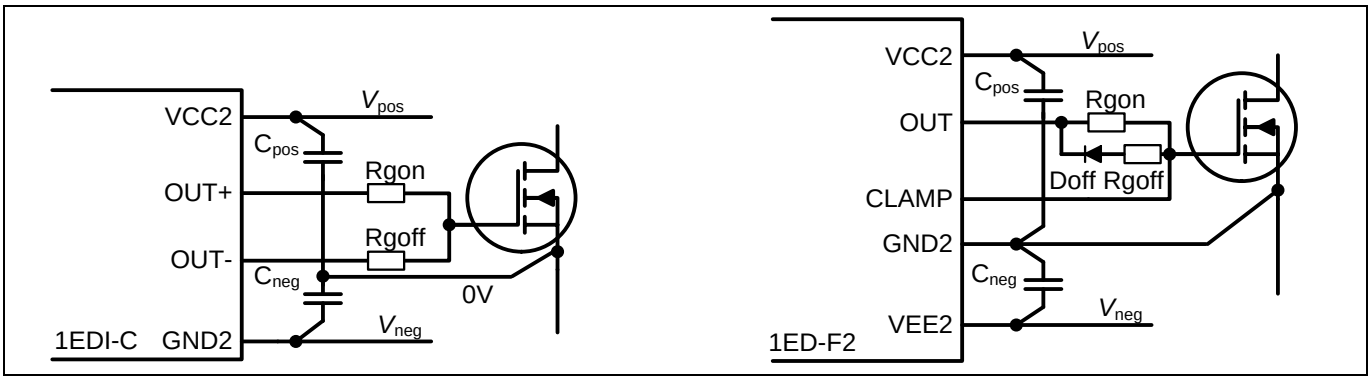

Figure 4 Schematic example for using negative gate voltage (left: EiceDRIVER™ with virtual reference point, right: EiceDRIVER™ with negative gate voltage capability)

The generation of the positive gate voltages on the output can be realized easily with isolated SMPS or by means of bootstrapping. However, the realization of the negative portion of the gate voltage requires normally a SMPS. The principle of such SMPS is discussed in [1] and [2]. However, these examples are designed for gate voltage ranges suitable for IGBTs and thus could not be used directly for SiC MOSFETs. One has to be aware that considerable displacement currents can flow through the parasitic coupling capacitances of such SMPS transformers. Such currents can have negative influence to the application´s sensing functions.

2.4 Wide range of gate voltages

The positive gate-source voltage defines the on-state $R_{DS(on)}$ of the SiC MOSFET. It can easily be seen in Figure 5 that Infineon´s CoolSiC™ transistors achieve their nominal on-state $R_{DS(on)}$ at a gate voltage of 15 V. This is a big benefit in numerous applications, because no changes have to be considered for the positive gate voltage supply compared to IGBT or even to conventional silicon MOSFETs.

Other SiC MOSFETs reviewed require a relatively high gate voltage, even compared to IGBT or to conventional silicon MOSFETs. A lower gate voltage level is of course possible, but it results in an increase of the steady-state channel resistivity and therefore in higher conduction losses. Figure 5 shows the absolute maximum ratings of the gate-source voltages V_{gs} of selected SiC MOSFETs in full shaded colors. The red colored bars represent the negative gate-source voltage and the blue bars the positive gate-source voltage. The light shaded bars depict the recommended gate-source voltage levels as per the datasheet of each device. The gate driver IC has to fulfill the range of positive and the negative gate voltage for optimized operation of the SiC MOSFET.

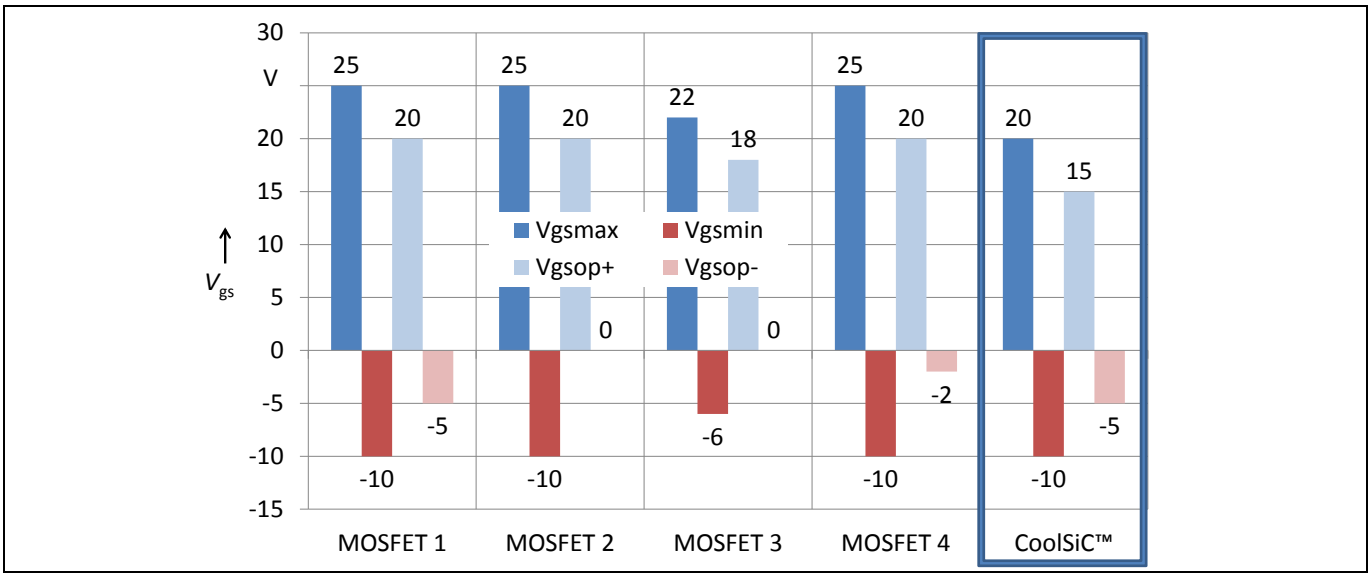

Figure 5 Gate-source voltage range of SiC MOSFET (full shaded: absolute maximum rantings, light shaded: recommended range as per datasheet)

As can be seen in Figure 5, the largest gate-voltage range of 25 V is required for MOSFET 1. Other MOSFETs such as MOSFET 4 also require a range beyond 20 V. However, the majority of SiC MOSFETs including CoolSiC™ can be driven with a total supply voltage range below $V_{pos} – V_{neg}$ = 20 V. This can be achieved theoretically by any EiceDRIVER™ specifying a maximum supply voltage of only 20 V. However, voltage spikes can easily exceed this maximum rating for a very short time. It is therefore recommended to select EiceDRIVER™ ICs with a rating for the output supply range V_{VCC2} - V_{VEE2} or V_{VCC2} - V_{GND2} of at least 25 V for a reliable gate drive circuit design. Exceptions of this recommendation are discussed in section 4. Table 3 shows these parameters for the products under discussion.

Table 3 Output voltage parameters relevant for driving SiC MOSFETs

IC sales code x = F or H (package options)	Max. output supply range V_{VCC2} - V_{VEE2} / V_{VCC2} - V_{GND2}	Min. negative gate voltage
1EDI05I12Ax, 1EDI20I12Ax, 1EDI40I12Ax, 1EDI60I12Ax*	40 V	V_{VCC2} – 40 V
1EDI20N12AF, 1EDI60N12AF	40 V	V_{VCC2} – 40 V
1EDI60H12AH. 1EDI60H12AH	40 V	V_{VCC2} – 40 V
1EDI10I12Mx, 1EDI20I12Mx, 1EDI20I12Mx	20 V	V_{VCC2} – 20 V
1ED020I12-F2, 1ED020I12-B2 2ED020I12-F2	28 V	-12 V
1EDI20I12SV, 1EDS20I12SV (with respect to slew rate control)	28 V	-12 V

2.5 Extended common mode transient immunity (CMTI) capability

The extremely fast switching capability of voltage amplitudes up to 900 V or higher requires an extended CMTI robustness from the gate driver IC. Both fall and rise times of SiC MOSFET are very short. A maximum rating of 100 V/ns is currently for EiceDRIVER™ ICs. The current standard VDE0884-10 for magnetic and capacitive couplers specifies a measurement procedure, which demands CMTI tests with rising and falling edges of the applied voltage slope. This gives a good comparability of CMTI specifications of various driver ICs.

The EiceDRIVER™ portfolio is divided into two groups of ICs. The first group offers a CMTI capability of 50 V/ns:

- 1EDI20I12SV, 1EDS20I12SV

The second group offers an extended capability to withstand higher common mode transients. This is specified up to 100 V/ns.

- 1EDI05I12AF, 1EDI20I12AF, 1EDI40I12AF, 1EDI60I12AF
- 1EDI20N12AF, 1EDI60N12AF
- 1EDI05I12AH, 1EDI20I12AH, 1EDI40I12AH, 1EDI60I12AH
- 1EDI60H12AH. 1EDI60H12AH
- 1ED020I12-F2, 1ED020I12-B2
- 1ED020I12-FT, 1ED020I12-BT

2.6 Fast DESAT detection

SiC MOSFETs do not have a sharp saturation behavior under conditions with excessive currents. Short circuit current levels can therefore easily reach 15 times the nominal current rating and are much higher compared with IGBT operation. Therefore the short circuit withstand time of SiC MOSFETs is approximately 3 µs and relatively short. A fast detection and a fast shut down are therefore mandatory for a reliable operation of SiC MOSFETs and long lifetime. Suitable techniques for overload handling of SiC MOSFETs are a fast DESAT function and the two-level turn-off function, which are explained in detailed below.

The well-known desaturation detection circuit for IGBTs can be used SiC MOSFETs as well. It is based on a monitoring of the drain-source voltage. Several parasitic effects of power diodes and the IGBT itself, as well as layout crosstalk during the current commutation, require a so-called DESAT blanking time in the range of several µs, maybe up to 7 – 8 µs. Such a long blanking time is not acceptable for SiC MOSFET as described above. A well optimized layout is mandatory to detect the short circuit condition safely and to avoid false DESAT triggers by means of ground bounce or signal cross talk. Refer to the technical description of the driver IC used for further information about adjusting the DESAT components R_{DESAT}, C_{DESAT}, and D_{DESAT}.

A suitable way to avoid such effects is to apply all rules for a good PCB layout. One of these rules is to optimize for small PCB track loops in the IC´s supplies, in the IGBT gate control, and in the DC-link as indicated in Figure 6. This avoids parasitic stray inductances which could lead to inductive coupling of switched currents.

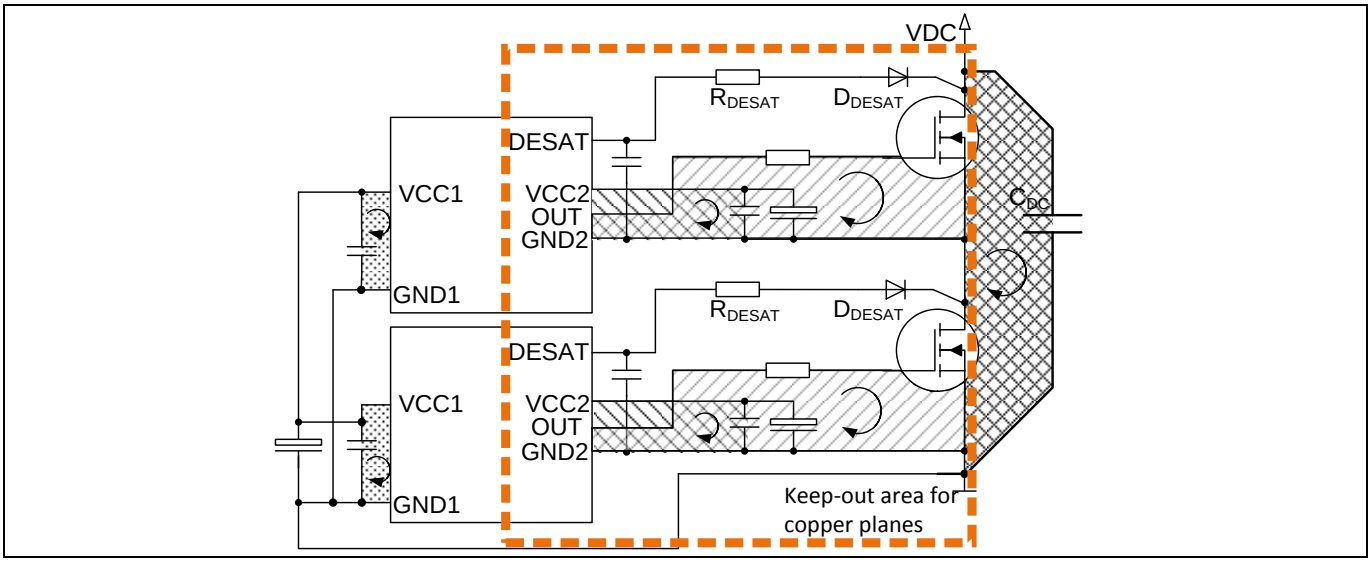

Figure 6 Example of a suitable layout for a fast DESAT detection function

Specific care is required to avoid parasitic capacitive coupling. The fast switching speed of SiC MOSFET is not comparable at all with the switching speed of IGBT. It is therefore recommended to keep the area of the gate drives circuit free of planes, which are connected to GND1, or GND2 or VDC. This measure avoids unnecessary capacitive coupling with high d*V*/dt. Note however that this approach may result in a conflict with the cooling demands of the gate driver IC, which may recommend specific copper areas.

The placement of the DESAT diode D_{DESAT} and resistor R_{DESAT} and the routing of the DESAT sense track have to avoid both inductive and capacitive coupling in order to generate a DESAT signal with minimum noise.

The following gate driver products in the EiceDRIVER™ family provide the DESAT function:

- 1ED020I12-F2, 1ED020I12-B2,
- 1ED020I12-FT, 1ED020I12-BT
- 1EDI20I12SV, 1EDS20I12SV

2.7 Active Miller clamping

Active Miller clamping is a well-known technique to avoid parasitic dV_{ds}/dt triggered turn-on. This function uses a CLAMP terminal, which is directly connected to the power transistor´s gate terminal as shown in Figure 7, and pulls down the gate during off-state. The off-state condition is monitored by sensing the instantaneous gate voltage with the same terminal. The clamp function is activated as soon as the gate voltage drops below a specified threshold which is typically V_{CLAMP} = 2.0 V.

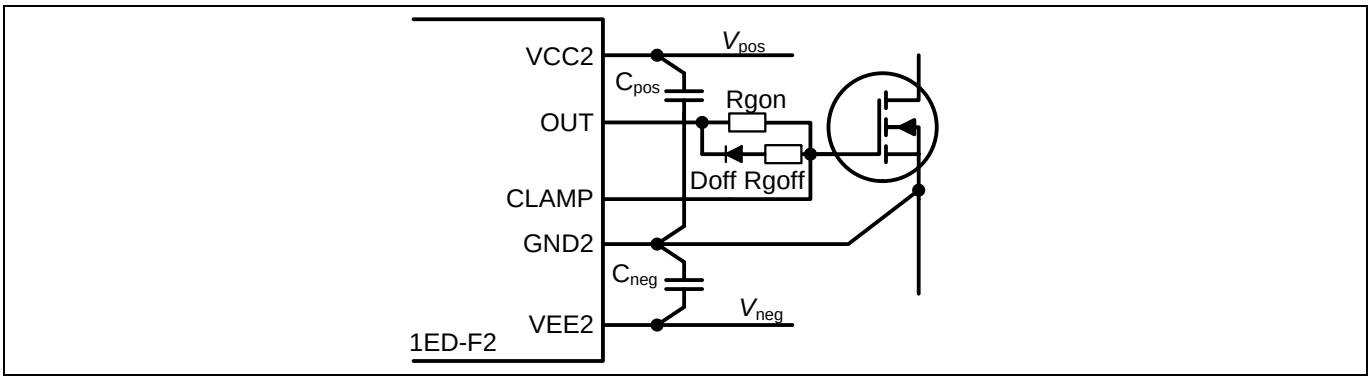

Figure 7 Schematic example for implementation of the active Miller clamp function.

The monitoring comparator threshold V_{CLAMP} is referenced to the lowest available voltage inside the IC. The lowest voltage occurs at terminal VEE2 of the 1ED-F2 family or at terminal GND2 of the 1EDI compact family.

Even though the 1EDI Compact family offers variants having an active Miller clamp function, one has to be aware that this family supports basically positive gate voltage only. However, several applications cases do allow a positive only gate voltage. Please refer to section 4 for further background information.

Isolated EiceDRIVER™ ICs with active miller clamp and a positive only gate voltage supply are:

- 1EDI10I12MF, 1EDI10I12MF, 1EDI10I12MF,

Isolated EiceDRIVER™ ICs with active miller clamp in combination with a DESAT function:

- 1ED020I12-F2, 1ED020I12-B2,
- 1ED020I12-FT, 1ED020I12-BT

3 Power dissipation

The calculation of the gate driver IC´s power dissipation is a key point to avoid too high operating conditions. This section describes the calculation flow for the power dissipation of the gate driver ICs in general.

The main contributors for power dissipation are:

- The input side operating supply current
- The input side input bias currents
- The output side quiescent current
- The output side gate charge losses

The individual items can be calculated by means of the following recipe:

1. Measure the operating current $I_{q,in}$ for maximum switching frequency of the application. The power transistors should not be connected.

$$P_{\mathrm{d,VCC1}} = I_{\mathrm{q,in}} \cdot V_{\mathrm{VCC1,max}} \tag{1}$$

The input bias currents of logic input terminals contribute with

$$P_{\mathrm{d,bias}} = n \cdot I_{\mathrm{IN}} \cdot V_{\mathrm{VCC1,max}} \tag{2}$$

The parameter *n* is the number of input terminals of the gate driver IC. This portion of power dissipation is usually very small compared to the portion contributed by the supply voltage.

2. The output side section generates a continuous power dissipation in respect of the quiescent current $I_{q,out}$. This is given by

$$P_{\mathrm{d,VCC2}} = I_{\mathrm{q,out}} \cdot (V_{\mathrm{VCC2,max}} - V_{\mathrm{VEE2,max}}) \tag{3}$$

The output side quiescent current value should be measured as well at the maximum switching frequency without the power transistors being connected.

3. Calculate the losses of the output section by means of the total gate charge of the power transistor Q_{Gtot} , the supply voltage $V_{VCC2} – V_{VEE2}$, the switching frequency f_P ,and the external gate resistor. Different cases for turn-on and turn-off have to be considered, because many designs use different resistors for turn-on and turn-off. This leads to a specific distribution of losses in respect to the external gate resistor $R_{Gxx,ext}$ and the internal resistance of the output section.

$$P_{\mathrm{d,on}} = \frac{1}{2} Q_{\mathrm{G,tot}} \cdot (V_{\mathrm{VCC2}} - V_{\mathrm{VEE2}}) \cdot f_{\mathrm{P}} \cdot \frac{R_{\mathrm{Gon,IC}}}{R_{\mathrm{Gon,ext}} + R_{\mathrm{Gon,IC}}} \quad \text{, for turn-on} \tag{4}$$

$$P_{\mathrm{d,off}} = \frac{1}{2} Q_{\mathrm{G,tot}} \cdot (V_{\mathrm{VCC2}} - V_{\mathrm{VEE2}}) \cdot f_{\mathrm{P,max}} \cdot \frac{R_{\mathrm{Goff,IC}}}{R_{\mathrm{Goff,ext}} + R_{\mathrm{Goff,IC}}} \quad \text{, for turn-off} \tag{5}$$

Both portions $P_{d,on}$ and $P_{d,off}$ together add up to output section losses.

4. All remaining contributions can be estimated as approximately 20% of the sum of the above mentioned values. The final power dissipation during operation at highest switching frequency is then the sum of both contributions

$$P_d = 1.2 \left(P_{\mathrm{d,VCC1}} + P_{\mathrm{d,bias}} + P_{\mathrm{d,VCC2}} + P_{\mathrm{d,on}} + P_{\mathrm{d,off}} + P_{\mathrm{d,add}}\right) \tag{6}$$

5. Note that some gate drivers may have additional portions of power dissipation or a different partitioning of losses, such as the DESAT function or the active Miller clamping. This portion is represented by the term $P_{d,add}$ in equation (6). It is important to analyze the individual effect of each of these functions with respect to the power dissipation.

The datasheet shows specific layouts, for which the given thermal resistance junction to ambient ($R_{th(j-a)}$) is valid. It is important to know, that different layouts may lead to different thermal resistances. Therefore, it is always a good engineering practice to examine the package temperature by experiment additionally.

4 Considerations for single transistor topologies and applications with low dV_{DS}/dt stress during off-state

This section explains special conditions for SiC MOSFET gate drives in single-transistor topologies. Popular topologies using a single SiC MOSFET for example are boost, buck or flyback converters. It is easy to see that the low-side referenced switch, e.g. of a boost topology, does not have a mandatory requirement for an isolated gate driver. However, being non-isolated, drivers can suffer often from heavy ground bouncing. This can lead to latch-up of the driver IC or to additional switching losses, due to stray inductances, which do not allow a proper switching process. Isolated gate drivers on the other hand do not suffer from ground bouncing due to the large offset voltage range. This provides extra gate drive performance particularly in single transistor topologies.

4.1 Positive (unipolar) gate voltage

An actively injected dV_{DS}/dt event by means of a turn-on of the opposite switch while the other MOSFET is in off-state cannot happen in single-transistor topologies. A dV_{DS}/dt triggered parasitic turn-on is only a minor threat and depends strongly on the gate-source threshold voltage $v_{DS,th}$ of the SiC MOSFET. Therefore, a positive gate voltage is often sufficient to control the SiC MOSFET. CoolSiC™ MOSFETs have special benefits because the gate-source threshold voltage $v_{DS,th}$ is high as discussed in section 2.3 and therefore these devices are very robust against noise triggered turn-on. This simplifies gate drive circuits a lot because no isolated supply is required e.g. for boost or flyback converters.

A unipolar positive gate voltage can be applied in some drive applications with a limited dV_{DS}/dt switching speed. The dV_{DS}/dt is often limited to 5 V/ns in such applications due to motor lifetime considerations. Infineon´s CoolSiC™ transistors offer relatively a high gate-source threshold voltage $v_{GS,th}$ as shown in Figure 3 so that dV_{DS}/dt triggered parasitic turn-on is very unlikely to happen even in half-bridge configurations. Additionally, the applications using a positive only gate voltage can be supported by the active miller clamping function which is previously explained in section 2.7 and in the section below.

4.2 Active miller clamping

Even though some SiC MOSFET such as the CoolSiC™ family have relatively high gate-source threshold voltage $v_{DS,th}$, a hardware design engineer may like to have an additional safe path to keep the SiC MOSFET in off-state. Specific EiceDRIVER™ ICs support this need by means of the CLAMP terminal. An additional sink transistor is activated inside the IC as soon in parallel to the terminal OUT as soon as the gate voltage is below typically 2 V and clamps the gate to V_{VEE2} or V_{GND2}.

Isolated EiceDRIVER™ ICs with active miller clamp and a positive only gate voltage supply are:

- 1EDI10I12MF, 1EDI10I12MF, 1EDI10I12MF,

Isolated EiceDRIVER™ ICs offer the active miller clamp in combination with a DESAT function:

- 1ED020I12-F2, 1ED020I12-B2,
- 1ED020I12-FT, 1ED020I12-BT

Text references

[1] Infineon Technologies: EVAL-1ED020I12-BT, Evaluation board description, 2014.

[2] Infineon Technologies: 2ED100E12-F2_EVAL, Evaluation board description, 2008.

Revision History

Major changes since the last revision

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