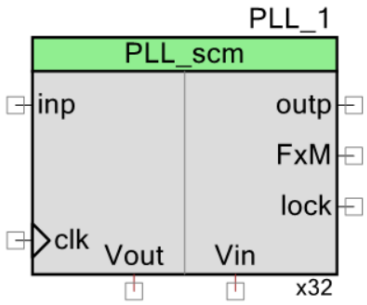
PLL_scm: Phase Locked Loop using SC_Modulator
0.0

Features



- Implements analog PLL using Type-II Phase Frequency Detector.
- Uses 1st-order delta-sigma modulator as VCO.
- Primary output is locked in both frequency and phase.
- Secondary output for multiplied frequency.
- Output for optional lock detection.
- Does not consume CPU.

General description

The PLL_scm(*) implements all-analog Phase Locked Loop using Type-II phase-frequency detector (PFD), external passive low-pass filter (LPF) and voltage-controlled oscillator (VCO) based on switched-capacitor delta-sigma modulator(†). It can lock to the digital signal, producing output signal of the same frequency, and another for multiplied frequency, both are phase-aligned with the input. The component was designed to operate at low frequencies (10 Hz – 10 kHz), with primary goal is tracking the power line AC frequency (50-60 Hz). The component utilizes traditional architecture [1] and consumes little PSoC resources. Up to four instances of component can run simultaneously on PSoC.

When to use Decoder component

Component was developed as part of RMS detection project. At large its functionality is similar to a CD4046 PLL circuit. It can be useful for frequency multiplication, quadrature generation, motor control, etc. Component was tested using CY8KIT-059 PSoC5 prototyping kit. Demo project is provided.

* Hereafter referred as PLL
† SC_Modulator is a part of the Chris Keeser PSoC component library.

Input-output connections

inp – digital signal input

External terminal for connecting input signal, which PLL is locked to. Pin must be connected to a valid digital source. The input signal doesn't need to be 50% duty cycle. The pin is always visible.

clk – clock input

Valid clock signal must be connected to this input. Acceptable clock range for this input is from 5 kHz to 4 MHz. Selecting right clock frequency is important for proper operation of the component, as PLL lock range is dependent on it. See **Implementation** section for details. The pin is always visible.

Vout – analog output signal

Provides analog output signal from PFD. In order PLL to operate, the pin must be connected to the LPF. It is best to connect it to a hardware terminal which has a direct path to the IDAC output. The pin is always visible.

Vin – analog input signal

Analog input of the VCO. In order PLL to operate, the pin must be connected to the output of LPF. The pin is always visible.

outp – digital output signal

PLL frequency is being output on this pin. The output on this pin has 50% duty cycle. When PLL is locked, the output frequency coincides with input signal. When out of lock, output frequency slips to the upper boundary of the lock range. See **Implementation** section for details. The pin is always visible. The pin does not have to be connected.

FxM – multiplied frequency output signal

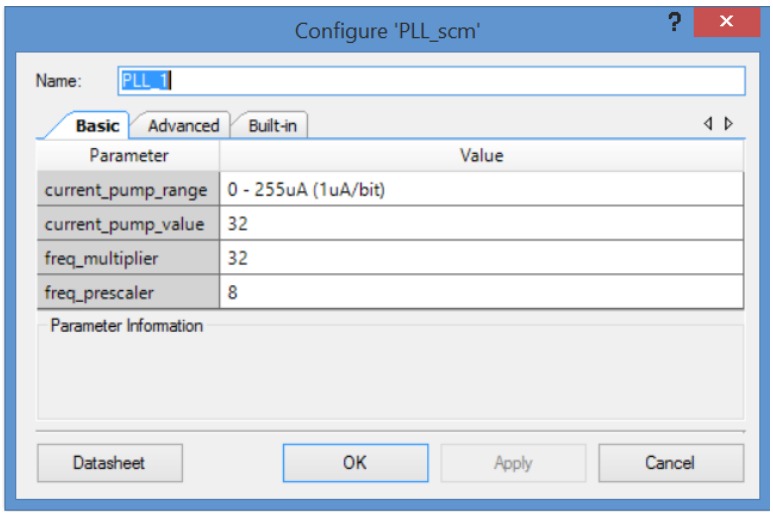
PLL multiplied frequency is being output on this pin: $F_M = M \times F_{PLL}$ (M=2÷256). Output of this pin is not 50% duty cycle. The pin is always visible. The pin does not have to be connected.

lock – lock detect output

Output of this digital pin can be routed to a lock detect circuit. When PLL is not locked, this pin produces positive pulses of long duration; the closer it gets to the locked state, the shorter and rare the pulses become. See **Implementation** section for details. The pin is always visible. The pin does not have to be connected.

Parameters and Settings

Basic dialog provides following parameters[(*)]:



current_pump_range (0 – 31.875 uA / 0 – 255 uA / 0 – 2040 uA)

This parameter allows setting the range for PFD current pump. The range may be changed during run time. If the highest current range, 0 – 2040 uA, is selected, then the output should be routed to one of the PSoC5 special pins that provide a low resistive path.

current_pump_value (uint8)

Current setting value for the **current_pump_range**. Actual current is controlled by setting both current pump value and range. The value may be changed during run time.

[*] PLL_scm component is intentionally compiled using Creator 4.0 for compatibility with older versions.

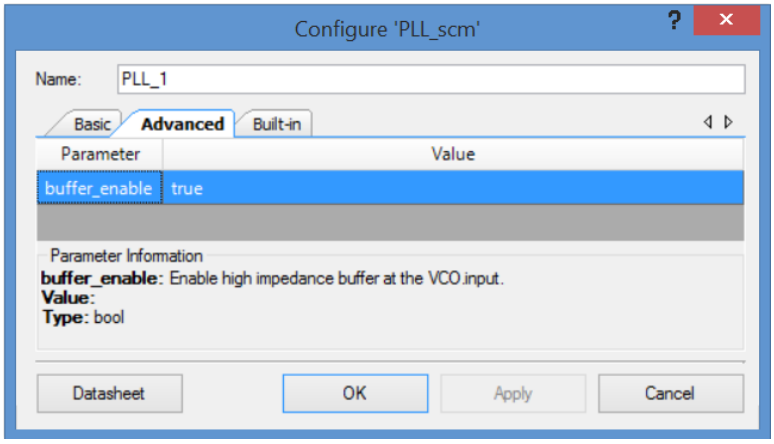
freq_multiplier (uint16)

Frequency multiplier value (M). Valid range is from 2 to 256. This value can't be changed during run time. See **Implementation** section for details.

freq_prescaler (uint8)

Value of supplementary frequency divider in PLL feedback divider path, which scales down high frequency from the Modulator to PLL outputs. The higher the divider, the less is the PLL phase jitter. Valid range is from 2 to 128. This value can be changed during run time. See **Implementation** section for details.

Advanced dialog provides following parameters:



buffer_enable (bool)

Enables high impedance buffer at the input of the VCO. Default value is True. If enabled, this feature consumes one Opamp. See **Implementation** section for details.

Application Programming Interface

Function	Description
`PLL_Start()`	Initialize and start component
`PLL_Stop()`	Stop component

void PLL_Start()

Description: Initializes and starts component.

Parameters: none

Return Value: none

void PLL_Stop()

Description: Stops and disables component.

Parameters: none

Return Value: none

Functional Description

The phase-locked loop is important component of many electronic circuits. Major properties of PLL are: (i) signal tracking (clock synchronization) – ability to phase-align an internal clock to the input clock, (ii) signal conditioning - ability to clean-up input clock from jitter, (iii) frequency multiplication - ability to multiply the input clock, making higher frequencies.

The PLL_scm utilizes traditional all-analog PLL design, which includes a phase comparator, low-pass filter, and voltage controlled oscillator (Fig. 1). Such design occupies low PSoC footprint and has wide support [1-4].

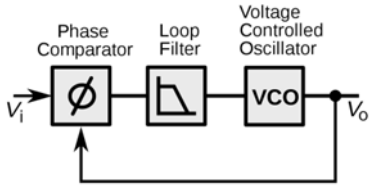


Figure 1. PLL structure diagram.

The phase comparator is implemented as Phase Frequency Detector (PFD) [2, 3], in basic form consisting of two D-type flip flops; one DFF output enables a positive current source, and the other DFF output enables a negative current source (Fig. 2). Unlike XOR comparator, the PFD produces output that has both same frequency and phase as the input signal.

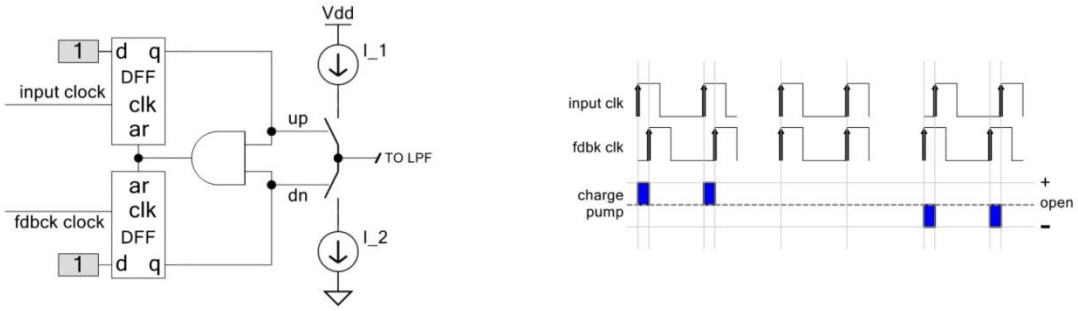


Figure 2. Phase frequency detector schematic and output response.

The Voltage Controlled Oscillator was implemented using 1st-order delta-sigma modulator [5], occupying a single SC/CT block. Such approach saves other PSoC resources (IDAC, comparator), which, otherwise, would be consumed to make a VCO, and needs no external parts (e.g. capacitor), but is limited to low frequencies operation due to the modulator's intrinsic phase noise. For that reason, the emphasis of current implementation is given to ability of PLL to lock to power mains AC signal in 50-60 Hz frequency range. At low frequencies such VCO displayed same or superior performance to other VCO types tested.

Implementation

Phase-Frequency Detector

The phase comparator implemented as Phase-Frequency Detector (PFD) [2, 3], consisting of two D-type flip flops (Fig. 5). In classic implementation, one DFF output enables a positive current source, and the other DFF output enables a negative current source. To save resources, the design uses a single IDAC8 with polarity control, thus combining both positive and negative current pumps functions into a single(*) IDAC.

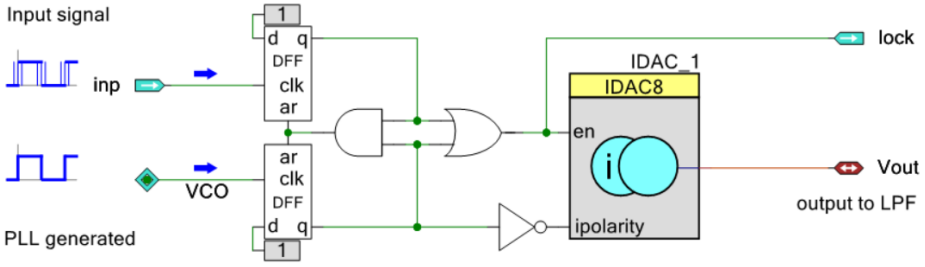


Figure 3. Phase-Frequency Detector implementation using PSoC5 blocks.

The PFD output polarity is controlled by logical NOT element, which is added to match negative slope of the VCO frequency output. In such design, PFD analog output is positive when VCO frequency is higher than input signal frequency, and negative when input frequency is lower than VCO's.

The IDAC current setting controls PLL bandwidth, which affects the loop settling time and phase noise. Optimal values for 60 Hz operation are typically in range 32-255 uA. Low current setting decrease bandwidth, leading to higher phase noise and settling time. High current setting increases bandwidth, which reduces phase noise and settling time.

Low-Pass Filter

The low-pass filter (LPF) is a critical component of analog PLL circuit [2, 3]. It converts stream of current pulses from PFD into control voltage for VCO operation. The component was tested with 2nd- and 3rd-order passive filters using few off-chip resistors and capacitors. The PPLatinum Simulator Tool [6] was used to facilitate LPF tuning (see **Appendix 1**). Values optimized for 60 Hz operation are shown on Fig. 4.

* Ideally, IDAC's source and sink currents should be equal over entire voltage control range (which is not the case for IDAC8), together with LPF leakage it may contribute to asymmetry and static phase error.

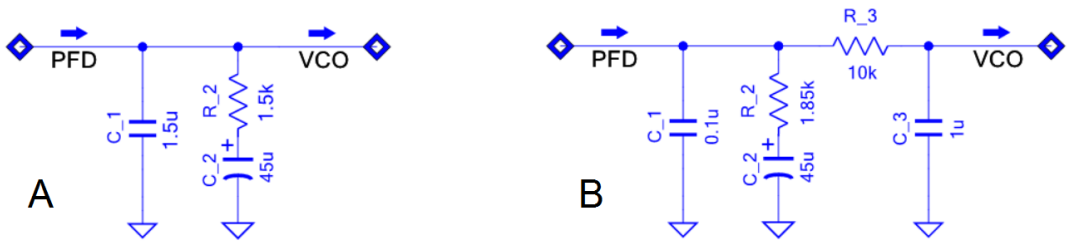


Figure 4. (A)- 2nd-order, and (B)- 3rd-order LPF examples tuned for 60 Hz operation.

The important function of the LPF is to provide a phase margin to dampen oscillations in the loop by providing some "friction". It is achieved by the R_2, C_2 pair, where resistor R_2 must be fine-tuned for critical dumping.

The choice of filter type didn't significantly affect the performance, though some differences remain. See **Performance** section for details.

Voltage-Controlled Oscillator

The VCO implemented using SC_Modulator component(*) [5], which is a 1st-order delta-sigma modulator, implemented using one SC/CT block, and a couple of frequency dividers (Fig. 5).

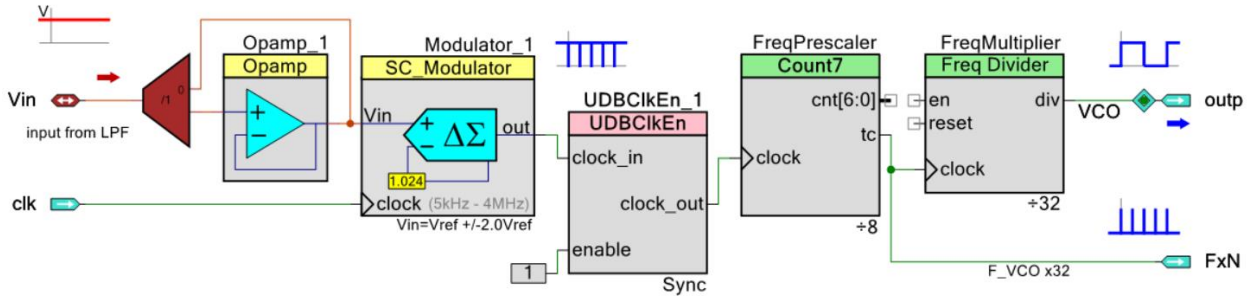


Figure 5. VCO implementation using PSoC blocks.

The Modulator translates analog voltage into a digital stream, which frequency controlled by the input voltage (Fig. 6). The plot has two slopes, centered around V_{ref} (1.024V); the PLL operates on the negative slope, which provides wider dynamic range:

$$F_{MOD} = F_{CLK} \times (0.75 - 0.25V/V_{ref}),\ V > V_{ref} \qquad (1)$$

The highest frequency that Modulator can produce is ½ of the input clock.

* The SC_Modulator component used here has cosmetic improvements for better visual appearance. Its performance is the same as for the original component.

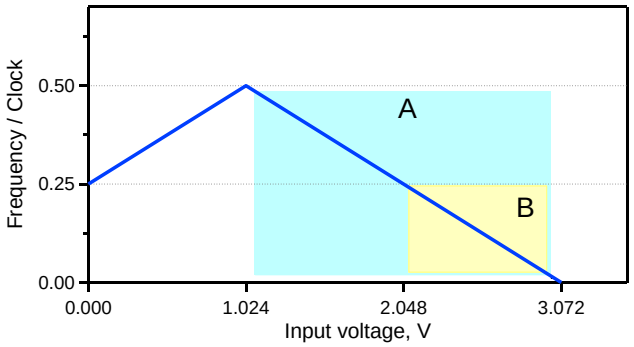


Figure 6. SC_Modulator output frequency vs. input voltage. Marked areas indicate: (A) PLL holding range, (B) PLL locking range.

Employing delta-sigma modulator has advantage of not using external components for VCO operation; the drawback is that the output frequency stream is not steady on a micro-timescale. For that reason modulator clock is set to high value and then downsampled using a couple of feedback dividers, FreqPrescaler (P) and FreqMultiplier (M) to bring output VCO frequency to a desired range of 60 Hz, effectively averaging out phase noise. Resulting VCO frequency is:

$$F_{VCO} = F_{CLK}\,(0.75 - 0.25V/V_{ref})/(P \times M) \qquad (2)$$

According to specs sheet, maximum allowed clock frequency for Modulator is 4 MHz, taking it down to 60 Hz would require a 15-bit divider, consuming PSoC resources. It was found that a moderate clock as low as 160 kHz and divider of 256 (8×32) provides reasonable results.

Having two frequency dividers (prescaler and multiplier) allows for independent control of the modulator clock frequency and frequency multiplier. The Count7 component was used as FreqPrescaler. Though it is more resource-efficient than Freq_Divider component, its scale is limited to maximum of 128, it needs UDB Clock Enable for synchronization, and it does not provide 50% duty cycle. The Freq_Divider component has none of such limitations and guarantees 50% duty cycle, but consumes PLD resources. Depending on application it is possible interchanging Count7 and Freq_Divider components in VCO schematic without performance penalty, as PFD-type phase comparator doesn't require 50% duty cycle for proper operation.

The PLL holding and locking ranges are marked out on Fig. 6. The upper bound of the lock range was found to be about half that of the holding range: $F_{max}^{lock} \approx 0.5\,F_{max}^{hold}$. The reason for this effect is not clear, as for PFD-type comparator the regions are typically overlap.

When PLL is not locked, the VCO output frequency slips to the upper bound of the lock range:

$$F_{max}^{lock} \approx 0.25\,F_{CLK}/(P \times M) \qquad (3)$$

The VCO input is buffered by Opamp operating in the follower mode. Without buffer, the Modulator may load LPF, resulting in the phase offset in the output signal (see **Performance** section for details). Such offset is typically small (<1%), and depending on application, the input buffer may be optionally disabled to save one Opamp.

Lock Detect Circuit

The PLL component provides a **lock** pin, which can be used for optional lock detection. When PLL is not locked, this pin produces positive pulses of long duration; the closer it gets to the locked state, the shorter and rare the pulses become. Many lock detection schemes exist. Basic circuit can be realized as external analog circuit using few passive components (Fig. 6).

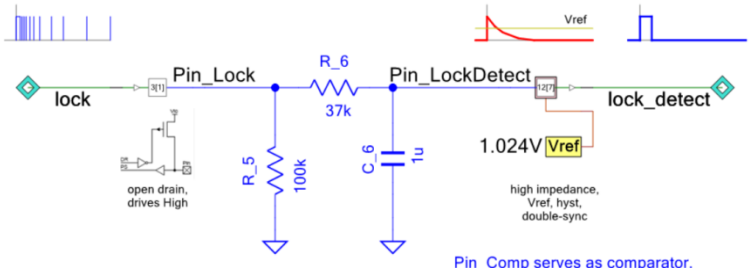


Figure 7. Lock detect analog implementation using SIO pin as a comparator.

The output Pin_Lock is set to open drain, drives high mode. In the high state it charges capacitor C_6 through resistor R_6; resistors R_5 and R_6 provide discharge path when the Pin_Lock is off. Together, R_5, R_6 and C_6 create analog circuit, which output transitions from High to Low when lock is achieved. The SIO Pin_LockDetect is set to comparator mode to detect the lock state. Its output can be hardwired to LED or directly polled by CPU to check the lock status. Using SIO pin instead of a Comparator is sufficient for lock detection purposes and saves one Comparator.

The lock detection circuit is optional and can be omitted to save PSoC pins. Often, information about lock state can be obtained indirectly through other parameters in the application.

Performance

Component was tested using PSoC5LP (CY8KIT-059) and prototyping breadboard. Both 2nd- and 3rd-order LPF were tested, their components value were adjusted to tune the loop while varying current, clock and dividers. Performance of PLL using 2nd- and 3rd-order LPF was similar.

Typical results observed for 3rd-order LPF tuned for 60 Hz are shown on Figs. 8 and 9, which show performance at high (255 uA) and low (32 uA) IDAC current setting accordingly. In the locked state PLL output tracks the input signal (Fig. 8A). At current 255 uA the loop is critically dumped, resulting in small phase jitter (~7 us, Fig. 8B) and fast settling (~0.17 s, Fig. 8C,D). Estimated loop bandwidth here was about 6 Hz. The locking and holding ranges at 255 uA were 30-145 Hz and 30-295 Hz (see Table 2(1)).

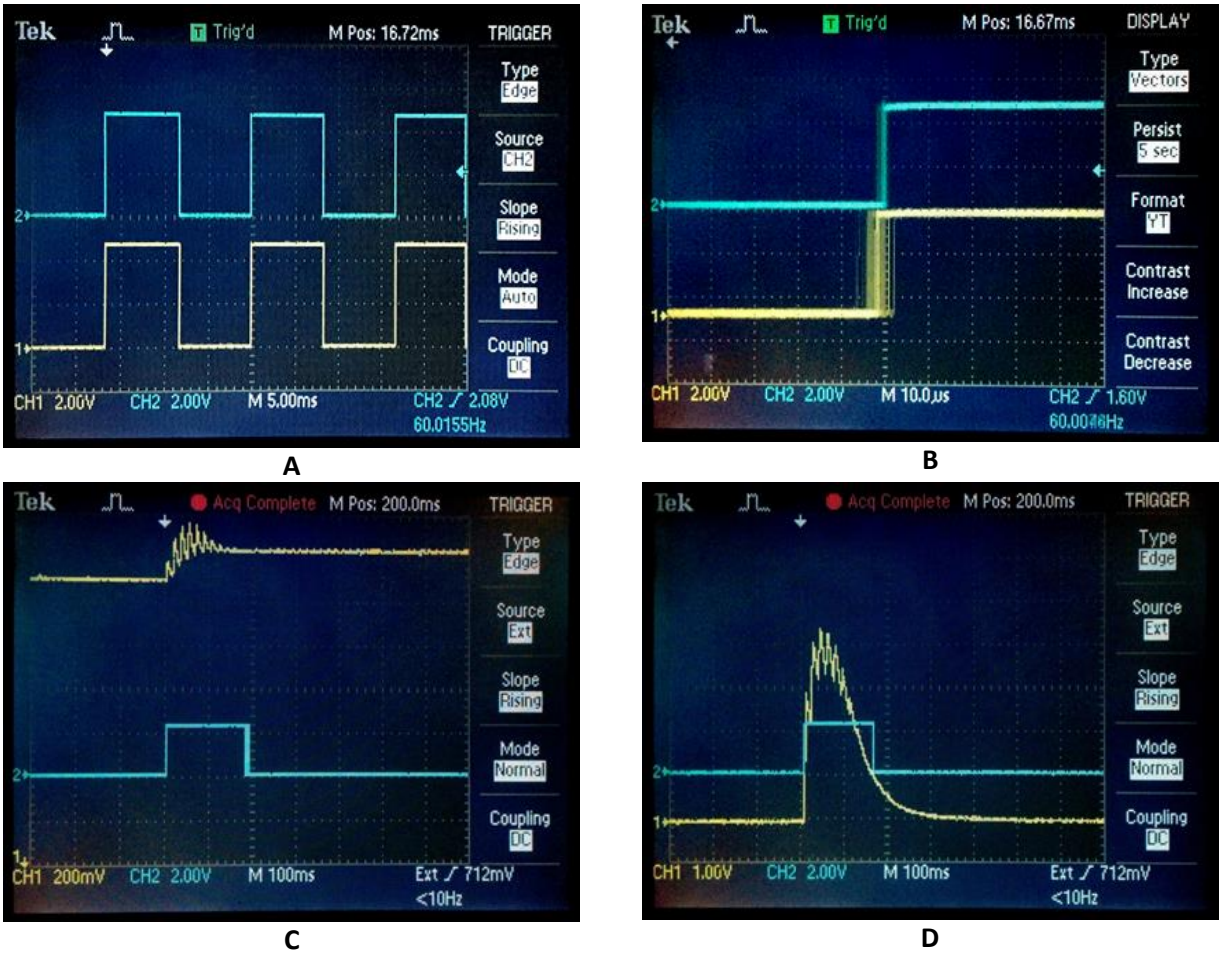


Figure 8. Critically dumped PLL at 60 Hz and current 255 uA: (A) blue - input signal, yellow - PLL output; (B) – PLL phase jitter; (C) filter output and (D) lock detect transients upon frequency jump from 80 Hz to 60 Hz (yellow line); blue line - Pin_LockDetect comparator output (low = locked). Data taken using 3rd-order LPF; other settings in Table 2(1).

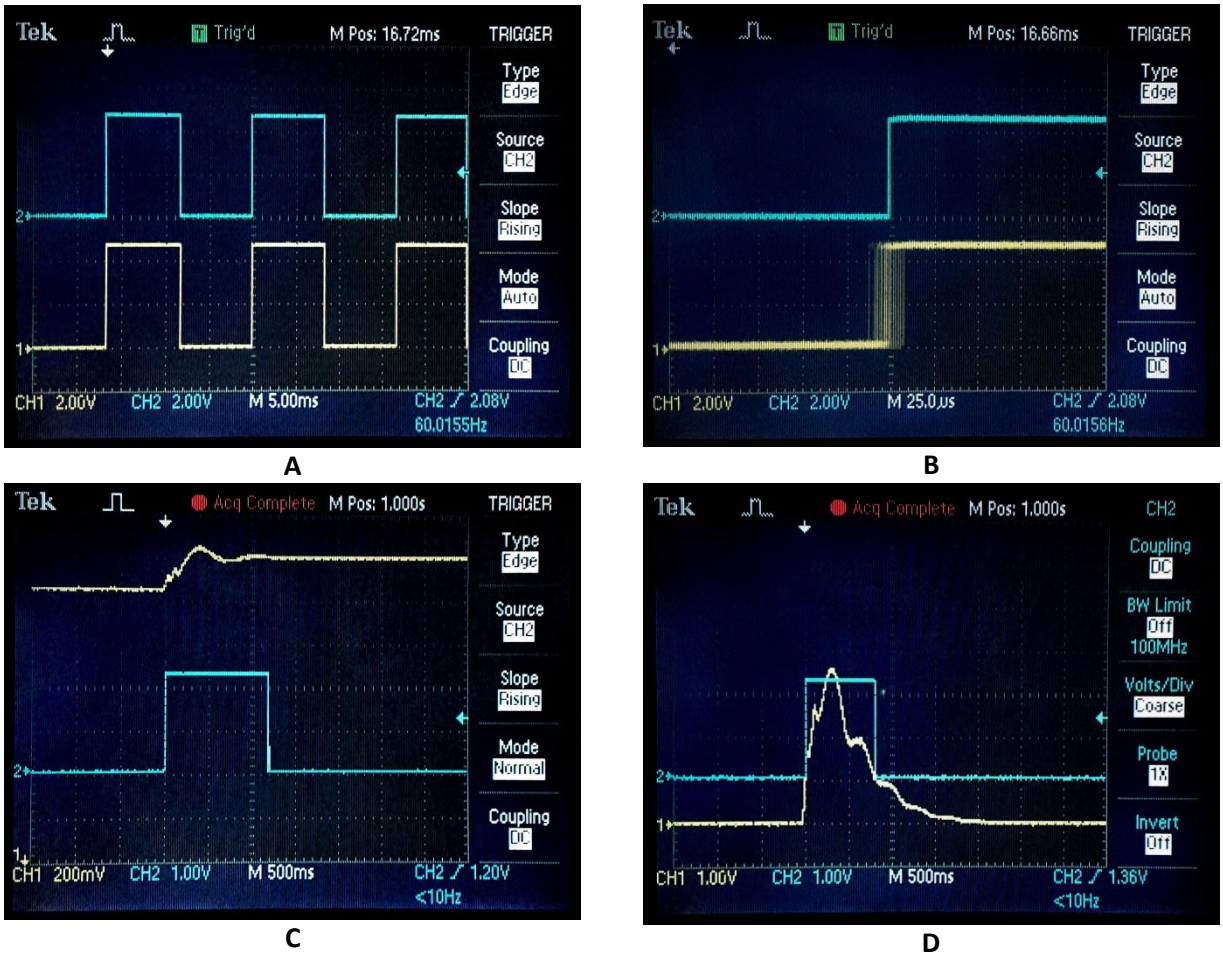


Figure 9. Under-dumped PLL at 60 Hz and current 32 uA: (A) blue - input signal, yellow - PLL output; (B) – PLL phase jitter; (C) filter output and (C) lock detect transients upon frequency jump from 80 Hz to 60 Hz (yellow line); blue line - Pin_LockDetect comparator output (low = locked). Data taken using 3rd-order LPF, other settings in Table 2(4).

Lowering IDAC current down to 32 uA reduced loop bandwidth to about 1 Hz, resulting in higher jitter (~25 us, Fig. 9B) and slower settling time (~1 s, Fig. 9C,D). It didn't affect much the locking and holding ranges, which became 10-135 Hz and 10-270 Hz accordingly (Table 2(4)), differences being attributed to the amplitude of the voltage spikes feeding through the LPF.

The output jitter discussed above is "intrinsic" to PLL, as no artificial noise has been introduced to the input signal. It originates from VCO noise being suppressed by the loop feedback gain, which is proportional to the IDAC current. Thus higher current lowers "intrinsic" jitter. It also increases loop bandwidth, making PLL sensitive to any input noise. Lowering IDAC current relaxes feedback and reduces loop bandwidth in expense of higher PLL intrinsic noise and longer settling time, but it will be able to average and smooth noisy input signal. Optimal current setting depends on application requirements and requires balancing approach.

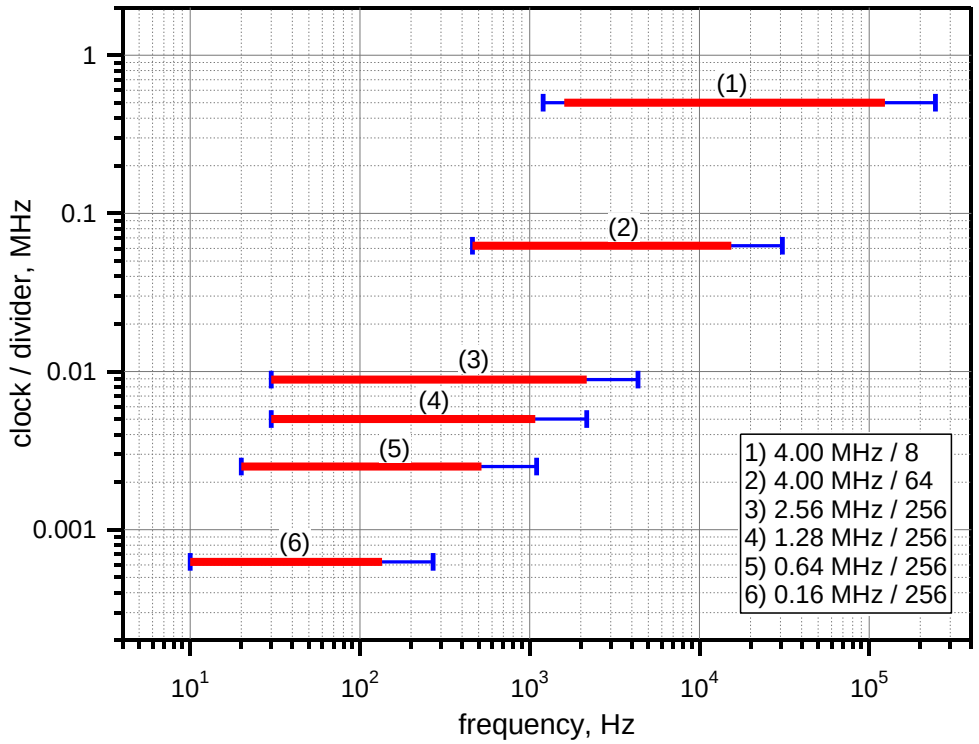


Figure 10. PLL frequency range vs. input clock and feedback divider: red - lock range; blue - hold range. Data collected using 3rd-order LPF are taken from Tables 2-4.

Factors which define PLL locking and holding ranges are the input clock and feedback divider ($P \times M$). Using these parameters, PLL frequency can be adjusted in wide range approx. 10 Hz to 120 kHz (Fig. 10). Two characteristic features persist among various settings: (i) the lower bounds for locking and holding ranges are about the same; (ii) the upper bound for the holding range is twice[(*)] that of the locking range.

[*] This phenomenon is not clear as for PFD-type comparator the locking and holding ranges typically overlap.

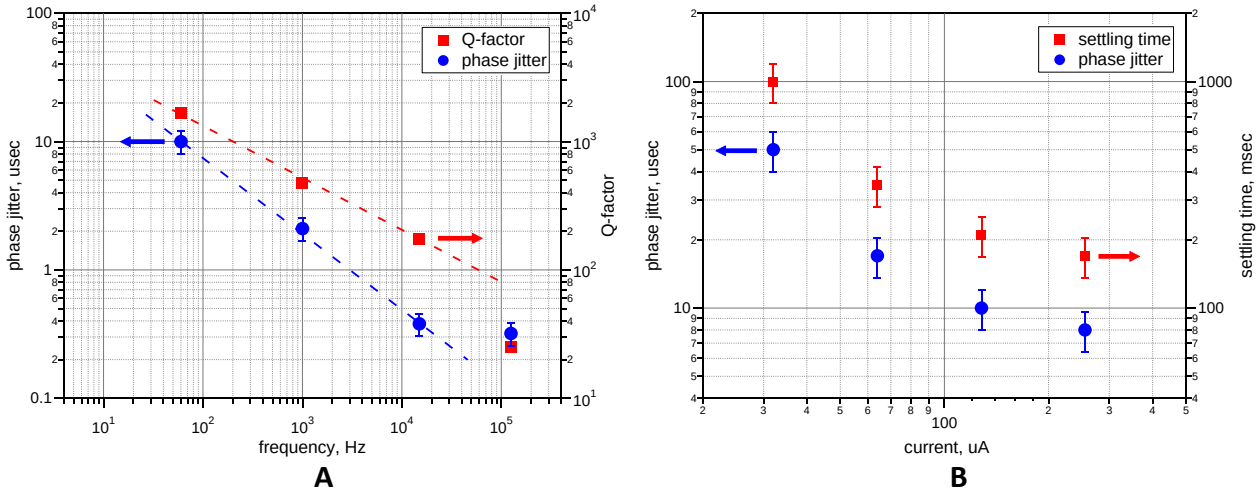


Figure 11. (A) Phase jitter and Q-factor vs. frequency taken at fixed current 255 uA. (B) PLL settling time and phase jitter vs. IDAC current taken at fixed frequency of 60 Hz. Data collected using 3rd-order LPF.

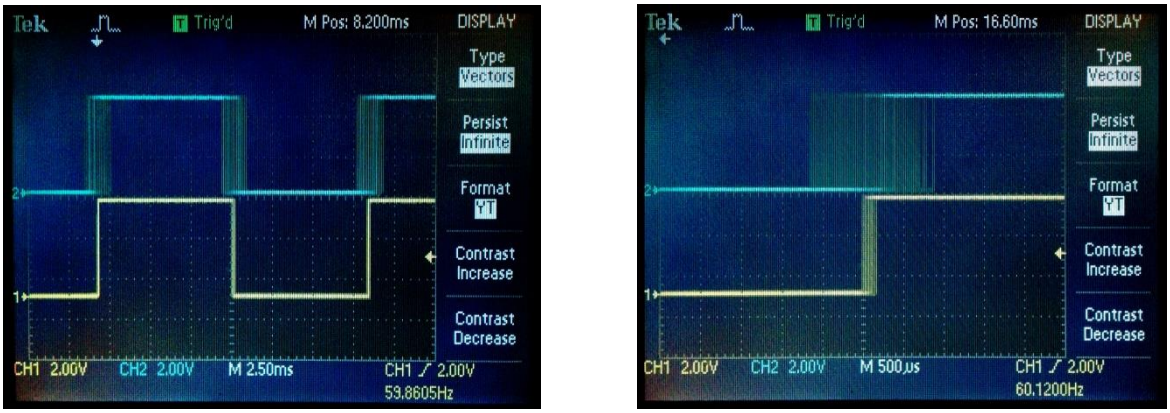
The phase jitter reduces with frequency ($\sim F^{-0.5}$), but the quality factor (Q = period/jitter) diminishes, limiting practical range of operation to about 10 kHz (Q~200, Fig. 11A).The phase jitter and settling time are current-dependent, saturating at higher current; typical data taken at 60 Hz are shown on Fig. 11B. Several sources contributing to PLL noise were identified: (i) IMO instability, (ii) DDS signal generator jitter, (iii) the Modulator quantization, and (iv) analog noise from breadboard setup.

PLL ability to clean 60 Hz input signal from noise is shown on Fig. 12. Input test signal had 10% of random (white) phase noise. Here PLL was able to substantially (about 10x) reduce the input jitter when bandwidth was narrow (current 32 uA, estimated loop bandwidth is ~1 Hz). PLL did not filter the noise when loop bandwidth was high (current 255 uA, estimated bandwidth ~6 Hz). The PFD-type detector generally considered as being not noise-immune; for heavy noise rejection a XOR-type detector is preferred.

Frequency multiplication example is shown on Fig. 13. The multiplied frequency output is phase-aligned with the input signal. Though it is not 50% duty cycle due to the prescaler implementation using Count7, this is typically not a problem when it used for generation of quadratures or ADC triggering(*). The positive pulse length equals the Modulator period.

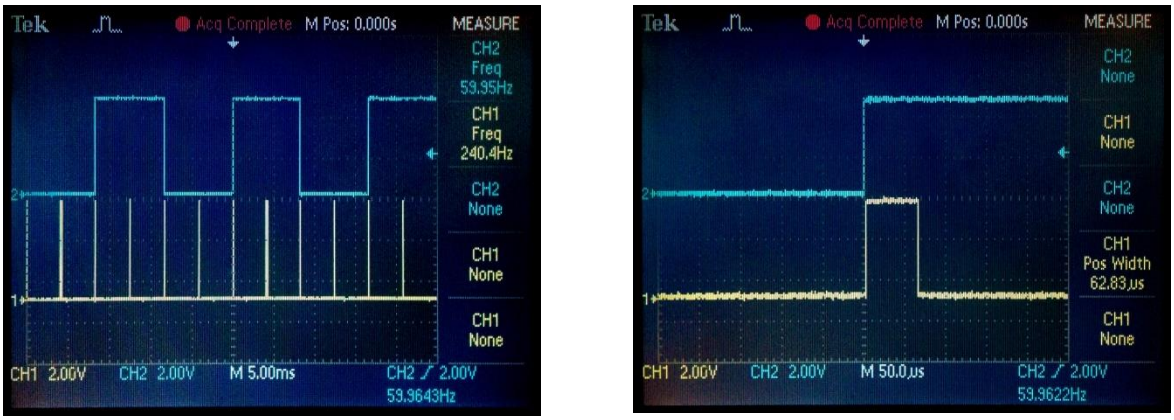
Effect of the VCO input buffer is presented on Fig. 14. When enabled, the output of the PLL is phase aligned with the input signal (Fig. 14A); disabling the buffer results in phase offset (Fig. 14B), attributed to Modulator's low input impedance (estimated value ~100k) and associated LPF leakage.

* For true 50% duty cycle output the Count7 can be substituted with Freq_Divider component.



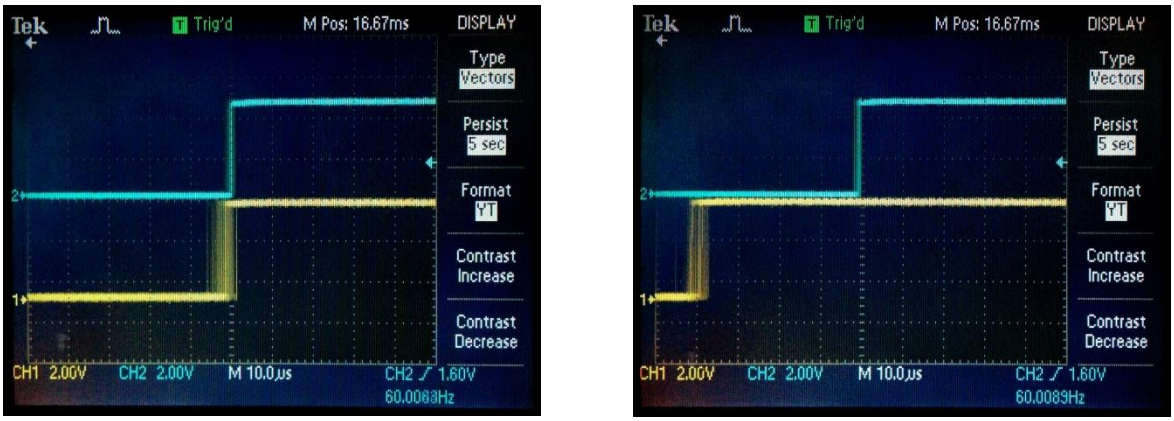
A **B**

Figure 12. PLL input clock clean-up from random jitter. Blue - input signal; yellow - PLL out; (B)-expanded view after one period. Input frequency 60 Hz, jitter 10%, IDAC current 32 uA, 2nd-order LPF with settings in Table 5(1).



A **B**

Figure 13. PLL frequency multiplication example. Blue - input signal; yellow - FxM out; (B)-expanded view. Input Signal frequency 60 Hz, clock=160 kHz, P=64, M=4, IDAC current 255 uA, 2nd-order LPF.



A **B**

Figure 14. PLL phase offset with: (A) – buffer enabled, (B) - buffer disabled. Blue - input signal, yellow - PLL out. Signal frequency 60 Hz, IDAC current 255uA, 2nd-order LPF. Other settings are in Table 5(2).

Summary

- Minimalistic PLL design needs only two capacitors and one resistor for operation.
- Lowest usable PLL frequency achieved was about 10 Hz; highest – about 120 kHz.
- Due to PFD the input signal does not have to be exactly 50% duty cycle.
- Performance of the PLL using 2nd-order and 3rd-order LPF is close (but not the same). The 2nd-order LPF has fewer parts, but the 3rd-order LPF provides better filtering of PFD output.
- Clear advantage of the 2nd-order LPF is that a single pin can be used for input-output without noticeable performance loss, but the pin selection needs extra care.
- The upper hold range value is defined by the input clock and divider value of the prescaler and multiplier: $F_{max}^{hold} \lesssim 0.5\, F_{CLK}/(P \times M)$.
- The upper lock range is about half that of the hold range: $F_{max}^{lock} \approx 0.5\, F_{max}^{hold}$.
- The lower lock and hold ranges are about the same: $F_{min}^{lock} \approx F_{min}^{hold}$.
- When lock is lost, the VCO frequency slips to upper lock limit: $F_{max}^{lock} \approx 0.25\, F_{CLK}/(P \times M)$.
- At high current the hold and lock ranges are ~10% narrower, particularly at lower bound, attributed to the voltage spikes, which are feeding through the LPF.
- High IDAC current results in fast settling and low jitter, but poor input noise filtering. Low IDAC current results in slow settling and high jitter, but better noise filtering.
- PFD is not immune to strong input noise, it may not lock for noise exceeding 10%.
- Lowest phase jitter observed at 60 Hz was approx. 7-8 us (quality factor ~2000). PLL phase jitter declines with frequency approx. as $F^{-0.5}$.
- Disabling the input buffer results in phase offset (~40 us at 60 Hz), which may be of no importance for some applications, but can save one Opamp.

Resources

Resources consumption for the default configuration is provided below, actual results may vary. The component does not consume CPU, Datapath, DMA or interrupts. Component does not have built-in DMA capabilities. Total up to 4 components can fit into PSoC5.

Table 1. Resources consumption for default configuration.

Resource	
PLD (m-cells/P-terms)	14 / 7
Control Register	1
VIDAC	1
SC/CT block	1
Analog clock	1
Opamp	1 (*)
IO Pins	Analog: 2 (†); GPIO : 1 (‡), SIO: 1 (‡)

(*)optional; (†)option to use a single pin with 2nd-order LPF; (‡)optional, for lock detect circuit only

Sample Firmware Source Code

Examples of using 2nd- and 3rd-order LPF are given in **Appendix 2**. Demo project is provided.

Component Changes

Version	Description of changes	Reason for changes/impact
0.0	Version 0.0 is the first beta release of the component	

References

1. Wikipedia. Phase-locked loop, https://en.wikipedia.org/wiki/Phase-locked_loop
2. Texas Instruments. Dean Banerjee, PLL Performance, Simulation, and Design Handbook.
3. Analog Devices. MT-086. Fundamentals of Phase Locked Loops (PLLs).
4. Cypress. Demystifying the PLL, http://www.cypress.com/file/60101
5. Chris Keeser. SC_Modulator, https://community.cypress.com/thread/21987
6. Texas Instruments. PLLatinum Simulator Tool, http://www.ti.com/tool/PLLATINUMSIM-SW

Appendix 1

PLLatinum Simulator Tool

Tuning a PLL circuit can be time consuming task requiring clear understanding of its functionality. To streamline the process, Texas Instruments provides PLL Simulator Tool, PLLatinum, which is available for free download [6]. The software simulates performance of the TI proprietary PLL chips, listed on the Device Selector tab. It can also simulate a generic PLL circuit if "Custom" field is selected, and has a choice for 2nd-, 3rd- and 4th-order LPF. Despite some ambiguity on the input parameters, calculated values correlate well with the ones found empirically. A screenshot with data fields populated for 3rd-order LPF simulation is shown on Fig. 15.

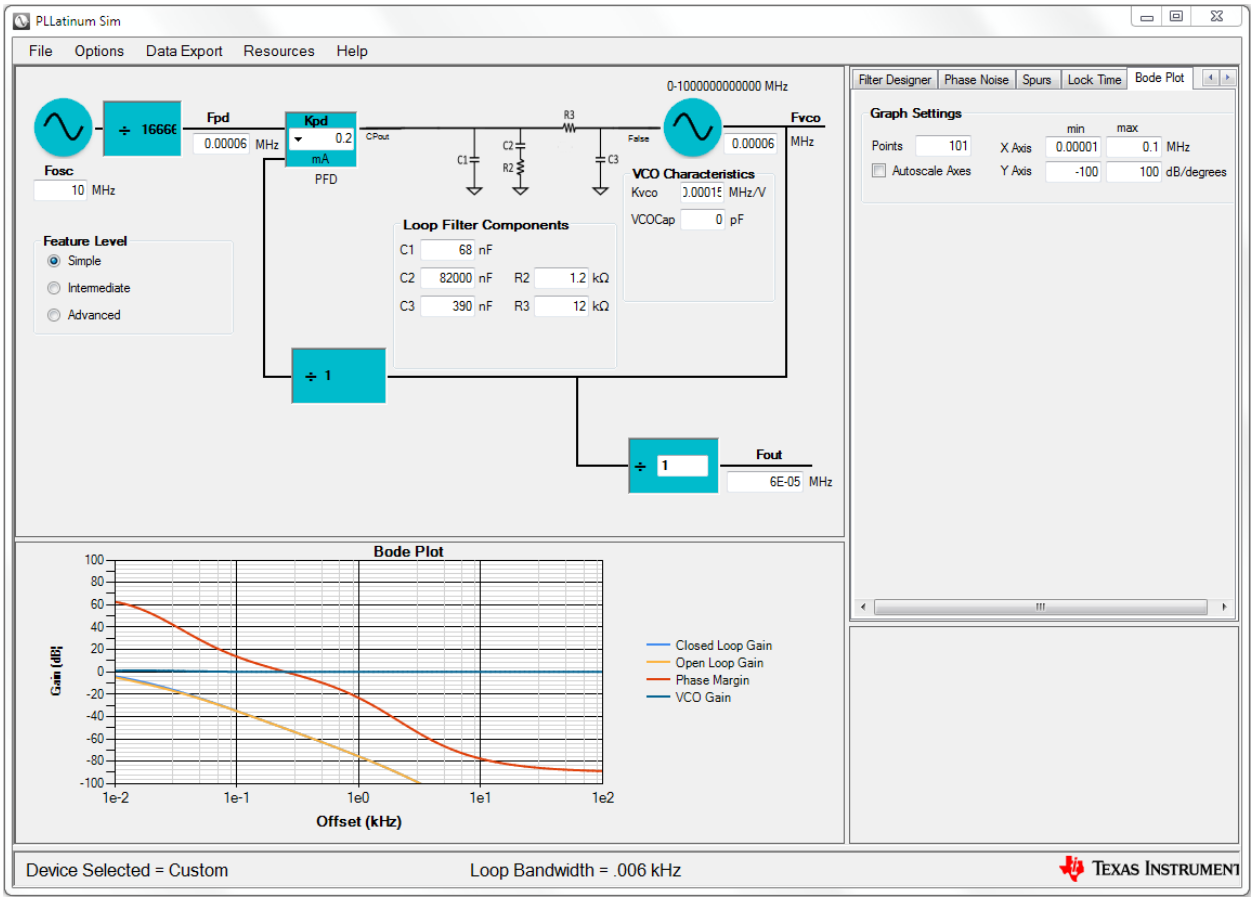


Figure 15. PLLatinum screenshot with typical parameters for 3rd-order LPF operating at 60 Hz.

Appendix 2

PLL examples using 2nd- and 3rd-order LPF

Examples of PLL using the 2nd-order LPF are shown on Fig. 16. The standard approach takes two analog pins for LPF input and output (Fig. 16A). Alternatively, a single pin connection can be used, subject to careful selection of the PSoC terminal (Fig. 16B). It is best if the pin selected has direct connection to the IDAC output (and thus lowest resistance to the LPF), and has no direct path to the Opamp input (thus creating some on-chip trace resistance from IDAC to Opamp). PLL performance obtained this was about the same as with two pins.

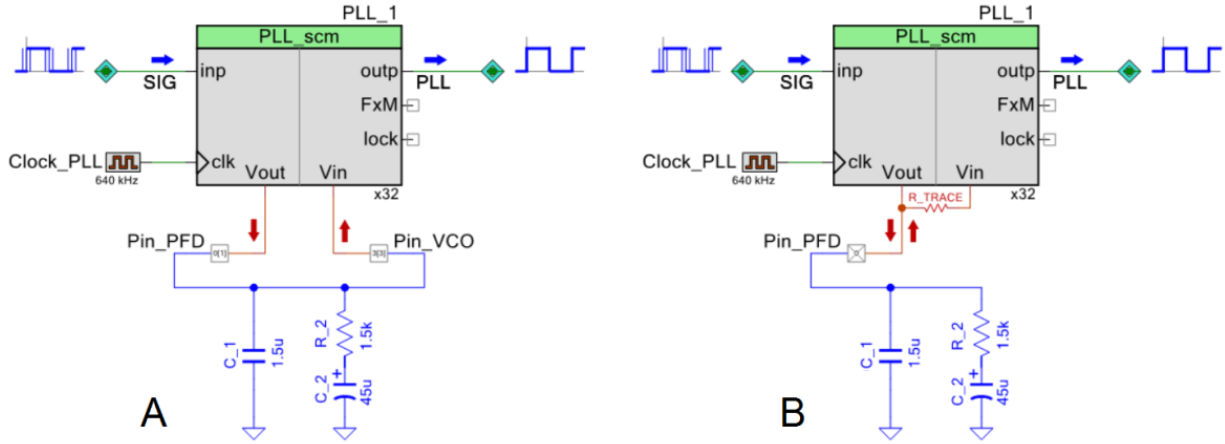


Figure 16. Example of 2nd-order LPF connection using: (A) two pin connection; (B)- single pin connection. Pin_PFD has direct path to the IDAC (Vout), and no direct path to the Opamp (Vin). On-chip trace resistance is typically few hundreds Ohm is depicted on schematic for illustration.

PLL example using 3rd-order LPF is shown Fig. 17. Unlike the 2nd-order LPF, it always needs two analog pins for LPF connection. Low leakage capacitor should be used for C_2 to avoid LPF leakage and phase lag, the tantalum and electrolytic here performed better than ceramic one.

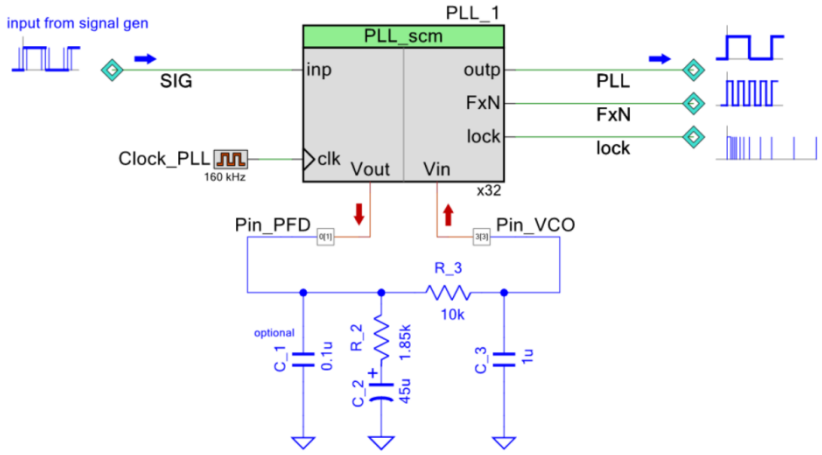


Figure 17. PLL circuit demo using 3rd-order LPF.

Appendix 3

Table 2. PLL performance for different current settings and same input clock. 3rd-order LPF.

PLL setting	1	2	3	4
IDAC current	255uA	128uA	64uA	32uA
modulator clock	640kHz	640kHz	640kHz	640kHz
divider (P × M)	1024 (32x32)	1024 (32x32)	1024(32x32)	1024 (32x32)
Passives				
C_1	0.1u	0.1u	0.1u	0.1u
R_2	1.1k	1.5k	1.6k	1.85k
C_2	45u	45u	45u	45u
R_3	10k	10k	10k	10k
C_3	1u	1u	1u	1u
R_5	47k	47k	100k	100k
R_6	3.7k	13k	37k	37k
C_6	1u	1u	1u	1u
performance				
Lock range	30-145 Hz	20-145 Hz	20-145 Hz	10-135 Hz
Hold range	30-295 Hz	20-295 Hz	20-295 Hz	10-270 Hz
Phase jitter (60 Hz)	~8 us	~10 us	~17 us	~25 us
Lock time (60Hz → 80Hz)	~0.17 s	~0.21 s	~0.26-0.35 s	~1 s

Table 3. PLL performance for low current settings and different input clock. 3rd-order LPF.

PLL setting	1	2	3	3
IDAC current	32uA	32uA	32uA	32uA
modulator clock	160kHz	640kHz	1280kHz	2560kHz
divider (prescaler × multiplier)	256 (8x32)	256 (8x32)	256 (8x32)	256 (8x32)
Passives				
C_1	0.1u	0.1u	0.1u	0.1u
R_2	1.85k	1.85k	1.85k	1.85k
C_2	45u	45u	45u	45u
R_3	10k	10k	10k	10k
C_3	1u	1u	1u	1u
R_5	100k	100k	100k	100k
R_6	37k	37k	37k	37k
C_6	1u	1u	1u	1u
Performance				
Lock range	10-135 Hz	20-520 Hz	30-1080 Hz	30-2170 Hz
Hold range	10-270 Hz	20-1100 Hz	30-2170 Hz	30-4350 Hz
Phase jitter (60 Hz)	~25 us	~50 us	~50 us	~100 us
Lock time (60Hz → 80Hz)	~1 s	~1 s	~1s	~1s

Table 4. PLL performance for various clock and divider settings using 3rd-order LPF.

PLL setting	1	2	3	4
IDAC current	255uA	255uA	255uA	
modulator clock	4000kHz	4000kHz	2560kHz	
divider (P × M)	8 (2x4)	64 (2x32)	128 (4x32)	
passives				
C_1	0.1u	0.1u	0.1u	
R_2	0.12k	0.12k	0.53k	
C_2	45u	45u	45u	
R_3	10k	10k	10k	
C_3	0.1u	0.1u	0.1u	
R_5	47k	47k	47k	
R_6	3.7k	3.7k	5.9k	
C_6	1u	1u	1u	
performance				
Lock range	1.6-124 kHz	0.46-15.4 kHz	0.30-4.70 kHz	
Hold range	1.2-246 kHz	0.46-30.8 kHz	0.30-9.45 kHz	
Phase jitter (Freq)	~0.32 us (124kHz)	~0.38 us (15kHz)	~2.5 us (1.0 kHz)	
Lock time ($F_1 \rightarrow F_2$)	~48 ms* (80→60 kHz)	~28 ms* (8→6 kHz)	~136 ms* (2.0→1.5 kHz)	

Table 5. PLL performance for various clock and divider settings using 2nd-order LPF (2 pins).

PLL setting	1	2	3	4
IDAC current	32uA	255uA	255uA	
modulator clock	640kHz	640kHz	4000kHz	
divider (P × M)	1024 (32x32)	1024 (32x32)	64 (2x32)	
passives				
C_1	1.5u	1.5u	1.5u	
R_2	3.5k	1.5k	1.5k	
C_2	45u	45u	45u	
R_3	-	-	-	
C_3	-	-	-	
R_5	47k	47k	47k	
R_6	3.7k	3.7k	3.7k	
C_6	1u	1u	1u	
performance				
Lock range	10-145 Hz	35-150 Hz	0.86-15.5 kHz	
Hold range	10-295 Hz	35-295 Hz	0.86-30.8 kHz	
Phase jitter (60 Hz)	~17 us	~7 us	~0.38 us (15kHz)	
Lock time (80→60 Hz)	~0.46 s	~0.17 s	~28 ms (8→6 kHz)	