Introduction to Low Power Modes in PSoC 6

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Infineon

Demo – Simple Low Power Mode

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Agenda

- Low Power MCU Systems
- Low Power Features in PSoC 6
- System and CPU power modes
- CPU Power Modes
- System Power Modes
- Transitioning between Power Modes
- Power Mode Transition Callbacks
- Demo
- Power Reduction Techniques
- Backup Domain

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Low Power MCU Systems

- Small
- Wireless
- Larger feature set
- Higher battery backup
- Lesser cost
- Security

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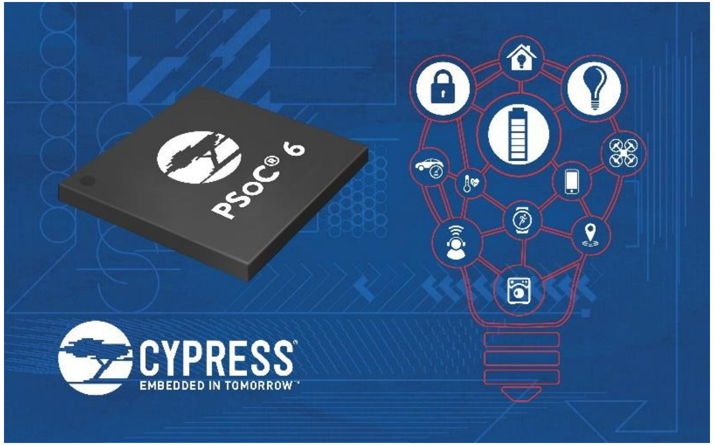
Low Power Features in PSoC 6

- Designed for low power
- No significant sacrifice in performance
- 7 power modes – 4 system and 3 CPU power modes
- MCU Active Power – 22 uA / MHz
- Low operational voltage support (1.1 V or 0.9 V)
- Low Power Assistant
- SysPm PDL, HAL driver support



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CPU Power modes

- Standard ARM-defined power modes
- Different CPU power modes
  - CPU Active
  - CPU Sleep
  - CPU Deep Sleep
- Specific to the CPU and entered separately for each CPU
- Retains program state
- Based on WFI and WFE instructions
- Implementation is vendor specific

System Power modes

- Additional low power modes supported by PSoC 6
- Different System power modes
  - System Low Power
  - System Ultra Low Power
  - System Deep Sleep
  - System Hibernate
- Affects the whole system
- All CPU power modes are available in both System Low Power (LP) and System Ultra Low Power (ULP) modes

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CPU Power Modes

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Overview of CPU Power Modes

	Active	Sleep	Deep Sleep
Code Execution	• **CPU executes code**	• CPU executes WFI/WFE instruction with **Deep Sleep disabled** • CPU **halts code execution**	• CPU executes WFI/WFE instruction with **Deep Sleep enabled** • CPU halts code execution • Requests device to go into **System Deep Sleep mode**
Resources Available	• All peripherals are available • Memory is powered	• All peripherals are available • **CPU clock turned off**	• All peripherals are available • CPU clock turned off
Wakeup Source	• CPU enters Active mode on reset or wakeup	• Any peripheral interrupt will transition CPU to Active mode	• Any peripheral interrupt will transition CPU to Active mode

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System Power Modes

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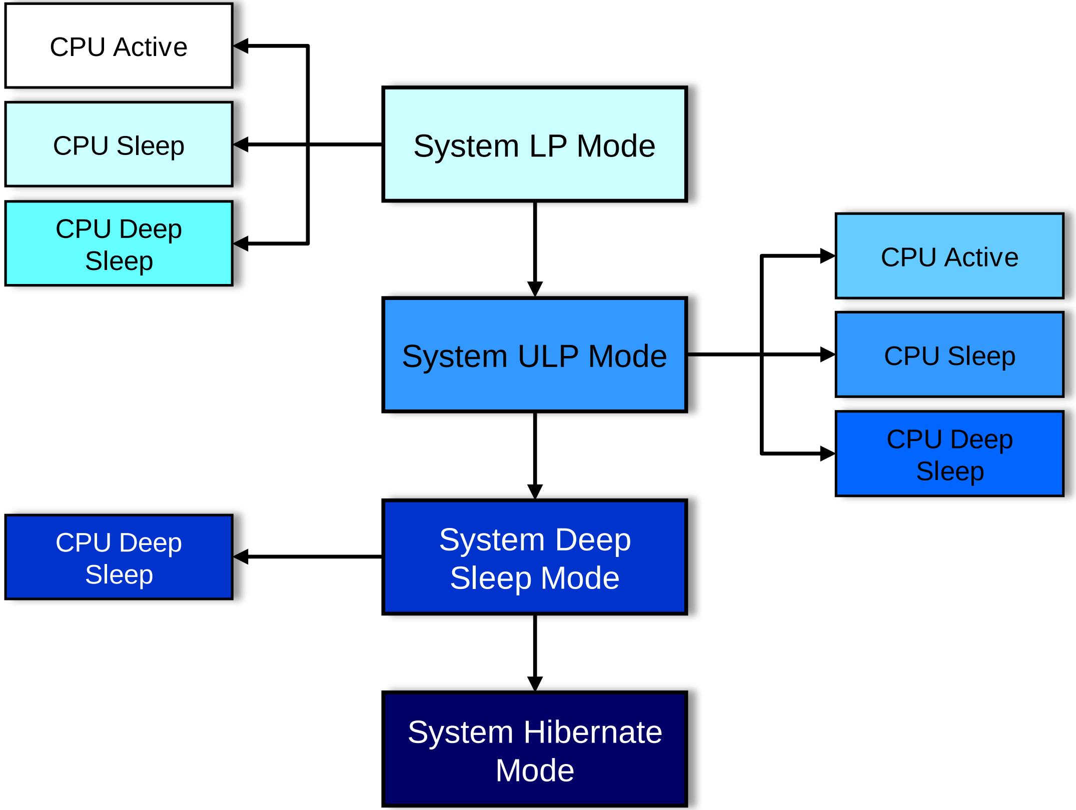
Overview of System Power Modes



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System Power Modes

	System LP Mode	System ULP Mode	System Deep Sleep	System Hibernate
Features	• Default operating mode • Maximum system performance • Maximum clock frequencies • **1.1 V core voltage**	• Restricted system performance • **Limited clock frequencies** • **0.9 V core voltage**	• Achievable when **both CM4 and CM0+ enters CPU Deep Sleep** • **LP and ULP Regulators turned off**. Deep Sleep regulators used. • Buck Regulator can be used • On wakeup only the **woken up CPU enters Active mode**. • System returns to LP or ULP	• Lowest power mode of the device • LP/ULP and Deep Sleep regulators are off • **Brown out detection is not available**. • Supply should be stable for at least 250 us before entering Hibernate mode • **GPIO states are frozen** • Device **resets on wakeup** -> Reset reason is Hibernate Wakeup
Resources Available	• All resources are available	• HF Clocks are restricted to 50 MHz • Peripheral and slow clocks restricted to 25 MHz • **No Flash write actions** • All resources are available	• HF Clocks are disabled. • High speed peripherals not available. • **Low speed clocks and peripherals** available. • Externally clocked peripheral (Deep Sleep capable SPI/I2C slave). • **SRAM blocks can be retained**. • **LPComp, WDT, MCWDT, RTC**	• All peripherals and clocks are off • **PWR_HIBERNATE and PWR_HIB_DATA registers are retained**. • ILO • LPComp, WDT, RTC
Wakeup Source	• Any interrupt to CPU	• Any interrupt to CPU	• GPIO • LPComp • SCB • CTBm • WDT • RTC alarm	• Wakeup pins • LPComp (requires externally generated voltages for wakeup) • WDT • RTC alarm

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An Example…

1 System LP

- User active
- Max performance for continuous tracking
- CPU in Active mode

2 System ULP

- User in rest for more than 15 min
- CPU in Sleep mode

3 System Deep Sleep

- Night
- User in rest for more than an hour

4 System Hibernate

- Battery Low
- Save tracking data

Movement Tracking Watch

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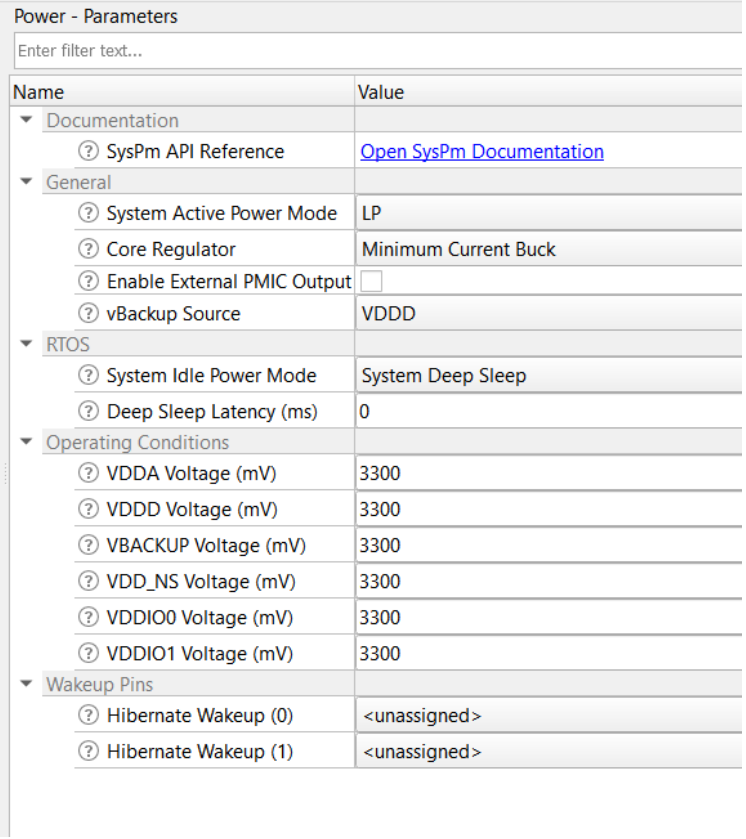
Low Power Assistant



Power - Parameters

Enter filter text...

Name	Value
Documentation	
SysPm API Reference	Open SysPm Documentation
General	
System Active Power Mode	LP
Core Regulator	Minimum Current Buck
Enable External PMIC Output	□
vBackup Source	VDDD
RTOS	
System Idle Power Mode	System Deep Sleep
Deep Sleep Latency (ms)	0
Operating Conditions	
VDDA Voltage (mV)	3300
VDDD Voltage (mV)	3300
VBACKUP Voltage (mV)	3300
VDD_NS Voltage (mV)	3300
VDDIO0 Voltage (mV)	3300
VDDIO1 Voltage (mV)	3300
Wakeup Pins	
Hibernate Wakeup (0)	<unassigned>
Hibernate Wakeup (1)	<unassigned>

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Transitioning between Power Modes

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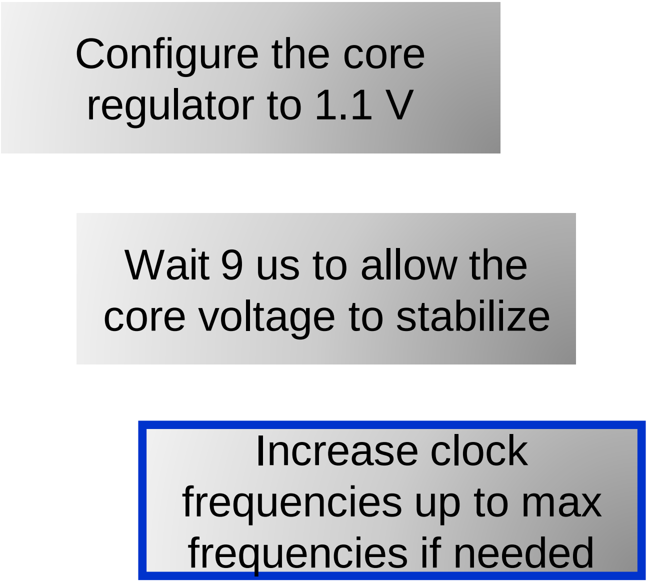
Transitioning to System LP Mode



Configure the core regulator to 1.1 V

Wait 9 us to allow the core voltage to stabilize

Increase clock frequencies up to max frequencies if needed

*Blue outline indicates that the step needs to be performed by the application.

To transition to low power -

```
cyhal_syspm_set_system_state(CYHAL_SYSPM_SYSTEM_NORMAL);
```

- API takes care of setting the right core regulator voltage.
- Returns success of the transition is successful.

To change clock frequency –

```
cyhal_clock_set_frequency()
```

- The clocks need to be configured by the application

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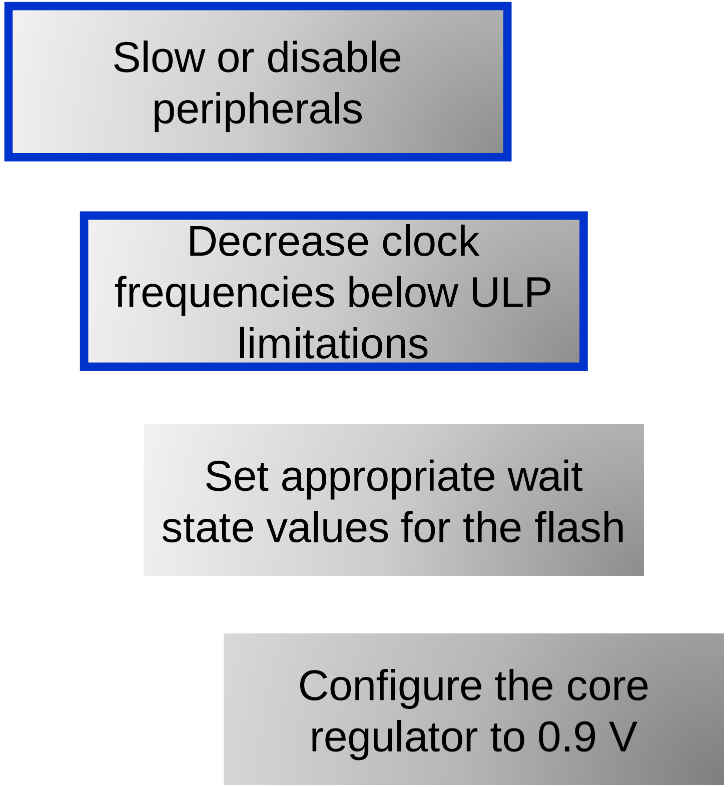
Transitioning to System ULP Mode



Slow or disable peripherals

Decrease clock frequencies below ULP limitations

Set appropriate wait state values for the flash

Configure the core regulator to 0.9 V

*Blue outline indicates that the step needs to be performed by the application.

To change clock frequency –

```
cyhal_clock_set_frequency()
```

- The clocks need to be configured by the application

To transition to low power -

```
cyhal_syspm_set_system_state(CYHAL_SYSPM_SYSTEM_LOW);
```

- API takes care of setting the appropriate wait states and core regulator voltage.
- Returns success of the transition is successful.

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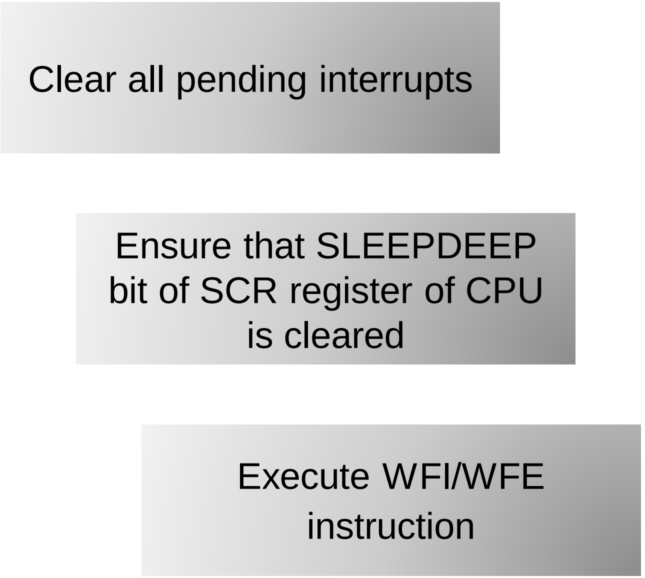
Transitioning to CPU Sleep Mode



Clear all pending interrupts

Ensure that SLEEPDEEP bit of SCR register of CPU is cleared

Execute WFI/WFE instruction

To transition to low power -

```
cyhal_syspm_sleep();
```

- HAL API takes care of clearing the SLEEPDEEP bit and executing the WFI/WFE instruction.
- Returns success of the transition is successful.

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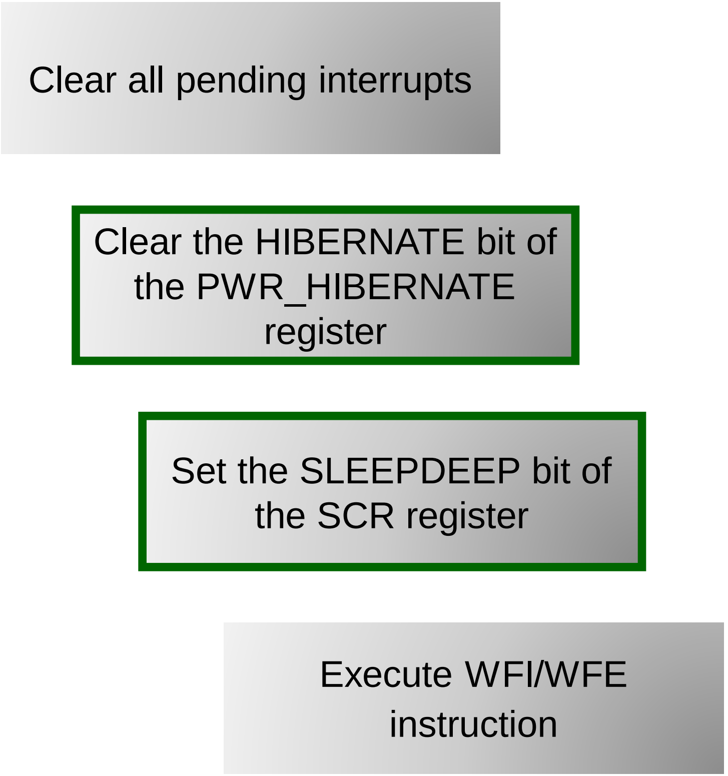
Transitioning to System Deep Sleep Mode



Clear all pending interrupts

Clear the HIBERNATE bit of the PWR_HIBERNATE register

Set the SLEEPDEEP bit of the SCR register

Execute WFI/WFE instruction

*Green outline indicates the steps that are different from CPU Sleep transition

To transition to low power -

`cyhal_syspm_deepsleep();`

- API takes care of setting the appropriate wait bits and executing ARM instructions.
- Returns success of the transition is successful.
- Application must ensure that both CPUs call the API to enter System Deep Sleep.

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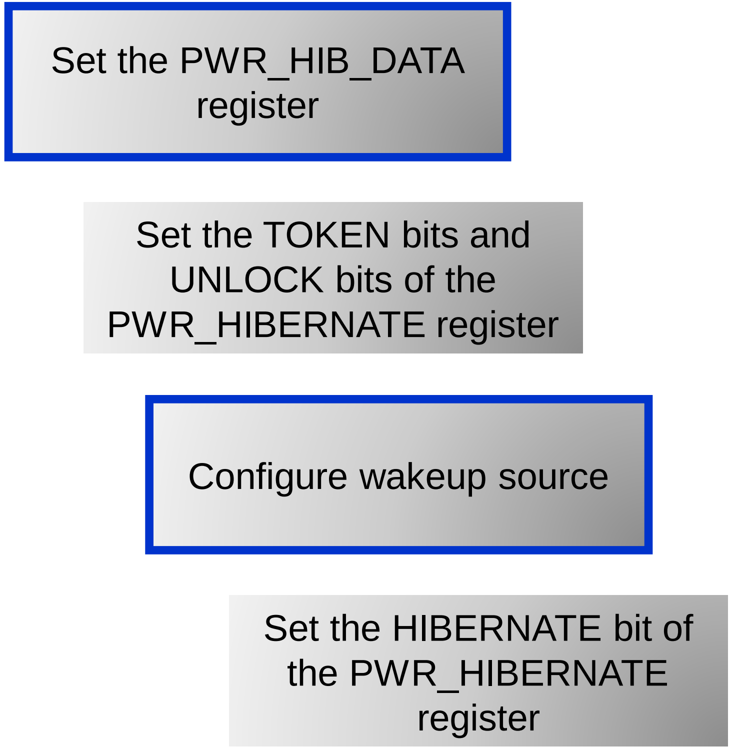
Transitioning to System Hibernate Mode



Set the PWR_HIB_DATA register

Set the TOKEN bits and UNLOCK bits of the PWR_HIBERNATE register

Configure wakeup source

Set the HIBERNATE bit of the PWR_HIBERNATE register

*Blue outline indicates that the step needs to be performed by the application.

To transition to low power -

```
cyhal_syspm_hibernate(<wakeup_source>);
```

- HAL API takes care of the entire process other than setting PWR_HIB_DATA.
- Returns success of the transition is successful.
- Application specific data can be retained in the PWR_HIB_DATA register if needed by the application.

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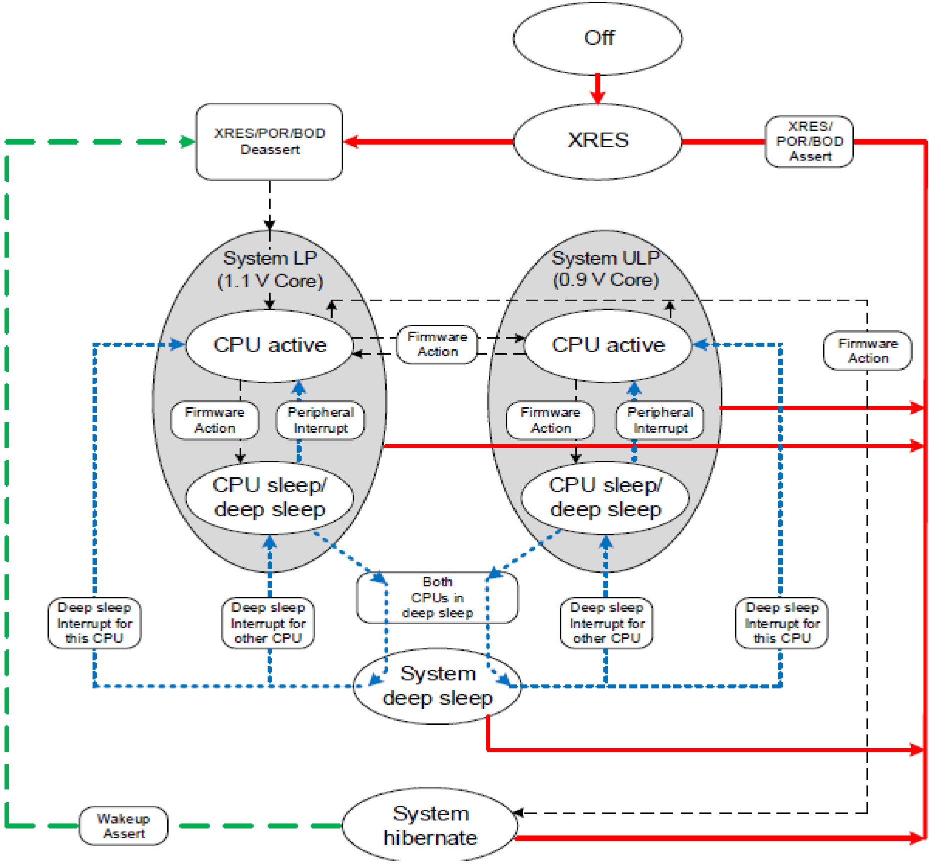
Transitioning Flow Diagram



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Power Mode Transition Callbacks

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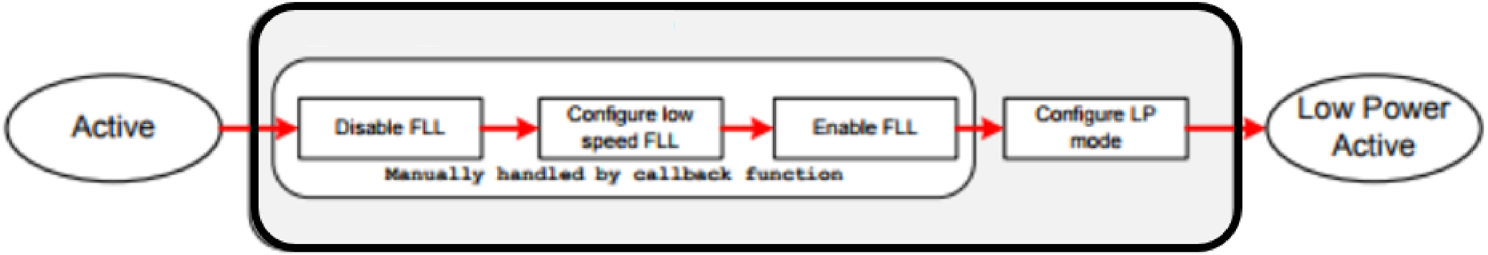
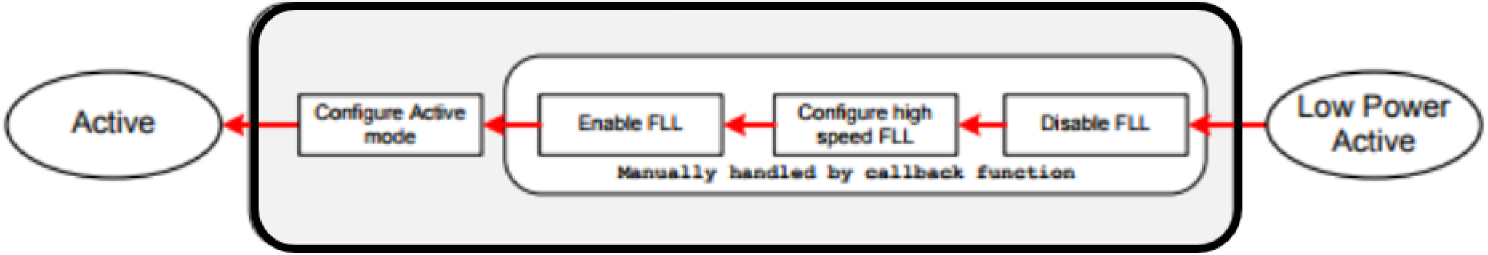
Callback Functions





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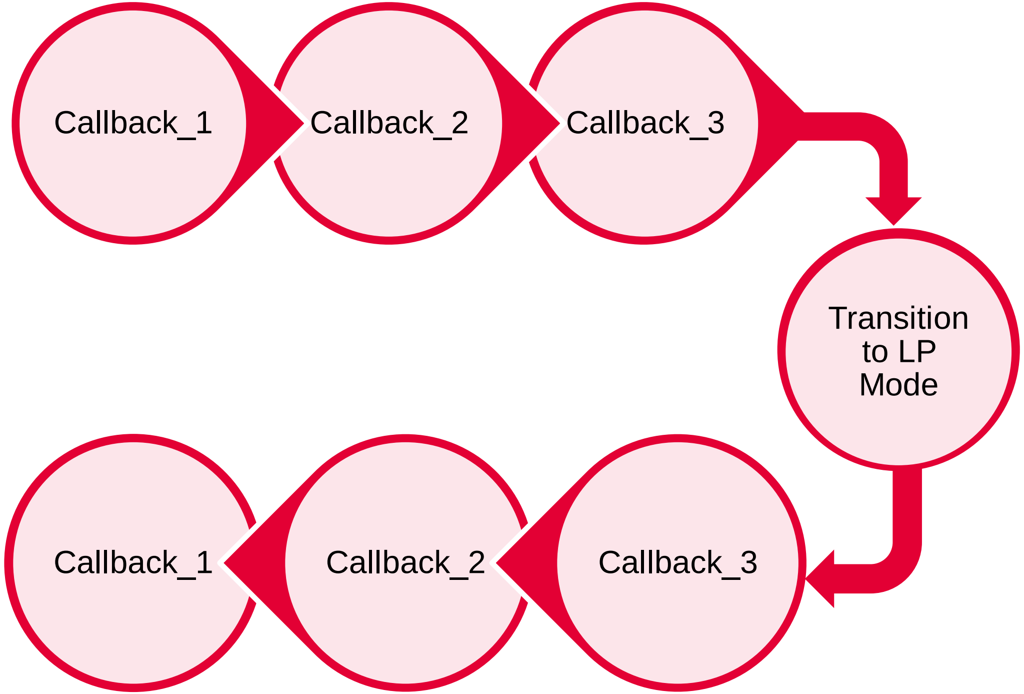
Callback Sequence

- Generally each peripheral gets a callback
- Sequence based on order of registration
- Global resource callbacks should be registered last
- Should not be modified after registration



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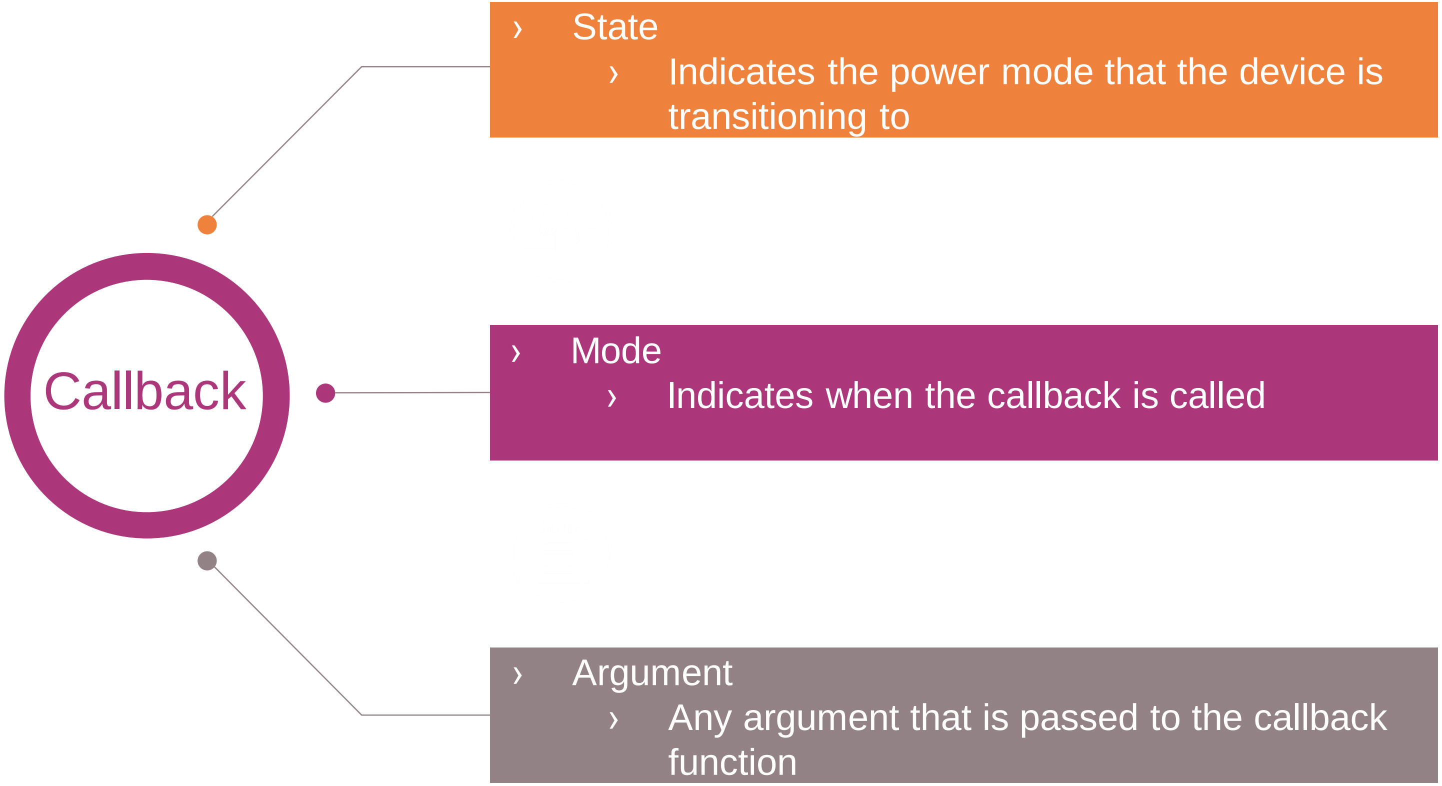
Callback Parameters



Callback

- State
  - Indicates the power mode that the device is transitioning to
- Mode
  - Indicates when the callback is called
- Argument
  - Any argument that is passed to the callback function

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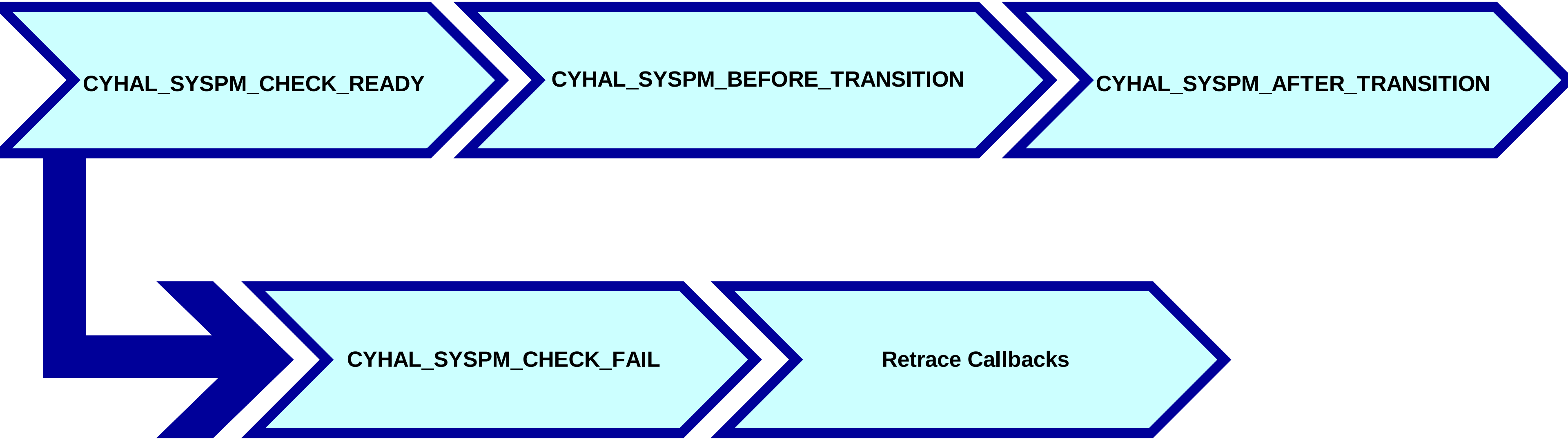
Callback Execution Flow



CYHAL_SYSPM_CHECK_READY

CYHAL_SYSPM_BEFORE_TRANSITION

CYHAL_SYSPM_AFTER_TRANSITION

CYHAL_SYSPM_CHECK_FAIL

Retrace Callbacks

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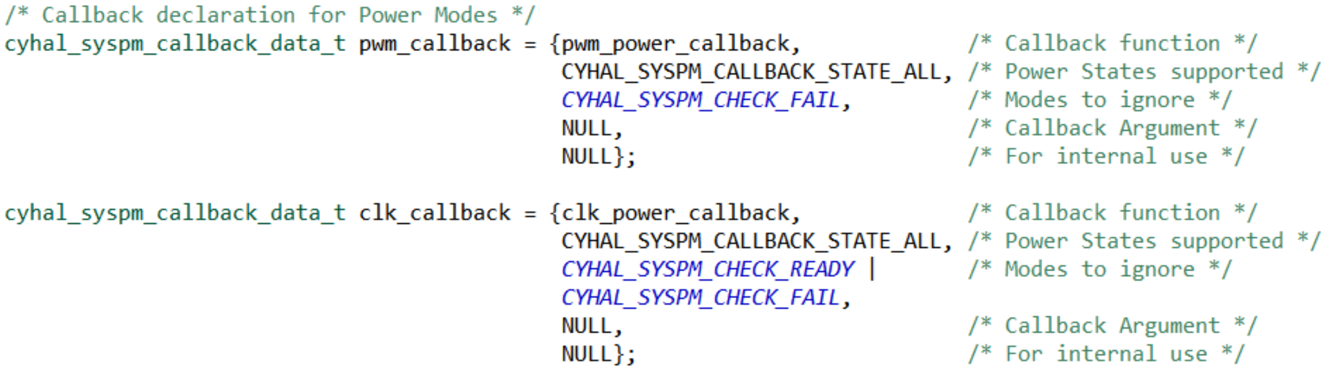
Callback Usage

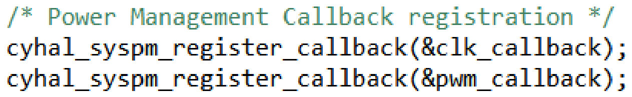
- Callback Declaration



```
/* Callback declaration for Power Modes */
cyhal_syspm_callback_data_t pwm_callback = {pwm_power_callback,          /* Callback function */
                                             CYHAL_SYSPM_CALLBACK_STATE_ALL, /* Power States supported */
                                             CYHAL_SYSPM_CHECK_FAIL,         /* Modes to ignore */
                                             NULL,                           /* Callback Argument */
                                             NULL};                          /* For internal use */

cyhal_syspm_callback_data_t clk_callback = {clk_power_callback,          /* Callback function */
                                             CYHAL_SYSPM_CALLBACK_STATE_ALL, /* Power States supported */
                                             CYHAL_SYSPM_CHECK_READY |       /* Modes to ignore */
                                             CYHAL_SYSPM_CHECK_FAIL,
                                             NULL,                           /* Callback Argument */
                                             NULL};                          /* For internal use */
```

- Callback Registration



```
/* Power Management Callback registration */
cyhal_syspm_register_callback(&clk_callback);
cyhal_syspm_register_callback(&pwm_callback);
```

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Demo

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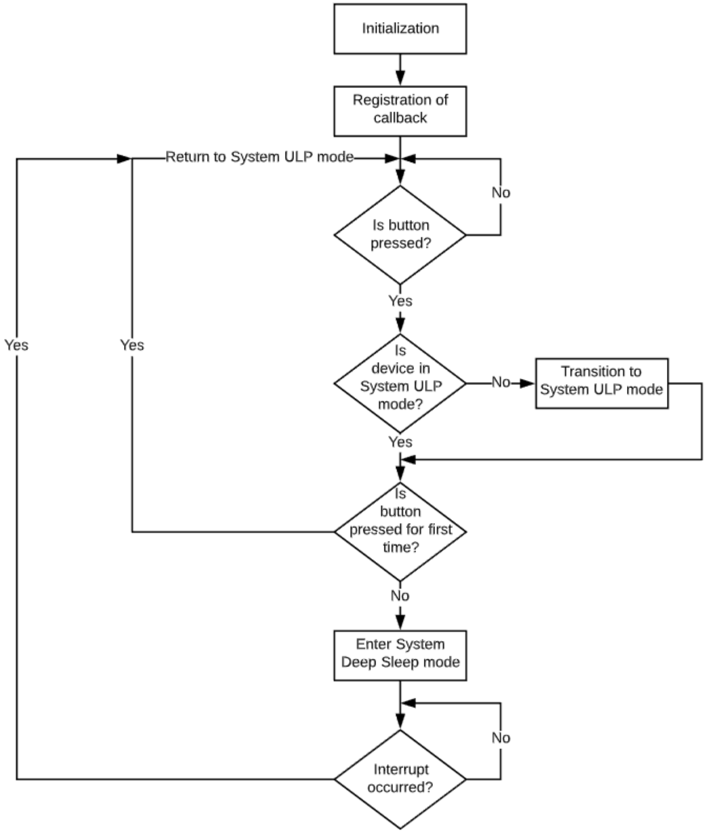
Demo – System Deep Sleep Mode



Initialization
Registration of callback
Return to System ULP mode
Is button pressed?
No
Yes
Is device in System ULP mode?
No
Transition to System ULP mode
Yes
Yes
Yes
Is button pressed for first time?
No
Enter System Deep Sleep mode
Interrupt occurred?
No

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Demo – System Deep Sleep Mode

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Power Reduction Techniques

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Disable Unnecessary Resources

- GPIO pins
  - Change GPIO pin state to High Impedance
- External Components
  - Powering through PSoC and disabling it in firmware
- Disable peripherals
- Disable Debug Mode
- Disable unused SRAM pages and/or banks
  - Each page is generally 32 KB
  - Use of custom linker scripts
- Disable UDBs (if present)

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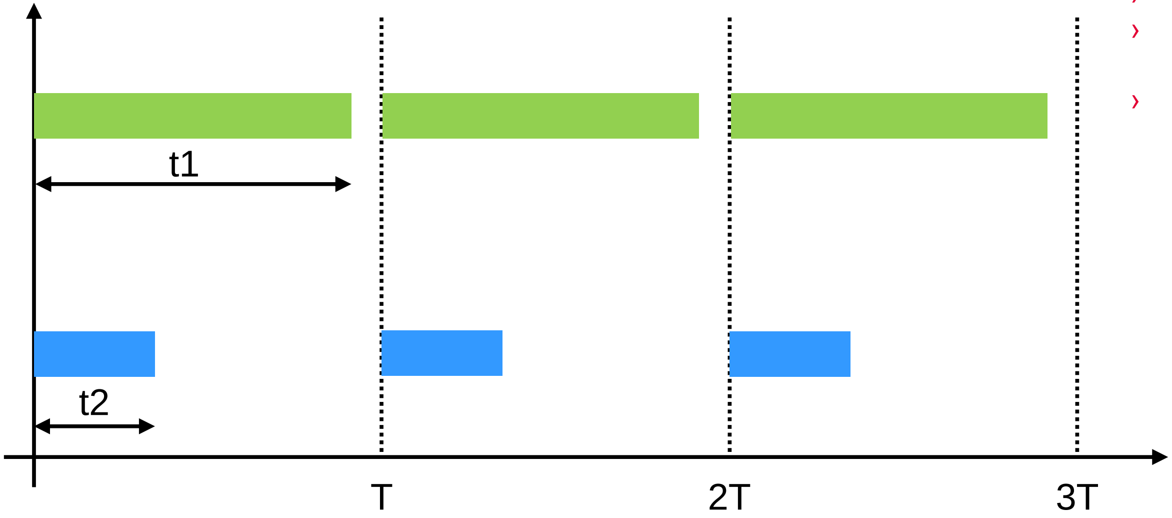
Clock Speeds

- Application specific



- T – Sensor sampling time
- t1 – Processing time with lower clock speeds
- t2 – Processing time with higher clock speeds

- Use appropriate clocks for peripherals
  - Do not use 1 MHz clock for a timer with 1 second period

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Other Power Reduction Techniques

- Use DMA for data transfer
- Avoid blocking functions -> poll for interrupt based events
- Select the SCB that has Deep Sleep capability
- Select GPIO with wakeup capability
- Select appropriate regulator and core voltage

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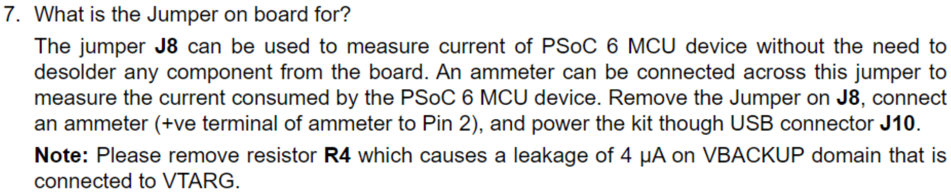
Factors affecting the current measured

- Multimeter accuracy
- Multimeter shunt resistor
- Current measurement guidelines of the Kit



7. What is the Jumper on board for?

   The jumper **J8** can be used to measure current of PSoC 6 MCU device without the need to desolder any component from the board. An ammeter can be connected across this jumper to measure the current consumed by the PSoC 6 MCU device. Remove the Jumper on **J8**, connect an ammeter (+ve terminal of ammeter to Pin 2), and power the kit though USB connector **J10**.

   Note: Please remove resistor **R4** which causes a leakage of 4 µA on VBACKUP domain that is connected to VTARG.

- Datasheet current measurement conditions

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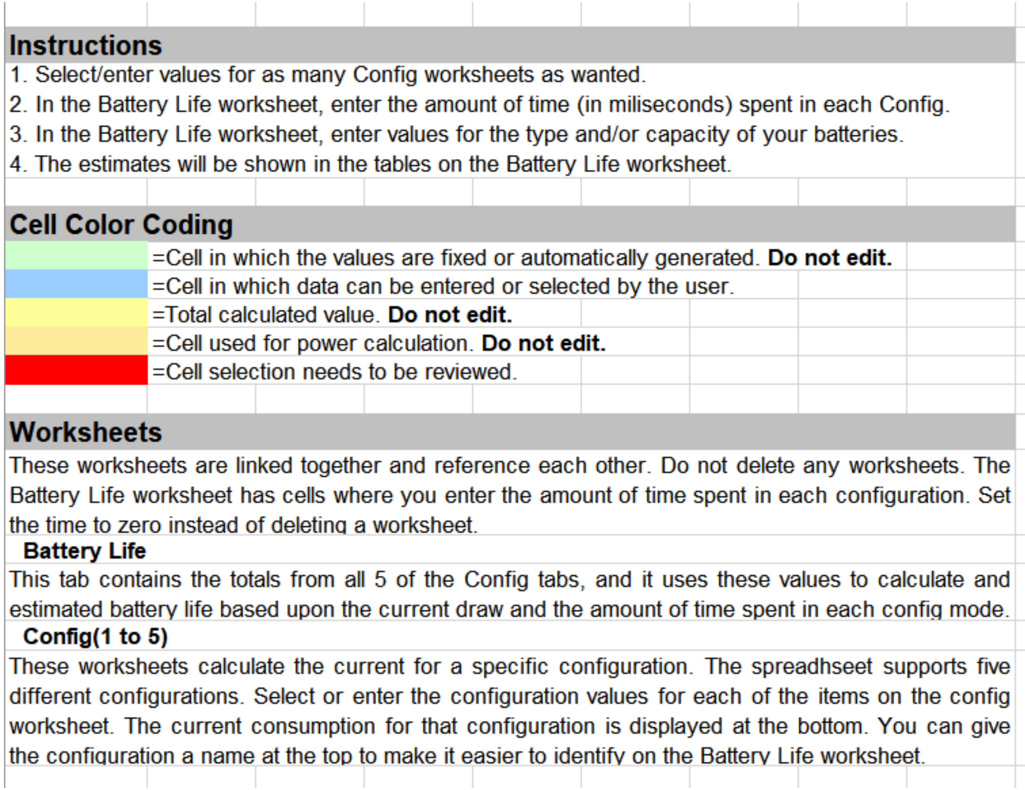
Approximating Power Consumption – PSoC6 Power Calculator

Instructions



Instructions

1. Select/enter values for as many Config worksheets as wanted.
2. In the Battery Life worksheet, enter the amount of time (in miliseconds) spent in each Config.
3. In the Battery Life worksheet, enter values for the type and/or capacity of your batteries.
4. The estimates will be shown in the tables on the Battery Life worksheet.

Cell Color Coding

🟩 =Cell in which the values are fixed or automatically generated. **Do not edit.**

🟦 =Cell in which data can be entered or selected by the user.

🟨 =Total calculated value. **Do not edit.**

🟧 =Cell used for power calculation. **Do not edit.**

🟥 =Cell selection needs to be reviewed.

Worksheets

These worksheets are linked together and reference each other. Do not delete any worksheets. The Battery Life worksheet has cells where you enter the amount of time spent in each configuration. Set the time to zero instead of deleting a worksheet.

Battery Life

This tab contains the totals from all 5 of the Config tabs, and it uses these values to calculate and estimated battery life based upon the current draw and the amount of time spent in each config mode.

Config(1 to 5)

These worksheets calculate the current for a specific configuration. The spreadhseet supports five different configurations. Select or enter the configuration values for each of the items on the config worksheet. The current consumption for that configuration is displayed at the bottom. You can give the configuration a name at the top to make it easier to identify on the Battery Life worksheet.

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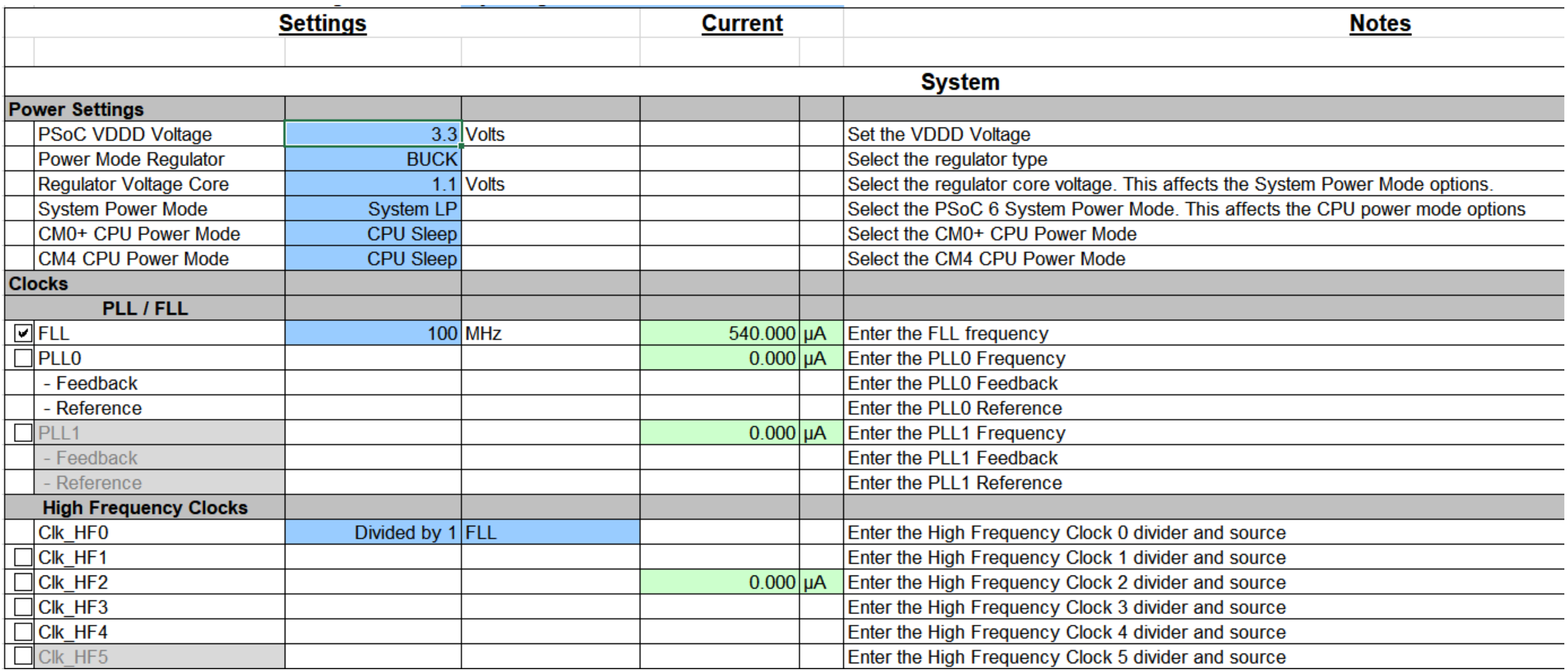
Approximating Power Consumption – PSoC6 Power Calculator

Filling in details



		Settings		Current		Notes
						System
Power Settings						
	PSoC VDDD Voltage	3.3	Volts			Set the VDDD Voltage
	Power Mode Regulator	BUCK				Select the regulator type
	Regulator Voltage Core	1.1	Volts			Select the regulator core voltage. This affects the System Power Mode options.
	System Power Mode	System LP				Select the PSoC 6 System Power Mode. This affects the CPU power mode options
	CM0+ CPU Power Mode	CPU Sleep				Select the CM0+ CPU Power Mode
	CM4 CPU Power Mode	CPU Sleep				Select the CM4 CPU Power Mode
Clocks						
	PLL / FLL					
☑	FLL	100	MHz	540.000	µA	Enter the FLL frequency
□	PLL0			0.000	µA	Enter the PLL0 Frequency
	- Feedback					Enter the PLL0 Feedback
	- Reference					Enter the PLL0 Reference
□	PLL1			0.000	µA	Enter the PLL1 Frequency
	- Feedback					Enter the PLL1 Feedback
	- Reference					Enter the PLL1 Reference
	High Frequency Clocks					
	Clk_HF0	Divided by 1	FLL			Enter the High Frequency Clock 0 divider and source
□	Clk_HF1					Enter the High Frequency Clock 1 divider and source
□	Clk_HF2			0.000	µA	Enter the High Frequency Clock 2 divider and source
□	Clk_HF3					Enter the High Frequency Clock 3 divider and source
□	Clk_HF4					Enter the High Frequency Clock 4 divider and source
□	Clk_HF5					Enter the High Frequency Clock 5 divider and source

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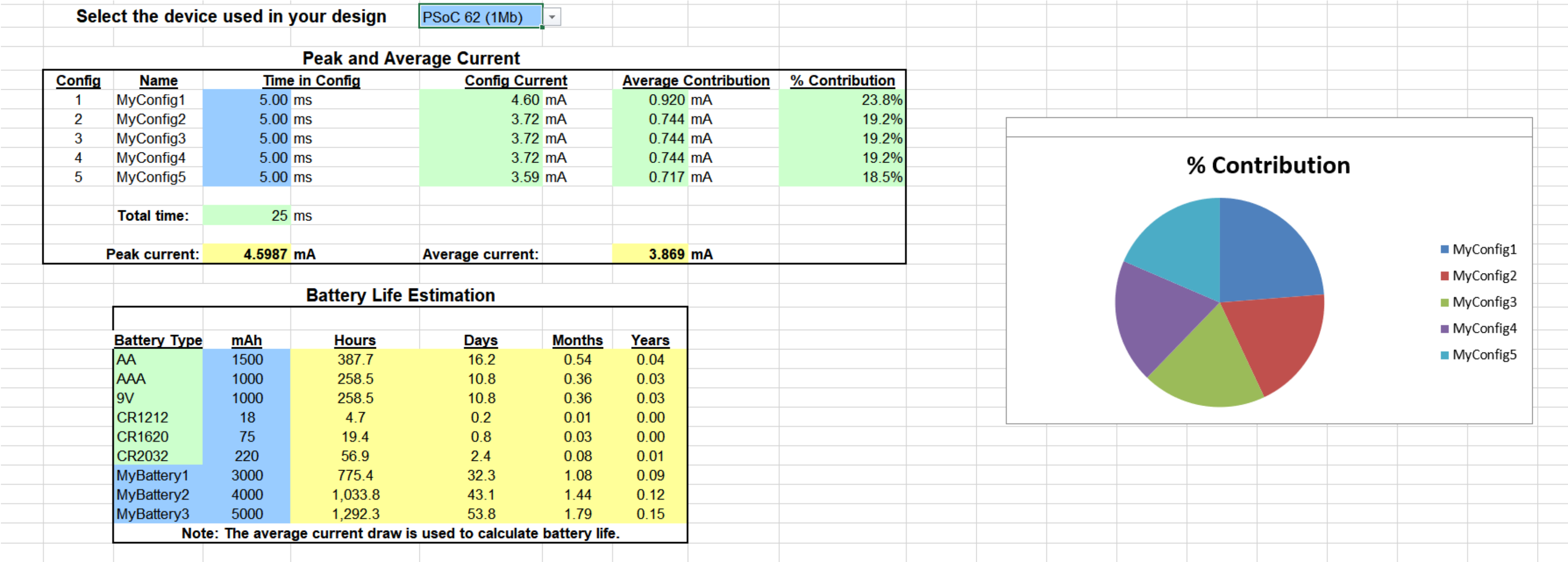
Approximating Power Consumption – PSoC6 Power Calculator

Summary



Select the device used in your design: PSoC 62 (1Mb)

Peak and Average Current

Config	Name	Time in Config		Config Current		Average Contribution		% Contribution
1	MyConfig1	5.00	ms	4.60	mA	0.920	mA	23.8%
2	MyConfig2	5.00	ms	3.72	mA	0.744	mA	19.2%
3	MyConfig3	5.00	ms	3.72	mA	0.744	mA	19.2%
4	MyConfig4	5.00	ms	3.72	mA	0.744	mA	19.2%
5	MyConfig5	5.00	ms	3.59	mA	0.717	mA	18.5%
	Total time:	25	ms					
	Peak current:	4.5987	mA	Average current:		3.869	mA	

Battery Life Estimation

Battery Type	mAh	Hours	Days	Months	Years
AA	1500	387.7	16.2	0.54	0.04
AAA	1000	258.5	10.8	0.36	0.03
9V	1000	258.5	10.8	0.36	0.03
CR1212	18	4.7	0.2	0.01	0.00
CR1620	75	19.4	0.8	0.03	0.00
CR2032	220	56.9	2.4	0.08	0.01
MyBattery1	3000	775.4	32.3	1.08	0.09
MyBattery2	4000	1,033.8	43.1	1.44	0.12
MyBattery3	5000	1,292.3	53.8	1.79	0.15

Note: The average current draw is used to calculate battery life.

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Backup Domain

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Backup Domain

- Always on functionality
- Automatic backup power switching -> $V_{DDBAK} = V_{DDD} | V_{BACKUP}$
- Reset only when power is completely removed or Backup Domain is reset through firmware
- Fully featured RTC with configurable alarm
- 32 kHz WCO
- Built-in supercapacitor charger
- External PMIC control
- 32-byte backup registers
  - BACKUP_BREG0 to BACKUP_BREG15
  - Used to store specific device related information

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Resources

- PSoC® 6 MCU Architecture TRM
- PSoC 6 MCU Low-Power Modes and Power Reduction Techniques
- PSoC 6 Power Calculator.xlsx
- HAL API Reference Guide
- ModusToolbox® Software Environment
- Code Examples: Github repository

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